DESIGN AND ANALYSIS OF NEW HIGH SPEED PERISTALTIC CCD'S

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ABSTRACT

Novel embodiments of silicon peristaltic CCD's for high speed operation are presented and analyzed. Included is a description of an input technique which shows promise of charge injection over a wide linear range at frequencies approaching 1 GHz. A nondestructive readout technique capable of greater than 100 MHz bandwidth, as well as on-chip drive circuits for reducing reactive power dissipation are described. Analysis is also presented showing that high speed transfer can be achieved with short gates and channel depths not exceeding several microns, allowing the buried channel to be implemented by ion-implantation rather than by epitaxial deposition. Such ion-implanted structures result in lower thermal leakage current than comparable epitaxial structures.

1.0 Introduction

Historically, peristaltic CCD's have been fabricated using an epitaxial structure[1]. Signal charge is confined in the epitaxial layer away from the surface in a region in which the electric fringe field between transfer gates is a maximum. The last fraction of charge under a gate is then efficiently transferred at high clock rates. Charge transfer experiments using a uniphase clock have projected clock rates of ~ 1 GHz with charge transfer inefficiencies of $\sim 10^{-4}$[2]. However, devices taking advantage of such data rates have not been realized because of limitations resulting from the CCD input and output structures, efficient clocking techniques at high speed, and degradation due to leakage charge and charge transfer inefficiency arising from epitaxial crystal quality. The following paper describes new techniques which address these difficulties and present analytical results supporting projections of improved performance.

2.0 Analysis of CCD Charge Transfer Characteristics and Bandwidth

In the operation of charge coupled devices, the free-charge transfer characteristics are determined by incomplete transfer of charge due to: (1) insufficient transfer time, and (2) trapping of fast interface states and bulk traps. High-speed operation of CCD's pose interesting problems quite different from the conventional problems associated with input, clocking, and output of signal charge. At the present time, it is certainly not at all clear that low values of transfer inefficiency ($\epsilon < 10^{-4}$) can be maintained when the transfer time is reduced below 5 nsec and still provide distinct isolation of charge packets along the CCD delay line. As the electrode length L is decreased to shorten the characteristic transfer time (i.e., $\tau_c = L^2/\mu$ (1 volt), with μ an effective free carrier mobility), the potential wells that define and isolate the charge packets become "spread-out" in a two-dimensional sense. In order to counter this effect, the substrate doping density is increased which reduces the so-called fringe field that provides efficient charge transfer for the remaining 1 percent of the charge in a potential well. The reduction of fringe field is countered by locating the centroid of the remaining charge further from the Si/SiO_2 interface into the bulk silicon, thereby increasing the coupling of the drive clock voltages to accelerate the free-charge transfer. The result of this action is to reduce the charge-handling capability of the CCD structure which is countered by "profiling" and involves the use of a two-step doping process: (1) a shallow, heavy doped region near the silicon surface to increase the charge-handling, and (2) a deep, lightly-doped region to provide efficient transfer of the remaining charge. Therefore, there is a unique set of device parameters and material parameters needed to obtain a specified level of performance in high-speed operation.

There are three basic mechanisms of charge motion in the CCD structure: (1) self-induced drift, (2) thermal diffusion, and (3) fringe-field drift. The dynamics of free-charge transfer (i.e., transfer in the absence of generation-recombination mechanisms) can be described by a one-dimensional charge transfer equation.[3]

$$\frac{\partial \rho}{\partial t} = -\frac{\partial}{\partial y}(\mu \rho E) \tag{1}$$

where ρ is the charge density, E the total tangential electric field in the direction of charge transport, y, and μ is the effective free-carrier mobility.

The total electric field is composed of the following terms:

$$E = E_{sd} + E_{th} + E_{fr} \tag{2}$$

where E_{sd} is a self-induced drift field given by

$$E_{sd} = -\frac{1}{C_{eff}} \frac{\partial \rho}{\partial y} \tag{3}$$

and $C_{eff.}$ is defined by the expression,

(4)

$$\frac{1}{C_{eff}} = \frac{X_0\,(eff)}{K_0\,\epsilon_o} + \frac{d}{K_S\,\epsilon_o}\left[1 - \frac{\Delta d}{d} - \frac{Q_S}{2N_{ion}}\right]$$

with X_O the effective oxide thickness (e.g., for a dual-electric system X_O (eff.) = X_O + (K_O /K_N X_N as in the case for Si_3N_4 /SiO_2), and d is the distance from the Si/SiO_2 interface into the silicon, where the centroid of the charge is located, Δd is the width of the charge centroid, Q_s is the signal charge density, and N_{ion} is the effective donar concentration in the epitaxial or ion-implanted region. Equation (4) neglects the repulsive field effects due to the image force in the gate electrode. The thermal field component of the total electric field may be written as,

$$E_{th} = -\frac{kT}{q} \frac{1}{\rho} \frac{\partial \rho}{\partial y} \tag{5}$$

and the fringe electric field is determined by the geometry, material parameters, and external clock voltage, and may be approximated by the expression[4]

$$E_{fr}(min) = \frac{\Delta V}{L}\left[e^{-\pi K_S \epsilon_o / 3C_{eff.} L} - e^{\pi K_S \epsilon_o / C_{eff.} L}\right] \tag{6}$$

where $C_{eff.}$ is defined by equation (4) and ΔV is the voltage difference between the transfer electrode and the receiving electrode (L is the length of the transfer electrode). The minimum fringe field is important because for small channel lengths the remaining charge is confined to the center of the gate electrode where the fringe field is a minimum. Plotting fringe field along the channel length under a transfer gate electrode, a linear approximation to $1/E_{fr}$ (where $E_y = E_{fr}$) is observed which is useful in the evaluation of a single carrier transit time given by the expression,

$$\tau_f = \frac{1}{\mu}\int_0^L \frac{dy}{E_F(y)} \cong \frac{L}{2\mu E_F(min)} \tag{7}$$

The important effect of the fringe field occurs after the initial charge profile is relaxed and within 800 psec, since the charge transfer process becomes dominated by the fringe field term. In the early part of the charge transfer the self-induced drift may dominate for large charge densities (i.e., $\rho/q > 10^{10}$ cm^{-2}); however, within a nanosecond, the effects of thermal diffusion and fringe fields determine the final charge transfer. Thus, approximately 99 percent of the charge in a full well may be transferred by self-induced drift, but to achieve 99.99 percent transfer efficiency (i.e., transfer inefficiencies $\epsilon < 10^{-4}$), the thermal diffusion and fringe fields must be large. Fringe fields enable 99.99 percent transfer efficiencies (in the absence of trapping effects) to be obtained in several nanoseconds. The absence of fringe fields means the charge transfer process is determined by thermal diffusion with typical times of several hundred nanoseconds.

The effect of the fringe field may be included in the field enhanced diffusion constant[5] which may be written as,

$$D_{eff.} = D + \frac{2\mu L}{\pi} E_{fr}(min) \tag{8}$$

Therefore, the time constant of charge transfer in the final stages is given as,

$$\tau_{eff.} = 4L^2/\pi^2 D_{eff.} \tag{9}$$

The transfer inefficiency, ϵ can then be written as,

$$\epsilon(t) = e^{-t/\tau_{eff.}} \qquad (10)$$

where, in a two-phase clock structure, the time allotted for charge transfer is given by,

$$t(max) = (1/2)f_c \qquad (11)$$

with f_c as the clock frequency.

The analog signal transfer characteristic of a SI/SO delay line is a function of the product $Np\epsilon$, where N is the number of stages of delay, p is the number of transfers per stage, and ϵ is the transfer inefficiency. A useful criteria for defining analog signal bandwidth of a device is when the signal amplitude output suffers a 3-dB attenuation with respect to the input. This criteria can be shown to satisfy the relationship

$$Np\epsilon = 0.2 \qquad (12)$$

for a maximum baseband frequency component satisfying the Nyquist sampling criteria:

$$f_s(max) = BW = fc/2 \qquad (13)$$

Therefore, combining equations (10) through (13) we have

$$BW = \frac{1}{4\ \tau_{eff.}\ \ln[5Np]} \qquad (14)$$

Finally, by combining equations (4), (6), (8), (9), and (14), the overall expression for the analog bandwidth (BW), in terms of the geometrical, material, and electrical parameters of the CCD structure, can be formulated:

$$BW = \frac{\pi^2 \mu}{16L^2 \ln[5Np]} \left[kT/q + \frac{2L}{\pi} E_{fr}(min.) \right] \qquad (15)$$

where E_{fr} (min.) is defined by equation (6). Table 1 illustrates the calculation of BW as a function of charge centroid "d" defined in equation (4) and illustrated in Figure 1, and the electrode length "L" for an 800-stage CCD with the fixed parameters indicated.

d (μm) / L (μm)	0.2	0.5	1.0	1.5	2.0	2.5
7.0	82	103	128	145	155	161
5.0	204	246	291	313	319	375
4.0	365	428	484	496	487	---
3.0	753	844	885	849	---	---
2.0	1910	1990	1820	----	----	----

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Table 1
Bandwidth of a CCD Analog Delay Line in MHz as a Function of Gate Length and d

- N = No. of stage delays = 800
- p = No. of transfers/delay = 4
- ΔV = Effective channel mobility of electrons = 1,000 cm²/V-sec
- X_O = Oxide thickness = 1700 A°
- X_N = Nitride thickness = 500 A°
- K_O = 3.85; K_N = 6.5; K_s = 11.8

The elements in table 1 are not completed for d > L/2 because the minimum fringe field E_{fr} (min.) decreases after this point. The important features of table 1 are:

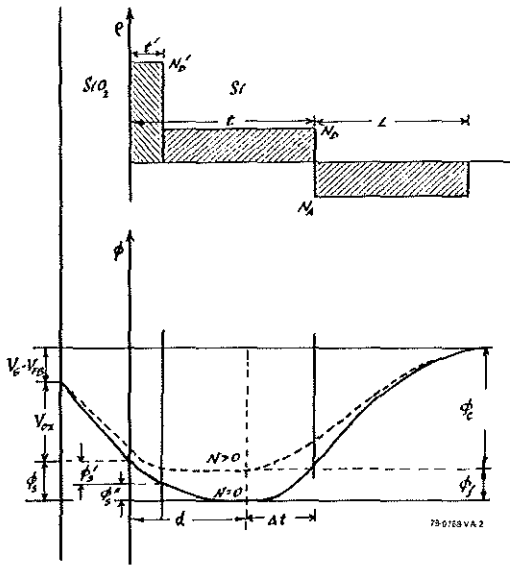

Figure 1. Energy Band Diagram and Potential Plot of PCCD with Profiled Channel

a. High-speed CCD analog delay lines with bandwidths exceeding 400 MHz are possible with 4 μm electrode lengths, 5-volt clock swing, and n epitaxial thicknesses greater than 0.4 μm, where the film thickness is approximately twice the centroid of charge, d.

b. Once the charge is removed from the Si-SiO_2 interface, the fringe field influence increases the bandwidth; however, the major contribution is achieved within 0.2 μm for the electrode lengths considered.

The design of the PCCD structure must consider the interrelationships between the geometrical, physical, and electrical parameters of the structure. Figure 1 illustrates the profiled PCCD structure and the designation of the geometrical and physical parameters. Summation of potentials yields:

$$V_G - V_{FB} = \phi_j + \phi_c - V_{ox} - \phi_s \qquad (16)$$

where

$$\phi_j = \frac{qN_D\,\Delta t^2}{2K_s\,\epsilon_o} \qquad \phi_c = \frac{qN_AL^2}{2K_s\,\epsilon_o} \qquad (17)$$

and

$$N_D\,\Delta t = N_AL \qquad (18)$$

The oxide voltage drop may be determined by

$$V_{ox} = \frac{1}{C_{ox}} \times \left[\text{mobile charge + fixed charge}\right] \qquad (19)$$

$$= \frac{1}{C_{ox}} \times \left[N_D(t-\Delta t-t') + N_D\,t' - N_o\right]$$

Where N_o is the carrier density (carriers/cm²) in the potential minimum. An analysis of the band structure shown in Figure 1 gives the surface potential

$$\phi_s = \frac{q(t-t'-\Delta t)}{K_s\,\epsilon_o}\left[\frac{N_D}{2}(t-\;t-t') - N_o\right] + \frac{qN_D\,'t^2}{2K_s\,\epsilon_o} \qquad (20)$$

$$\text{for } N_o \leq \frac{N_D}{2}(t-t'-\Delta t)$$

and

$$\phi_s = \frac{qN_D\,t'}{2K_s\,\epsilon_o} \qquad t'-2\;\frac{N_o - \frac{N_D}{N_D'}(t-t'-\Delta t)}{} \qquad (21)$$

$$\text{for } N_o > \frac{N_D}{2}(t-t'-\Delta t)$$

In the epitaxial PCCD structure, the epitaxial layer doping is variable because $N_N < N_A$ is possible, which confines the extent of the depletion region into the substrate. Figure 2 illustrates a potential profile plot of the epitaxial PCCD for a maximum change handling capacity of $N_{max} = 3 \times 10^{11}$ carriers/cm². The plots have been obtained by numerical evaluation of the above equations. Therefore, for an electrode area of 4 μm (length) x 50 μm (width), the total charge capacity is $7 \times 10^5 e^-$. The maximum charge is determined by the condition

$$\phi_s \geq 2\;\frac{kT}{q} \qquad (22)$$

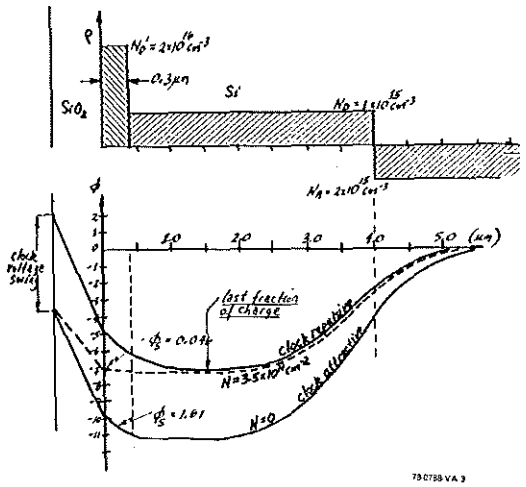

Figure 2. Epitaxial PCCD (Profiled): Dotted Lines Indicate Full-Well Profile

The last fraction of charge to transfer is located at 1.5 μm from the Si-SiO_2 interface and experiences the full magnitude of the electric fringe field. With reference to Table 1, this corresponds to a d = 1.5 μm and gives an analog bandwidth of approximately 500

MHz (f_c = 1 GHz) for an electrode length of L = 4 μm. The clock voltage swing is approximately 5 volts in this design analysis. An empty well has a surface potential ϕ_s = 1.61 volts and after loading in signal charge to a level of 3.5 x 10^{11} carriers/cm^2 the surface potential drops to ϕ_s = 0.046 volts or approximately 2kT/q. This is sufficient to avoid the surface channel mode of operation where the device suffers a transfer efficiency degradation due to charge trapping at the Si-SiO_2 interface. As is to be expected, a suitable substrate bias is required to deplete the N region.

A method, which appears very attractive for the construction of PCCD structures, is the use of deep driven ion-implantation to form the channel.[8] This fabrication technique has been used extensively for shallow so-called buried channel CCD structures. An ion- implanted band diagram is shown in Figure 3 using a numerical evaluation for surface potential. In this structure N_D is greater than N_A because of the nature of ion-implantation and diffusion to form junctions by "over-doping" the substrate. The last fraction of charge to transfer is approximately 0.7 μm from the Si:SiO_2 interface, and we see from Table 1 that a 4 μm electrode length gives an analog bandwidth of approximately 430 MHz (f_c = 860 MHz). Thus, the ion-implanted approach provides the bandwidth and also the charge-handling as N_O = 3.5 x 10^{11} carriers/cm^2 is possible with the design illustrated in Figure 3. A clock voltage swing of approximately 5 V is employed in the potential profiles. As in the epitaxial structure a substrate bias is required to translate the range of clock swing to a suitable level compatible with analog ground in the system.

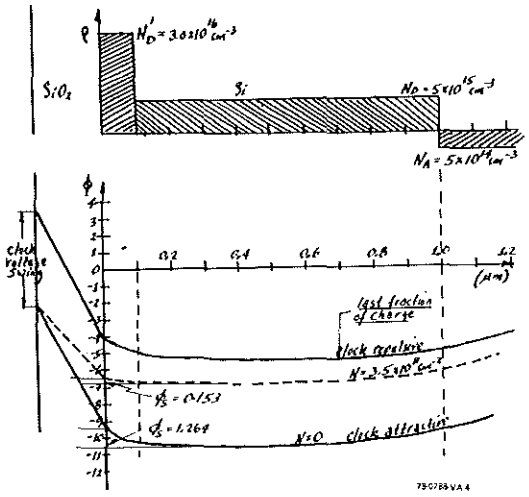

Figure 3. Ion-Implanted PCCD (Profiled): Dotted Lines Indicate Full-Well Profile

In order to achieve two-phase CCD operation, the ion-implantation profile must be adjusted along the length of the CCD device. The analysis performed above is for a full-well and a profiled PCCD. The profile ion-implant layer is adjusted to create a barrier to charge-flow in the reverse direction. With a 5-volt clock swing the barrier can be adjusted to permit 40 percent of full-well charge-handling capability.

The effects of charge trapping on surface channel CCD operation are well known to workers in the field. Analog signal processing requires a dc offset bias charge in the CCD well to enable the processing of bipolar signals. Therefore, the inherent bias charge left in the CCD well fills the interface states, which trap signal charge near the Si-SiO_2 interface. Nevertheless, the surface channel structure is still limited in signal processing because the fringe fields are small for reasonable electrode lengths. Therefore, for SI/SO delay line operation, bulk channel or buried channel operation is preferred due to the inherently more efficient transfer at high clock rates. The limitation to transfer efficiency in bulk channel CCD's is the number and location of bulk trapping states. In single crystal silicon, the number of bulk trapping centers is low on the order of 10^{11} - 10^{12} per cm^3, which leads to very high generation-recombination bulk lifetime (e.g., typically 100 μsec) and correspondingly low leakage currents (e.g., typically less than 10 nA/cm^2. The loss of charge due to bulk trapping may be analyzed as follows. When a sufficiently large charge packet enters under an electrode it rapidly fills all the bulk traps up to the conduction band edge. This fill time is strongly dependent on the signal size. In general, this process is extremely fast compared to conventional clock rates (i.e., < 10 MHz) when the charge packet is large. As the charge packet is transferred to the next electrode, the traps in the transfer electrode will re- emit a portion of the trapped signal charge, and this charge transfers along with the "main" signal packet. After the transfer time t, which is 1/1 f_c for a two-phase clock, any additional emitted charge goes into the trailing charge packet resulting in a loss of signal. The entire reasoning involved in this process is related to the filling and emptying of bulk traps. Bulk trapping states, in contrast with surface trapping states, are discrete and located within $\pm$0.1 eV of the middle of the energy gap; whereas, surface trapping states are continuous throughout the gap in density and distributed in time constants.

Although leakage current densities of the epitaxial or deep ion-implanted region are higher than virgin silicon, bulk traps are ineffective at high clock rates because they cannot emit in sufficient number to create a loss. Therefore, once the bulk traps are filled,

they are located so deep in the gap that they have insufficient time to release. This may be shown by writing the emission time of a bulk trap as

$$\tau_e = \frac{1}{\sigma_c N_t V_{th}} \exp\ (\Delta E/kT) \qquad (23)$$

where σ_c is the capture cross section of the trap, N_t the density of traps, and V_{th} the thermal velocity. ΔE is the activation energy of the trap which is near the center of the gap. If worst case numbers are used such as $\sigma_c = 10^{-15}$ cm^2, $N_t = 10^{16}$ cm^{-3}, $V_{th} = 10^7$ cm/sec, and $\Delta E = 0.45$ eV a value for trap lifetime is calculated:

$$\tau_e \text{ (bulk traps)} \cong 0.5 \text{ sec} \qquad (24)$$

which is long compared to a transfer time of a charge packet at high speed. The loss of charge per transfer in the first signal packet after "M" empty packets may be written as:

$$N_{loss}(M) = V_{sig.} \sum_i N_{ti}\, e^{T/\tau_{ei}} (1 - e^{-MT_c/\tau_{ei}}) \qquad (25)$$

where $V_{sig.}$ is the volume that the signal charge occupies, N_{ti} is the density of the i^{th} trapping state which has the emission time τ_e, T is the transfer time (e.g., $T = 1/2\ f_c$), and $T_c = 1/f_c$. Therefore, bulk trapping states responsible for increase in leakage current density cannot be responsible for the loss in the CCD at high frequency since their time constants are much too long to re-emit once they are filled. Equation (25) indicates that in order to observe such losses, the PCCD must be clocked at a slow rate and have a large number of empty packets such that $MT_c = 0.01\ \tau_e$.

A mode of PCCD operation for which this effect may have consequence is fast/slow clocking. This mode of operation is used for recording high speed transient data or high resolution radar signals. Since the ion-implanted deep driven structure has better physical properties (less defects) than a deposited epitaxial thin film, the former structure can be expected to yield lower leakage current devices with better transfer efficiency because of lower bulk trapping densities.

3.0 A Novel Bipolar CCD Input Structure with a 1-GHz Injection Bandwidth

The CCD input structure limits the maximum information bandwidth of the device. Therefore, any input structure for high frequency CCD's must satisfy guidelines appropriate for high frequency operation. Specifically, the input structure must be made from high frequency components. The procedure for metering analog charge packets into the CCD well should involve only a single step because metering techniques requiring several steps require bandwidths several times larger than the bandwidth of the input signal. Moreover, the input signal level and the impedance of the input structure must be amenable for coupling with the outside world. Cognizant of these requirements a new high speed CCD input structure has been designed which is amenable to coupling with the CCD shift register and does not require additional input clocking circuits. The new structure makes use of high speed bipolar transistor technology and high speed circuit theory for common base structures. Moreover, incorporation of a bipolar mirror into the input structure overcomes the problem of interfacing the input structure with the outside world. Consider the input structure shown in Figure 4(a) consisting of a double diffused lateral transistor and its mirror drawn, for purposes of clarity, outside the silicon substrate. In the actual device, the mirror transistor represented by the transistor symbol is monolithic with the transistor in the N layer. This input structure is referenced as a mirror circuit because when it is drawn in a symbolic representation (Figure 4(b)), it resembles a bipolar transistor and its mirror. Also, the relationship between the current I_M to I_{CCD} is proportional to the base-emitter junction areas of the two transistors because the base-emitter voltages are equal for both transistors. The common base lateral transistor and the mirror can be fabricated by employing double diffused techniques to obtain a very narrow base width (less than 1 μm). The base width will be smallest next to the virtual collector producing a condition where the current injected into the emitter will preferably enter the collector via the narrow base region. Bias on the first gate produces a virtual collector thereby achieving an input structure where the collector of the bipolar transistor is part of the CCD channel. Such a configuration results in a higher injection speed because the transport time of charge across the collector is eliminated by making the collector the CCD holding well. The gate adjacent to the virtual collector can be used as an injection gate or can be simply connected to one of the CCD shift register clocks with a two phase or one and a half phase clocking format. The amount of charge injected into the virtual collector's holding well depends on the value of the input current I_{IN} and integration (clock dwell) time. The input current is produced by applying a voltage via a resistor to the emitter mode. The injected current I_{IN} is then divided between the bipolar input transistor and its mirror.

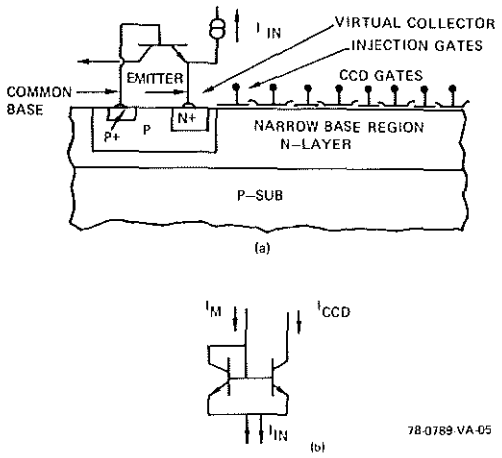

Figure 4. (a) Bipolar CCD Input Structure and (b) Circuit Diagram of Current Mirror
NOTE: The p-type base diffusion can contact the p-substrate without affecting the operation of the bipolar input structure

Experimental results on bipolar mirror structures show a precise current division according to the junction area over several decades of input current. Such a precise current division achieves two principal advantages: reduction of deleterious bandwidth effects by parasitic capacitance and reduction of the coupling difficulty between the CCD and an input signal.

Inherently, the CCD can accommodate only very low currents. Specifically, the current handling capability of a high speed CCD is in the 100-μA region. Generating such a low current level at high frequencies through low impedance lines is difficult and susceptible to induced noise currents by ac and dc offset voltages. Clearly, a higher level input voltage applied to the CCD's input structure should exhibit better noise immunity than low-level voltage signals. Moreover, reducing the input impedance of the CCD input structure yields a circuit less susceptible to bandwidth reduction by parasitic capacitances. Since the bipolar mirror input structure acts as a current transformer, a low input current into the CCD can be maintained while increasing the input current I_{IN} by applying a higher input voltage through a smaller series resistance, thereby achieving a wider input bandwidth. Typically, the base-emitter junction area can be made smaller than 100 μm by 4 μm while the mirror's junction area can be made 500 μm by 20 μm, resulting in a current attenuation of 16 to 1. The effect of the mirror transistor is to reduce the input impedance at the emitter mode and reduce the effect of parasitic capacitances.

The operating speed of a bipolar transistor is determined by three regions: emitter frequency response, base transit time, and collector transit time. The emitter frequency response represents the speed with which the emitter-base voltage can change to accommodate a changing input current signal. A simple expression for the emitter frequency response (f_e) is the input transconductance (g_m) divided by the total capacitance (C_T) at the emitter node multiplied by 2π, i.e., $f_c = g_m / 2\pi C_T$. The capacitance, C_T, is the sum of the emitter-base junction capacitance of the bipolar input transistor (C_B) and its mirror (C_M), and parasitic capacitance C_p. Note that capacitance C_M and C_B are proportional to each other by the ratio of currents flowing respectively through the mirror transistor and the bipolar input transistor by the emitter-base junction areas. Without loss of generality assume a proportionality constant determined by the ratio of the junction area to be 25. Hence, the CCD input current I_{CCD} will be 25 times smaller than the mirror current I_M. Substituting for g_m and C_T the following expression is obtained:

$$f_e = \frac{eI_{CCD}}{2\pi kTC_B}\left[\frac{1 + I_M/I_{CCD}}{\frac{C_p}{C_B} + \frac{C_M}{C_B} + 1}\right] = \frac{eI_{CCD}}{2\pi kT} X \qquad (26)$$

$$\left[\frac{1}{C_B + \frac{C_P}{26}}\right]$$

Clearly, the effect of the parasitic capacitance (C_p on the input bandwidth at the emitter node is reduced 26 fold, a number equal to the current division of the input signal by the bipolar input structure. Hence, for a 100 μA CCD input current, an emitter area of 100 μm by 4 μm, base doped with 10^{18} boron atoms/cm^3 and emitter concentration higher than 10^{20} arsenic atoms/cm^3, an emitter frequency response of $f_c = 2.8 \times 10^9$ Hz is obtained. The large frequency response is due primarily to a 26-fold reduction of the parasitic capacitance. If the parastic capacitance were not reduced, the emitter operating frequency response would be equal to 3.50×10^8 Hz. Therefore, the equivalent transit time for the emitter region is 3.60×10^{-10} sec. Using the diffusion equation, the transit time across the base, $t_B = 2\ W^2/2.43\ D_B$, for a 1 μm wide base (W) and 24 cm^2/sec for the diffusion

constant (D_B) is 3.5×10^{-10} seconds. Continuing the calculation for the transit time across a 5-μm virtual collector, $t_c = \pi L_c / V_s$, 2.6×10^{-10} sec are obtained as the minimum time required to transport electrons across the collector using a saturation velocity of 6×10^6 cm/sec for electrons. Summing all the transit times (emitter, base, and collector) a 1.03-GHz input frequency response for the bipolar mirror input circuit is calculated. Clearly, the input signal injection frequency is limited by the series input resistor and its shunting capacitor. With additional care, the 0.5 pF capacitor shunting the input resistor can be reduced, thereby achieving further improvements in the CCD injection bandwidth.

The calculations illustrated above have been refined using an ISPICE program, and the results are in good agreement with the above calculations.

4.0 High-Speed Nondestructive Readout (NDRO)

The accurate readout of analog charge packets from a high speed PCCD is a difficult problem. The usual output technique using a floating gate amplifier and a reset switch is found lacking because the output circuit bandwidth necessary for satisfactory operation is several times the signal bandwidth. This reflects the fact that several operations are required to reconstruct the input signal. Correspondingly, the noise associated with the wider band amplifier increases the noise contribution to the output signal. The nondestructive readout scheme presented in this paper is a novel approach for tapping a PCCD which overcomes the limitations inherent in conventional readout structures. The NDRO structure does not require a reset switch or several operations to reconstruct the input sample. Moreover, there is no floating readout diffusion which eliminates the $\sqrt{kTC}$ charge noise associated with setting and resetting the output diffusion.

The NDRO structure consists of a P-channel depletion - mode FET incorporated into the PCCD channel having its drain, channel, and source oriented transverse to the direction of charge flow (see Figure 5). Channel stops limit the width of the sensing P-channel FET and confine the signal in the CCD to flow under the charge sensing FET. Charge flowing in the PCCD channel passes under the sensing FET and modulates the FET's channel conductivity. Modulation is affected when the signal charge under the sensing FET decreases the depletion width at the P-N junction formed by the sensing FET and the N-type epi bias, thereby increasing the channel width (conductivity). Modulation of the sensing FET's conductivity by signal charge flowing in the PCCD channel is monotonic and does not consume the modulation signal charge packet. The modulating signal charge is transported under the sensing FET by clock pulses.

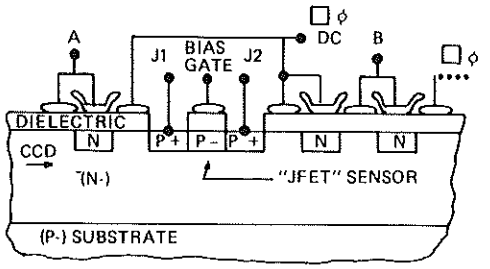

Figure 5. Nondestructive Readout Structure for High Speed PCCD's

Two types of gates are incorporated around the nondestructive readout FET. The adjacent gates are dc gates and are used to shield the sensing FET from the clock pulses applied to the PCCD clocking gates. These dc gates are also used to adjust the dc potential of the PCCD channel to facilitate charge transport to and from the region located below the sensing FET. The ac clocking gate preceding the R/O FET (A) pushes the signal charge under the sensing FET while the succeeding gate (B) blocks, thereby confining the charge under the R/O FET. The charge injected under the R/O FET modulates the channel's conductivity to form an output signal dependent on the analog value of the charge packet. Charge is removed from under the sensing FET when the blocking gate (B) is pulsed attractive and the preceding gate (A) is maintained in the blocking state. After the signal charge is removed, gate (B) is returned into the blocking state and gate (A) is opened to let the next analog packet of charge into the sensing well under the R/O FET. Injection and removal of the signal charge from the sensing well is achieved at high speed because the dc bias or the readout FET produces a drift field to move the charge from under gate (A) to under gate (B). Also, the fringing fields induced by the voltage applied to gates (A) and (B) augment the transport of charge into and out of the sensing well. No $\sqrt{kTC}$ noise is associated with this R/O technique for there is no capacitor to charge and discharge as in conventional R/O structures. With exception of bulk trapping centers, the charge transport into and out of the sensing well should be complete. The noise associated with the R/O FET can be reduced by increasing the quiescent current flowing in the channel, thereby increasing the transconductance and reducing the noise voltage and sensitivity of the R/O FET.

5.0 On-Chip Driver Circuits

High-speed bipolar drivers on the PCCD chip reduce clock line interconnect capacitance, and are similar to typical ECL circuits.

There are two primary objectives for any on-chip clock driver circuit as shown in Figure 6. The first is low power dissipation and the second is the needed switching speed when driving the specified capacitive load. The illustrated circuit is composed of a differential ECL input stage and a push-pull type driver stage. Typically there could be four such driver stages, each driving 25 percent of the gates of the two-phase CCD to reduce the loading on each individual stage. This reduces the transient current which each driver is required to handle. If the circuit is switching at 800 MHz, total transient current of 0.9 A are typical. Using four drivers reduces the current per stage to 225 mA. The differential input stage is operated at +4 and −5.2 volts, making it totally ECL compatible. Therefore, all logic is dc coupled straight through to the CCD gates. The switching current is 7 mA, for a total dc power dissipation of 128.8 mW in the differential stage. Low power is achieved in a push-pull stage by not having any paths to ground directly from a supply and thus eliminating quiescent operating power. When the stage is in positive slew, the lower transistors, Q5 and Q6, are turned off and the only power dissipated is the transient current through Q7. When the capacitor is fully charged, the power dissipation goes to zero in the drivers. In the negative slew condition, Q7 is immediately turned off by the IR drop across the resistor caused by the collector current of Q5. Therefore, Q6 sees only the discharging capacitor current, and when the load voltage goes to zero, the only power dissipated is that across the resistor R3.

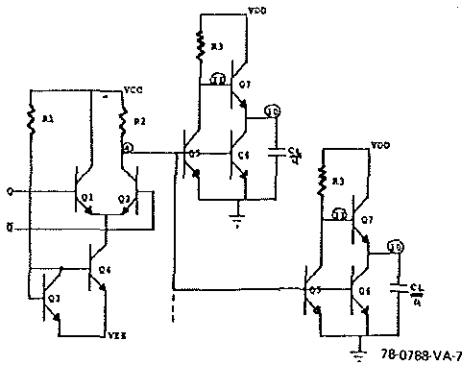

Figure 6. On-Chip CCD Drive Circuit

The high speed requirement is met by using a transistor to reduce the RC constant in the positive slew configuration, and a transistor to directly short the load to ground. This gives the lowest RC constants possible in both directions, to maximize speed. ISPICE simulation results (Figure 7) shows that the buffer is capable of operation in excess of 200 MHz.

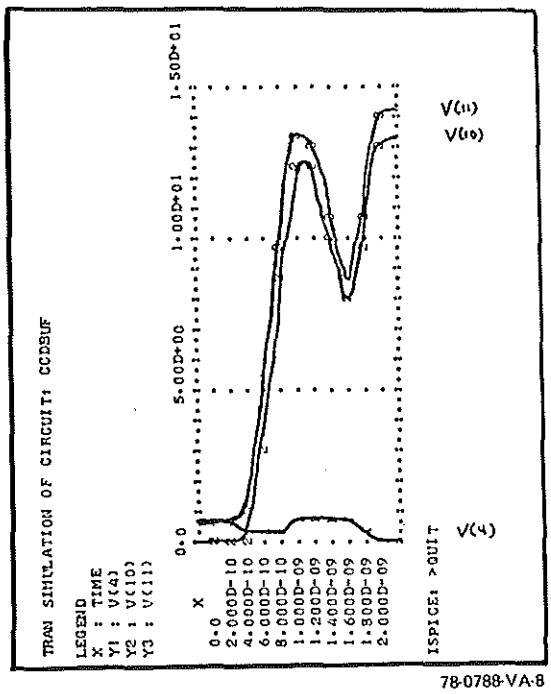

Figure 7. ISPICE Simulation of On-Chip CCD Drive Circuit

6.0 Conclusion

New CCD techniques for achieving high-speed injection, transfer, and readout have been presented and analyzed. The high-speed bipolar current-mirror injection scheme allows an exact metering of small currents into the transfer structure and improves coupling to off-chip circuits by acting as a low impedance source. Analysis is presented that show high-speed transfer can be achieved without the use of submicron lithography.

The use of deep ion-implantation structures rather than epitaxial structures is proposed for improved leakage current performance. A unique nondestructive readout scheme is proposed that is effectively reset by the CCD clock requiring no additional clock waveforms for signal reconstruction.

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