CHARACTERIZATION OF LEAKAGE CURRENT WITH PHOSPHORUS GETTERING IN CHARGE COUPLED DEVICES

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ABSTRACT. Gettering is a process designed to remove from a silicon wafer impurities and structural defects which can act as generation-recombination centers and so cause reduced lifetime and increased leakage. In an oxide-isolated double-polysilicon gate surface p-channel CCD process, gettering is performed at the same time that the polysilicon layer is doped with phosphorus. The gettering effectiveness of the phosphorus is dependent on the temperature of the phosphorus deposition to take advantage of the increased phosphorus solubility limit at higher temperatures. The phosphorus deposition temperature employed for the gettering comprised of 925, 975, and 1025°C. Also included were a group of control wafers with no phosphorus gettering.

The effectiveness of gettering was determined by performing leakage measurements on 128-bit CCD shift registers so that results obtained from more than 1,000 devices were found to be significant to a confidence level of greater than 99.9%. Also, leakage in CCD shift registers as a function of temperature and reverse substrate bias variations were also obtained.

Gettering experiment results produced three main conclusions: (a) gettering reduces average leakage on all wafers, (b) the wide variation of leakage generation of ungettered wafers is dramatically reduced, and (c) gettering at higher temperatures leads to lower leakage and narrower distribution of leakage.

INTRODUCTION

A critical parameter affecting the yield of large scale charge coupled devices for memory and imaging arrays is the leakage current density associated with each cell of the array[1]. Leakage current generation produces erroneous data in CCD memories by generating a ONE instead of a ZERO in the data pattern. In CCD imaging applications, leakage current manifests itself by blooming and streaking in the video output signal [2].

Leakage current generation is dominated by oxidation-induced and bulk stacking faults where heavy metals precipitate [3],[4]. Several techniques for reducing these stacking faults have been investigated [2],[5],[6]. One of the easiest to implement is the technique of phosphorus gettering[2]. Consequently, fabrication procedures were developed to minimize leakage current generation by optimizing the phosphorus gettering process.

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PHOSPHORUS GETTERING

Gettering is a process designed to remove from a silicon wafer impurities and structural defects which can act as generation-recombination centers and so cause reduced lifetime and increased leakage[6]. Heavy metal ions are known to precipitate in the vacancy structure associated with dislocations, stacking faults, and other material imperfections. These heavy metal ions are nearly all interstitial diffusers, and so, if a sink for them can be formed on the back of the wafer, they can be effectively removed from the active surface of the wafer during reasonably short diffusion times. One way of doing this is to diffuse phosphorus into the back of the wafer[5], leaving a layer of silicon oxide heavily doped with phosphorus on the back. Such a glass layer is molten at moderate temperatures and becomes a sink for the metal ions. A heat treatment at the temperature at which this glass is molten can, therefore, getter impurities. It is also shown that gettering occurs in a region of strain on the back of the wafer[6] because the very high concentration of vacancies in the strained region provides a concentration gradient of impurities away from the active surface. Because high phosphorus concentrations cause high strain in the silicon lattice, phosphorus gettering may be effective by both mechanisms under favorable circumstances.

In an oxide-isolated CCD double-polysilicon gate surface p-channel process, phosphorus gettering can be formed at the same time that the second polysilicon layer is doped with phosphorus. Thus, gettering is done as late as possible in the process; i.e., during the last high temperature step. The oxide is stripped from the back of the wafers so that this phosphorus is diffused into the wafers from the back as well as into the polysilicon on the front. This causes both strain and a phosphorus-glass layer on the back of the wafer. This glass layer maintains the high concentration of phosphorus in the back of the wafer during subsequent heat treatments.

A layer of silox is deposited on the backside phosphorus glass to prevent its removal during subsequent etching steps. By retaining the phosphorus glass on the wafer back, the phosphorus concentration will be maintained at (or close to) its solubility limit at the surface in spite of subsequent diffusions. It is expected that the considerable lattice strain produced by phosphorus in the back of the wafer will provide a high concentration of vacancies which may act as a sink for interstitially-diffusing metallic impurities known to give rise to recombination-generation centers in silicon. Such impurities, then, may be "gettered" from the front of a wafer, where the active device regions are located, and immobilized in the back.

The gettering effectiveness of phosphorus is expected to be dependent on the density of vacancies in the wafer back. More strain, and, therefore, (presumably) more vacancies, can be produced by increasing the phosphorus concentration in the wafer. This is most conventiently done by increasing the phosphorus deposition temperature to take advantage of the increased phosphorus solu-

bility limit at higher temperatures (at least in the temperature range under consideration).

EXPERIMENTAL INVESTIGATION OF PHOSPHORUS GETTERING

An experiment was designed to investigate and optimize phosphorus gettering procedures. The main parameter available for changing either the strain in the wafer or the phosphorus density is the temperature at which phosphorus gettering is performed. Because temperature controls the solid solubility of the phosphorus in the silicon, it, therefore, controls its concentration in the wafer. Accordingly, the phosphorus gettering process incorporates four variations: Control wafers (no phosphorus gettering) and gettering with phosphorus deposition temperatures of 925, 975 and 1025°C. Each group consisted of six wafers.

FABRICATION TECHNIQUE

A summary of the oxide-isolated double polysilicon processing sequence is as follows:

a. Starting silicon substrate <100>, 3 ohm-cm, n-type Czochralski.

b. Si_3N_4 deposition, delineation, field implant.

c. Local field oxidation

d. Gate oxidation

e. Polysilicon deposition and delineation.

f. Threshold shift implant

g. Second gate oxidation

h. Polysilicon deposition and delineation.

i. Contact mark and etch

j. Aluminum metallization, mark, and etch.

h. Anneal

A cross-section of the device is depicted in Fig. 1.

TEST PROCEDURES

The effectiveness of gettering was determined by making measurements on a 2-phase 128-bit CCD shift register. The clock frequency was found at which an empty bucket would become one-third full during the total time it was being clocked through the register. This clock frequency is a direct measure of the average rate, r, of charge generation in the register, since $r=Q/t_d$, where Q is that charge required to fill one-third of a bucket and t_d is the delay time through the register. Since $t_d=n/f$, where n is the number of bits and f is the clock frequency, then $r \propto f$. Note that this technique does not distinguish between high background generation rates, and low background with localized highly-generating point defects, but rather provides an overall average leakage density. The leakage current density, J_L, is related to the clock frequency, f_L, at which the bucket becomes one-third full by

$$J_L = \frac{C_{out} V_{out}}{A_{BIT} A_V \left(\frac{1}{f_L} - \frac{1}{f_H}\right) n} . \qquad (1)$$

where C_{out} is the total capacitance at the output floating diffusion node, A_V is the gain of the source follower, A_{BIT} is the area where charge generation exists, n is the number of bits in the shift register, f_H is the high clock frequency of CCD operation, and V_{out} is the increase in output voltage due to charge generation at frequency f_L.

A different test procedure[1] is employed to separate leakage spikes and back-

ground leakage density. The clocks are stopped or held for a period of time Δt. In this manner, charge is collected during the time Δt and then clocked out of the shift register. Clocking the data out serially provides an output signal proportional to the leakage current at the appropriate cell locations. Thus, non-uniformity and spike leakage current density are obtained. In this case, the leakage current density is given by

$$J_L' = \frac{C_{out} V_{out}}{A_{BIT} A_V \Delta t} \qquad (2)$$

where Δt is the shift register holding time. The above methods were examined and result in excellent agreement. The former method has the advantage of providing fast discernable data without excess data reduction and was used throughout the data gathering process. As noted before, each group comprised six wafers, providing a total of 1072 CCD shift registers for subsequent evaluation. Results are statistically significant to a confidence greater than 99.9%.

RESULTS

Experimental results are summarized in two histograms given in Fig. 2. Fig. 2(a) shows results from 17 wafers which were gettered and includes 640 measurements on individual registers. The histogram of Fig. 2(b) shows results from six non-gettered wafers, including measurements on 432 registers. Note that one block on the histogram is 1 KHz wide. There are no values above 5 KHz from the gettered wafers, but about 27% of the distribution for the controls is above 5 KHz. The primary conclusion is that, of the two groups, the gettered wafers have significantly less leakage. The distribution in Fig. 2(b), however, is strongly bimodal because the six ungettered wafers themselves fall into two quite distinct groups.

Fig. 3 shows two histograms: Fig. 3(a) for wafers #24, 25, and 26, and 3(b) for wafers #27, 28, and 29. Each block is 10 KHz wide. Note that the results in Fig. 3(a) are wholly contained in the 0-10 KHz block, but that 48% of the results in 3(b) lie above 10 KHz. Figs. 4 and 5 contain the same data as in Fig. 3, but are replotted with expanded abscissa scales so that the detail of these distributions may be seen.

If Figs. 2(a) and 4(a) are compared, it is seen that the "good" ungettered wafers #24, 25, and 26 are not much worse than the total gettered wafer population. However, the difference between the mean of the "good" ungettered wafers of 0.76 KHz and that of the gettered wafers of 0.46 KHz is statistically significant to a confidence level greater than 99.9%.

The question arises, would the three "bad" ungettered wafers, #27, 28, and 29 have improved if they had been gettered? Fig. 6 shows separate histograms of these three wafers. It is seen that these wafers have different characteristics, and, in particular, wafer #28 is closer to the group of "good" ungettered wafers than it is to the other two wafers in the "bad" group. It is at least arguable that wafers in the large batch from which those for this experiment were selected are extremely variable in the sense of their leakage

characteristics after processing, as evidenced by the six ungettered wafers. It is unlikely that wafers #26, 27, and 29 were the only ones out of the sample size of 24 that were bad (based on the criterion of this experiment). With no bad wafers occurring in the group of seventeen which were gettered, we may plausibly conclude that gettering can effectively reduce the very high leakage resulting from the wafers which fall into the "bad" classification.

Fig. 7 shows histograms of the three experimental groups of gettered wafers, i.e., those gettered at 925, 975, and 1025°C. The mean frequencies for these groups are 0.48, 0.50, and 0.38 KHz, respectively. There is no difference between the results at the temperatures of 925 and 975°C, but the difference between the results at these temperatures and those at 1025°C is statistically significant to a confidence level greater than 99.9%.

The effect of gettering at the various temperatures may be seen by listing the means of the frequencies for each wafer in their appropriate groups. This is done in Table 1, where wafers are listed in order of increasing mean value.

A summary of the above results is presented in Fig. 8, where leakage current density is plotted for each gettering group. The control wafers are shown to have two distinct categories: One having an average leakage current density of about 28 nA/cm^2 and the other 266 nA/cm^2. The group gettered at 925°C has four wafers with an average of about 16 nA/cm^2 and one wafer out of proportion. A similar case exists for 975°C gettering. The 1025°C gettered wafers, however, have an overall tight distribution with an average of 12 nA/cm^2.

TEMPERATURE AND REVERSE SUBSTRATE BIAS CHARACTERIZATION OF CCD LEAKAGE CURRENTS

The leakage current of the 128-bit CCD structures were characterized as a function of temperature and reverse substrate bias. In the investigation, spike leakage was also included to determine its variation with temperature and reverse substrate bias. In order to distinguish between background and spike leakage, the technique described earlier, employing clock disabling for a time Δt, was used.

Results are shown in Fig. 9. Normal operating conditions employ a +5 volt reverse substrate bias, V_{SS}. When V_{SS} is increased to +12 volts, both spike and background leakage increase by a factor of about 2.3. The depletion layer increases by a factor of 1.2, thereby contributing to the bulk leakage term. This implies that the remainder of the leakage is probably surface generated. This is demonstrated by temperature characterization of the devices. Measurement of leakage current versus temperature indicated that as temperature is increased to 65°C, the slopes for several values of V_{SS} are relatively constant, indicating that spike and background leakage both increase at approximately the same rate (viz., doubling every 10 degrees). In this temperature range, the leakage generation rate is dominated by an activation energy of 0.59 eV and is probably due to surface induced leakage[7].

CONCLUSIONS

The experimental evaluation of phosphorus gettering has produced the following results:

(i) Gettering reduced the average leakage for all wafers.

(ii) The wide spread of leakage generation in ungettered wafers is dramatically reduced.

(iii) Gettering at higher temperatures leads to lower leakage and a tighter distribution of leakage.

Temperature characterization has shown that spike and background leakage increase with temperature at the same rate and, thus, have the same activation energy of about 0.59 eV. The substrate bias characterization has shown that both bulk and surface leakage generation occur and that the latter is dominant.

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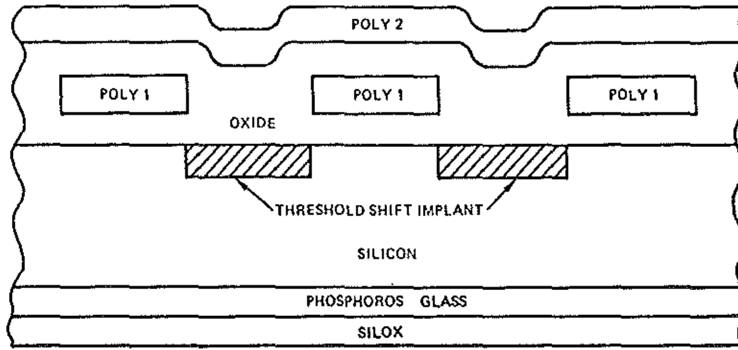

Figure 1. Cross-section of CCD After Phosphorus Gettering

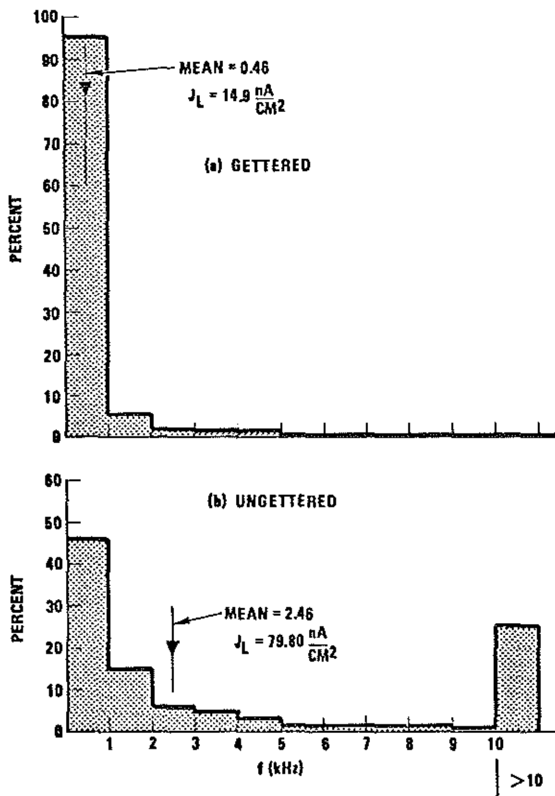

Figure 2. Histograms of Gettered and Ungettered Wafers

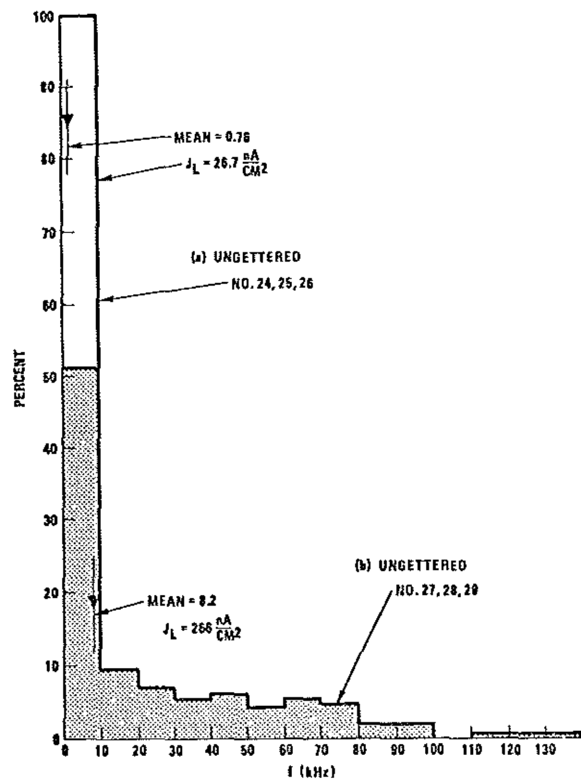

Figure 3. Histogram of Ungettered Wafers

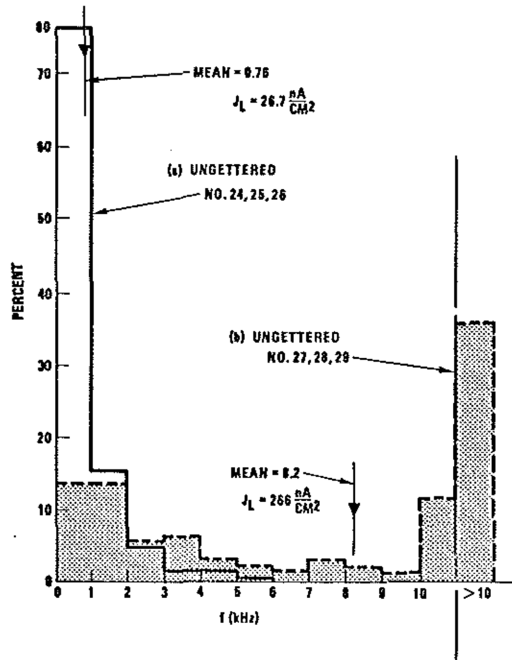

Figure 4. Histogram of Ungettered Wafers with Expanded Abscissa Scales

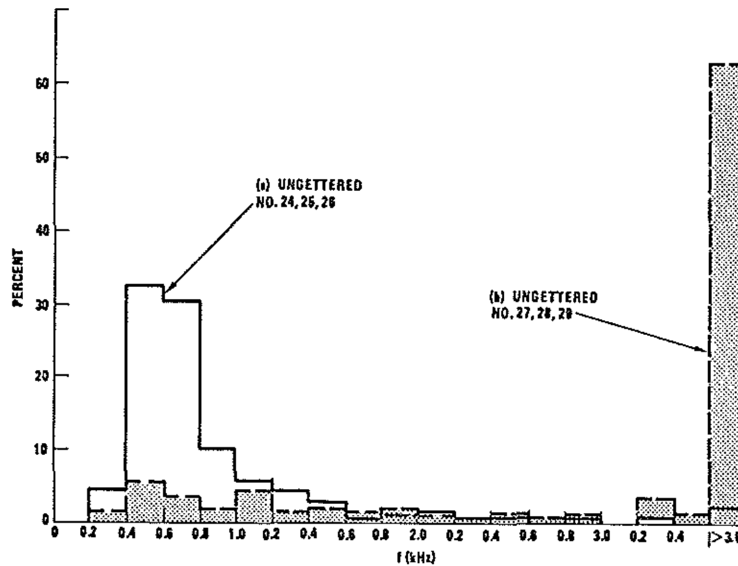

Figure 5. Histogram of Ungettered Wafers Depicting Bimodal Quality

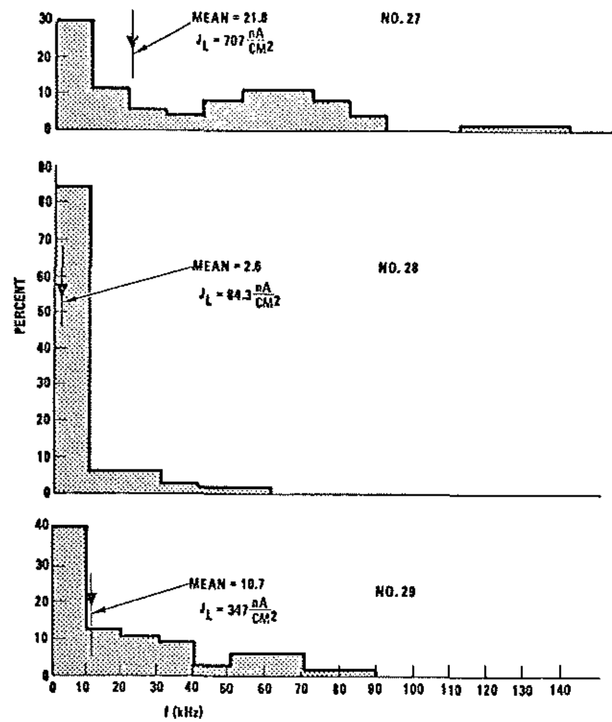

Figure 6. Histogram of "Bad" Ungettered Wafers

TABLE 1. WAFER AND OVERALL LEAKAGE CURRENT DENSITY MEANS

	NOT GETTERED	925°C	975°C	1025°C
WAFER MEANS (KHz)	.72 .75 .80 2.63 10.74 21.80	.33 .39 .52 .52 .52 1.00	.36 .36 .46 .52 .81 -	.25 .36 .39 .44 .50 .51
OVERALL MEANS (KHz)	2.46	.48	.50	.38
J_L (nA/cm^2)	79.80	15.60	16.20	12.30
R	30.30	3.00	2.30	2.00

R is the ratio of the highest mean in a group to the lowest mean.

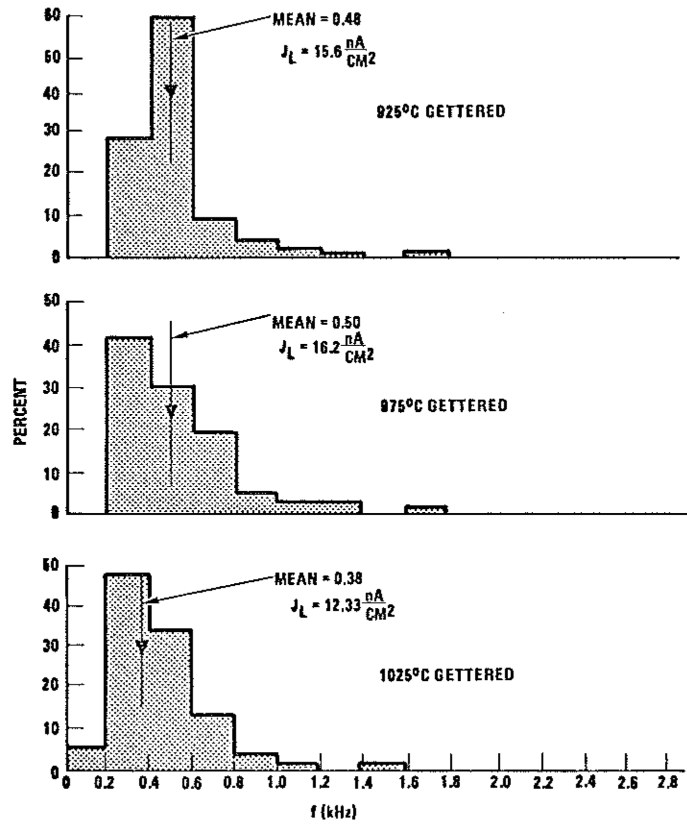

Figure 7. Histograms of Gettered Wafers at Various Temperatures

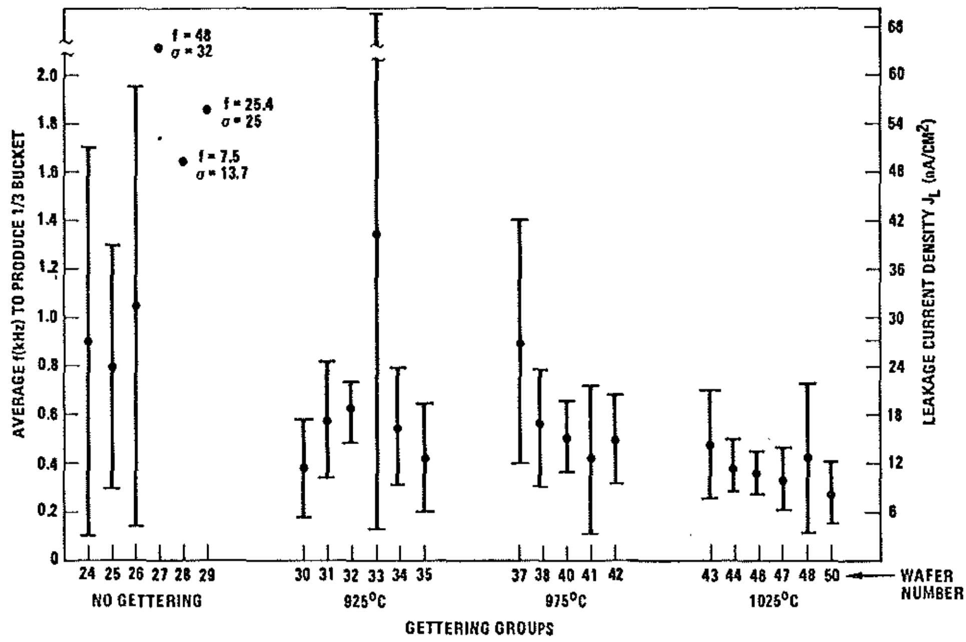

Figure 8. Leakage Current Density as a Function of Phosphorus Gettering Groups

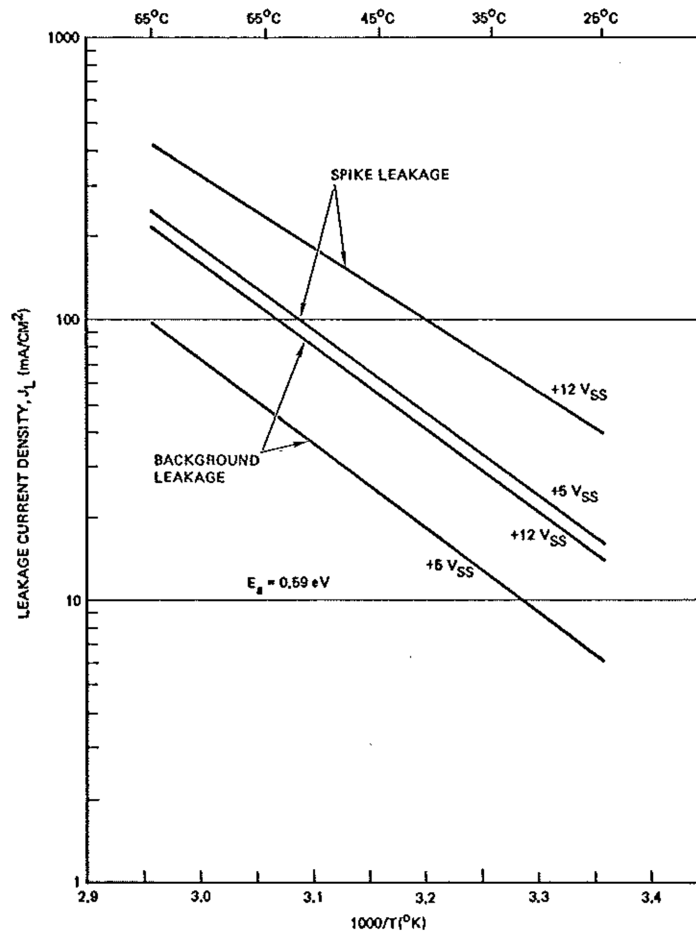

Figure 9. Leakage Current Density Versus Operating Temperature