DEGRADATION ANALYSIS OF CCD'S*

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ABSTRACT

The effort reported in this paper concerns an experimental study of factors which influence the degradation of parameters and performance of analog charge-coupled devices. Measured parameters include charge transfer efficiency, dark current density, analog dynamic range, and full well capacity. Test cells of a p-surface channel device and an n-buried channel device were temperature-bias stressed for 1,000 hours with parametric measurements taken at time 0, 168, 500, and 1,000 hours. A total of 40 surface channel devices and 21 buried channel devices were tested. Dynamic and dc stresses were applied to separate test cells at temperatures of 125°C and 200°C. Results show an increase in dark current density for all SCCD's test categories and a decrease of transfer efficiency for both SCCD's and BCCD's under 200°C stress for 1,000 hours.

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1.0 Introduction

The growing use of charge-coupled devices (CCD's) in systems for analog signal processing has generated a need to develop information on failure mechanisms that affect CCD structures. This paper reports the results of a temperature bias stress accelerated life testing experimental study aimed at revealing these failure mechanisms. Groups of 44-stage surface p-channel analog shift register CCD's (SCCD) and 455/910-stage bulk n-channel analog shift register CCD's (BCCD) were subjected to dc and dynamic electrical stress at 125°C and 200°C. The 44-stage devices were unscreened Westinghouse 7004 serial in-/serial out four-phase shift registers while the 455/910-stage devices were commercially available Fairchild CCD-321 serial in/serial out shift registers. Cross sections of these two devices detailing their structure are shown in figures 1 and 2.[1] The sample group sizes consisted of 10 devices each for the SCCD's and 7 devices each for the BCCD's. However, each BCCD had two separate 455-bit analog shift registers on a single chip and, therefore, provided data on two separate shift registers per device package. Electrical measurements were taken at time 0, 24, 168, 500, and 1,000 hours of stress time. An additional 500 hours of stress was applied to the 125°C dc n-channel BCCD test group for a total time of 1,500 hours under stress. Electrical measurements of the devices were made at room temperature with the precaution taken that devices were cooled to room temperature before electrical stress was removed. The experimental approach is summarized in figure 3.

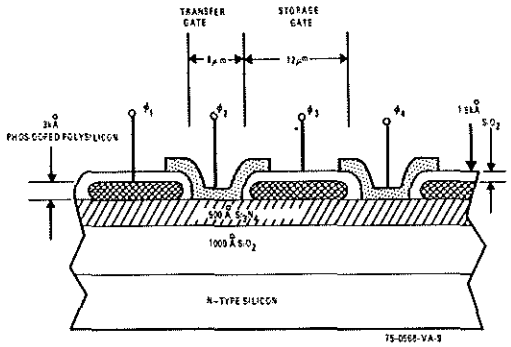

Figure 1. Cross Section of Aluminum/Poly Silicon Four Phase, Coplanar Electrode Configuration

2.0 Description

The dynamic stress consisted of the normally specified operating waveforms and bias voltage levels. The dc stress for the SCCD devices was −20 volts applied to the transfer gates with respect to the substrate with the input and output diodes back biased at the same voltage. In the case of the BCCD devices, the connec-

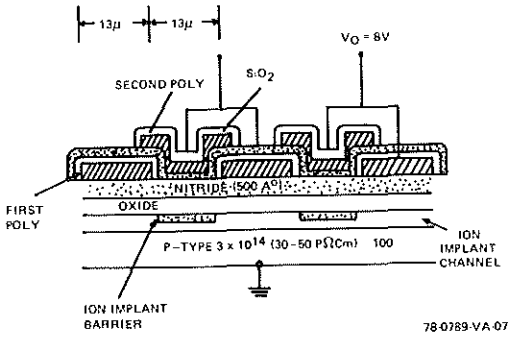

Figure 2. Cross Section of CCD-321 Structure

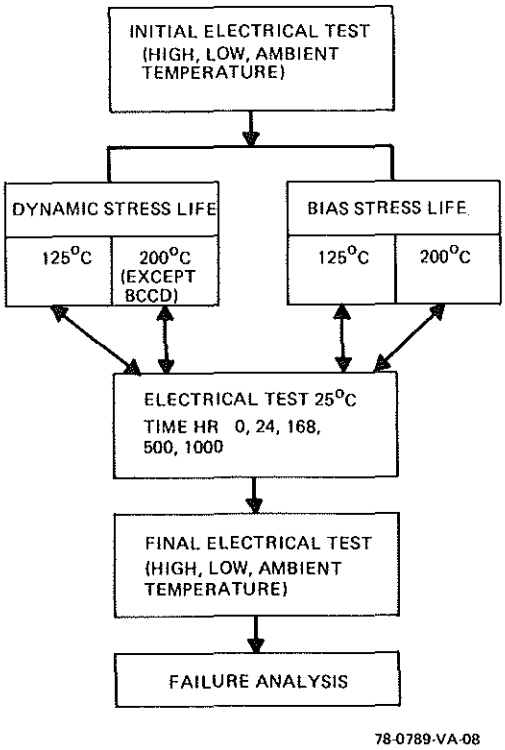

Figure 3. Life Test Plan for CCD Devices

tions were similar except that the initial positive dc stress applied to the transfer gates was 6 volts for the first 500 hours and then increased to 20 volts for the remaining 1,000 hours. Some of the electrical parameters measured were:

- Input Transfer Characteristics
- Full Well Capacity
- Dark Current
- Transfer Efficiency
- Insertion Loss
- Dynamic Signal Range
- g_m of Output Electrometer (SCCD's only).

Full well capacity is the maximum amount of signal charge which can be handled by a charge-coupled device. It was measured by the maximum output voltage difference between empty charge packets (when charge injection was cut off) and the largest charge packets the CCD can transfer when the output was saturated.

Dark current is the accumulation of additional carriers in potential wells from generation recombination centers found both in the bulk and at the silicon-silicon dioxide interface. The three major sources of dark current are thermal generation at the SiO_2 -Si interface, thermal generation in the depleted bulk, and thermal generation in the nondepleted bulk within a diffusion length of the depletion region. This latter source is small compared to the former sources. The dark current density (or leakage current) can be expressed as:[2]

$$= (1/2)\pi kTqN_i V_{th}\sigma_S N_{ss} + (1/2)qN_i\sigma_D V_{th}X_d N_t \quad (1)$$

where σ_S and σ_D are the capture cross section of surface and bulk traps respectively, N_{SS} and N_t are the surface and bulk trap densities, x_d is the depletion width and V_{th} is the thermal velocity of carriers. Surface trapping states are distributed uniformly across the band gap and distributed in emission time constants. Bulk trapping states which contribute to dark current are discrete and located within ± 0.1 eV of the middle of the band gap.[3] The dark current degrades stored information with increasing time causing a nonuniform noise distribution in system applications in which the CCD clocks are not operating continuously or for signals which take different paths through the device to the output. In the case of continuous clocking, increased dark current reduces dynamic range. For the SCCD devices, the dark current density was determined by measuring the difference in reset current flowing to the charge collection diode with the shift register running in the forward direction and reverse direction, with no charge injected by the input structure. Using this procedure, all charge collected in the potential wells is due to dark current. In the forward direction, the dark current is delivered to the collection diode, while in the reverse direction it is swept away from the collection diode and therefore, only the output amplifier noise is present. The difference between forward and reverse

clocking is the dark current. The BCCD device was not amenable to this measurement technique because charge transfer directivity is built into the structure during fabrication. The dark current measurement was made for the BCCD by first stopping the clock with one phase high for a period of time to collect leakage charge. After a suitable integration period the charge packets were then clocked at high speed to the output. The output waveform contained the signal voltage both with and without the leakage current integration. The voltage difference (ΔV) between the signal voltage, with and without integration, was due to the dark current. For readout times negligible to integration time (>10:1) the dark current is related to the voltage difference by:

$$J_D = \frac{C_{out}\Delta V}{t\,A_{SF}} \qquad (2)$$

where C_{out} is the total CCD output load capacitance, A_{SF} is the source follower voltage gain, and t is the integration time.

Charge transfer efficiency (or its complement, charge transfer inefficiency) is an important measure of device performance for analog signal processing. Transfer inefficiency is due to the trapping of charge at either the SiO_2 -Si interface or within the depleted bulk and/or insufficient transfer time. As clock frequency is increased, a break point is reached after which transfer inefficiency increases sharply because the time available for free charge transfer is reduced to the decay time constant associated with the longitudinal electric fringe field. The physical parameter which may change under stress which influences the decay time constant is the mobility of the carriers. A degradation in charge transfer efficiency in the clock frequency region in which free charge transfer effects do not dominate can result from the introduction of defects in the silicon, an increase in fixed charge loss and/or a change in the fixed charge density within the oxide. The first mechanism is manifested by an increase in interface or bulk trap density and/or a decrease in minority carrier mobility. The last mechanism is manifested by the trapping of electrons or holes in the oxide near the oxide-nitride interface necessitating a change in operating voltages for optimum performance. (This situation is undesirably from a user's viewpoint.) The effect of charge transfer inefficiency on the transfer function characteristics of serial in/serial out analog sampled data CCD's is given by the expression:

$$\frac{A_{out}}{A_{in}} = \left(\frac{g_m R_s}{1+g_m R_s}\right)\left(\frac{C_m}{C_{out}}\right)\left(\frac{n^2}{1+\epsilon^2-2\epsilon\cos(2\pi f/f_c)}\right)^{N/2} k\,\mathrm{sinc}\,k;\ k<1 \qquad (3)$$

where g_m is the transconductance of the output electrometer, R_s is the output electrometer source resistance, C_{in} is the effective input capacitance, and C_{out} is the output capacitance of the reversed biased readout diffusion. The term η is the charge transfer efficiency while ϵ is the charge transfer inefficiency defined as $\epsilon = (1-\eta)$. The term f is the input signal frequency, f_c is the clock frequency, N is the total number of transfers, and k is the ratio of signal output aperture time to clock period. The insertion loss, in dB, is then given by the ubiquitous relationship:

$$dB = 20\log\left(\frac{A_{out}}{A_{in}}\right) \qquad (4)$$

for a specified input frequency, clock frequency and value of k. Insertion loss was measured experimentally using a spectrum analyzer. The expression used to calculate transfer efficiency from the experimental data is:[4]

$$\eta = (1-\epsilon) = 1 - \frac{L_L}{N-1+L_L} \qquad (5)$$

where L_L is the total loss in the leading edge of a string of pulses. This expression yields a value of transfer efficiency per transfer. The usual pulse measurement technique was used for all tests to obtain the data for transfer efficiency calculations.

Dynamic range was measured as the difference, in dB, between the fundamental tone output of the CCD and its second harmonic when the second harmonic power equaled the rms noise power output of the device. The measurements were made using a spectrum analyzer. The spectral content of the noise was predominantly white with little contribution to total noise power due to 1/f noise for both groups of CCD's tested.

All measurements presented in the tables were made at a clock frequency of one MHz. A frequency of 0.225 MHz was used for the test signal while making insertion loss and dynamic range measurements.

3.0 Experimental Results and Discussion

A summary of the test data is presented in tables 1 through 6 and figures 4 through 7. Each data value in

the tables represents the mean and standard deviation of 10 measurements (10 devices) per category for the SCCD's and 14 measurements (7 devices) per category for the BCCD's. The g_m of the output transistor for the SCCD's was measured initially and at the end of stress testing, and was essentially unchanged. The output amplifier of the BCCD was not available for separate measurement of its g_m. Referring to table 1,

Table 1
Full Well Voltage Variation Over 1,000 Hours of Stress (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Full Well Voltage			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.66	0.14	0.58	0.08
SCCD P-Channel	dynamic	125°C	0.59	0.09	0.61	0.11
SCCD P-Channel	dc	200°C	0.57	0.11	0.57	0.11
SCCD P-Channel	dynamic	200°C	0.58	0.11	0.59	0.08
BCCD N-Channel	dc	125°C	1.83	0.13	1.84	0.13
BCCD N-Channel	dynamic	125°C	1.78	0.14	1.78	0.14
BCCD N-Channel	dc	200°C	1.75	0.14	1.94	0.13

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no significant change in full well capacity was observed for either the SCCD's or the BCCD's under stress testing except the BCCD 200°C dc test group showed an increase in capacity of 11 percent. Tables 2 and 3

Table 2
Dark Current Variation Over 1,000 Hours of Stress Testing (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Dark Current nA/Square Cm			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	118/31*	234/11*	80	40
SCCD P-Channel	dynamic	125°C	39	9	1825/134*	2693/138**
SCCD P-Channel	dc	200°C	55	45	122	94
SCCD P-Channel	dynamic	200°C	44	35	204	121
BCCD N-Channel	dc	125°C	37	25	44	32
BCCD N-Channel	dynamic	125°C	73	64	67	61
BCCD N-Channel	dc	200°C	34	16	47	20

*Data with all sample values/data with two of ten samples deleted.
**Data with all sample values/data with three of ten samples deleted.

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give the test data results for dark current and transfer efficiency for the various stress categories. The data shows a uniform trend towards increased dark current with temperature stress for all SCCD test categories. A constant ratio difference of the initial and final measurements between the dynamic and dc stress SCCD categories can also be determined from the data with the dynamic category always the larger. A possible explanation is that for the dc stressed devices the entire voltage drop occurred across the gate oxide because the surface was inverted. On the other hand, the devices stressed with dynamic voltages had a depleted region at the silicon surface over which some voltage drop occurred. An increase in leakage current of MOS devices has been shown to be caused by an increase in fast interface state density and fixed positive charge when stressed with temperature and dc bias.[5] A change in interface state density would also manifest itself as a decrease in charge transfer efficiency. Although a marked decrease in CTE was observed for the 200°C SCCD test categories, a similar decrease was not observed for the 125°C SCCD test categories although their leakage current did change appreciably. Table 6 shows the data representing the CCD input gate "threshold" voltage for the SCCD test categories. (This measurement is not analogous to the usual threshold measurement of MOSFET's but does give some information on fixed charge in the oxide.) The data shows a larger degradation for dynamic stressed devices than for dc stressed devices. In an attempt to separate degradation effects due to changes in carrier mobility and interface state density, the transfer inefficiency was measured as a function of clock frequency for pulse waveforms with 10 percent bias charge and then as a function of time between pulses without bias charge (the so-called double pulse technique).[6] The results of the first measurements are shown in figure 4 for selected SCCD's. The characteristic break point occurs at roughly the same clock frequency for all categories implying that minority carrier mobility does not change radically.

The results of the double pulse experiment for selected SCCD's are shown in figure 5. Comparison of these graphs for the 200°C and 125°C categories show a change in slope on the order of ~ 2 which represents a factor of two increase in interface state density. Comparison of the initial and final transfer efficiency for the 125°C and 200°C test categories show that this factor of two increase in interface state density reasonably explains the difference in values. Although the factor of two also causes a proportional increase in leakage current which is reasonably consistent with the 125°C and 200°C dc SCCD stress results, the factor of approximately four change for the leakage current in the 125°C and 200°C dynamic SCCD stress categories cannot be readily explained by the data shown in figure 5. The data in tables 3 and 4 show that neither the dynamic range nor the insertion loss changed dramatically for any of the SCCD test categories. Although the CTE did change substantially for 200°C stressed SCCD's, the devices are only 44 stages which is to short to impact insertion loss and dynamic range.

Table 3

Transfer Efficiency Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Transfer Efficiency per Transfer							
			Initial				Final			
			0% F.Z.		10% F.Z.		0% F.Z.		10% F.Z.	
			Mean	S.D.	Mean	S.D.	Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.9986	0.0005	0.9994	0.0003	0.9983	0.0005	0.9994	0.0003
SCCD P-Channel	dynamic	125°C	0.9990	0.0005	0.9995	0.0006	0.9979	0.0010	0.9993*	0.0003*
SCCD P-Channel	dc	200°C	0.9984	0.0007	0.9994	0.0005	0.9966	0.0018	0.9984	0.0011
SCCD P-Channel	dynamic	200°C	0.9990	0.0003	0.9997	0.0001	0.9970	0.0014	0.9982	0.0013
BCCD N-Channel	dc	125°C	0.9990	0.0002	0.9999	0.0000	0.9987	0.0002	0.9999	0.0001
BCCD N-Channel	dynamic	125°C	0.9991	0.0002	0.9999	0.0000	0.9989	0.0001	0.9999	0.0000
BCCD N-Channel	dc	200°C	0.9991	0.0002	0.9999	0.0000	0.9953	0.0006	0.9968	0.0004

*Data with three of ten samples deleted

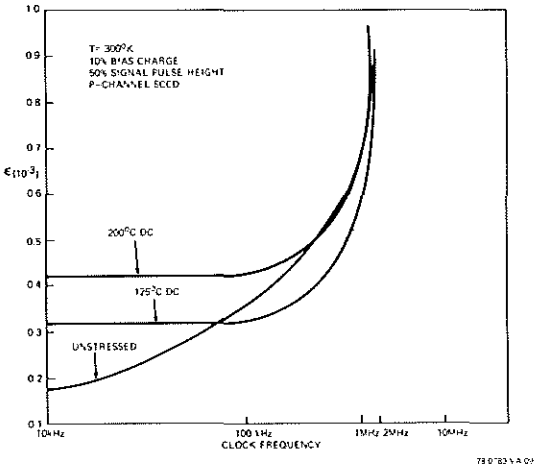

Figure 4. Surface Channel CCD Transfer Inefficiency as a Function of Clock Rate

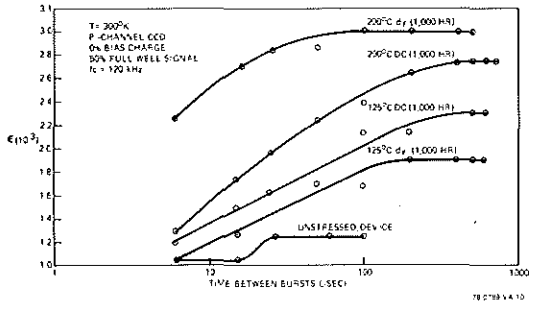

Figure 5. Double Pulse Measurements for Stressed and Unstressed SCCD's

Device Type	Voltage Stress	Stress Temperature	Insertion Loss dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	-25.9	1.3	-29.0	1.4
SCCD P-Channel	dynamic	125°C	-26.1	2.1	-25.7	1.4
SCCD P-Channel	dc	200°C	-26.1	1.7	-26.4	1.8
SCCD P-Channel	dynamic	200°C	-25.6	1.1	-26.8	3.0
BCCD N-Channel	dc	125°C	-13.7	0.5	-11.6	1.0
BCCD N-Channel	dynamic	125°C	-13.6	0.5	-12.1	1.2
BCCD N-Channel	dc	200°C	-13.7	0.5	-31.2	5.0

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Table 4

Insertion Loss Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

The experimental results for the BCCD do not lend themselves to easy physical interpretation. Although the device is a buried channel CCD, the data given in table 3 shows a marked improvement in transfer efficiency with the addition of a bias charge. The devices use an n+ floating diffusion for making several corner turns in the shift register. This corner turn technique has been modified by the manufacturer in later generations of the device type with the reported result that excellent transfer efficiency is achieved without bias charge.[7] Unlike the SCCD, there is no consistent increase in leakage current for the BCCD stressed devices. However, a substantial degradation in transfer efficiency occurred in the 200°C group. This loss in transfer efficiency could not be compensated by an increase in bias charge or by increasing or decreasing the clock voltages. Transfer efficiency measurements made as a function of frequency are shown in figure 6 for an unstressed device and the mean of all 200°C stressed devices. Differences are clearly apparent between the two 455-bit shift registers on the same device for the 200-degree dc results as well as a general shift of the break point toward lower fre-

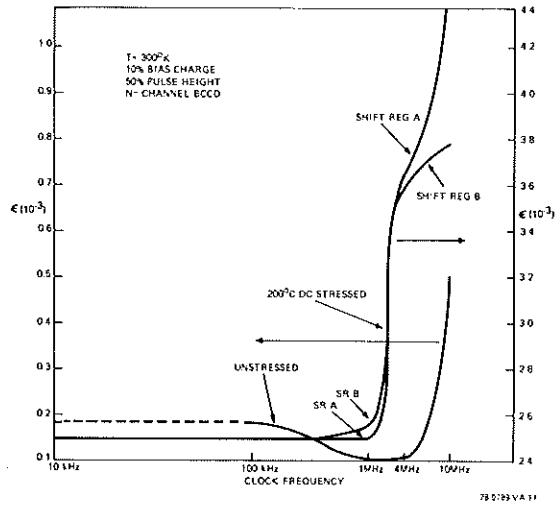

Figure 6. Transfer Efficiency versus Clock Frequency for BCCD's

quencies. The double pulse results for a single 200°C dc stressed device and an unstressed device are presented in figure 7. The shape of the curves for the unstressed device is consistent with measurements made by others of BCCD's[8 9 10] implying a single level of mid-gap electron trap states. However, the 200°C dc stressed curve is essentially different showing a peculiar twist at ~800 μsec which may be caused by multiple trap levels. Such traps, if not near the middle of the band gap, would not contribute to dark current but would contribute to a decreased CTE. Because of the poor transfer efficiency of the device, it was not possible to make meaningful measurements below 20 μsec at room temperature. Therefore, it has not been determined if the 200°C dc curve melds into the unstressed curve as the time between bursts goes to zero. If they do meld together, the observed loss in CTE for the 200°C category is due to other fixed charge losses than to bulk traps. Such other charge loss can be due to changes in the potential profile and/or loss out of the channel. The degradation in insertion loss and dynamic range for sinusoidal signals shown by the data in tables 4 and 5 for the 200°C dc BCCD stress category is consistent with the decreased transfer efficiency of these devices.

An Arrhenius relationship can be used to relate stressed measurements to degradation rate at room temperature. Assuming a thermal activation energy of 1 eV (a reasonable choice for silicon MOS devices) and screening devices that succumb to infant mortality, room temperature devices would degrade to the final values measured at 125°C after 8.54×10^4 hours and to the final values measured at 200°C after 5.13×10^6 hours.

Table 5
Dynamic Range Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Dynamic Range dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	43.0	1.3	40.2	1.7
SCCD P-Channel	dynamic	125°C	44.0	1.9	45.0	3.7
SCCD P-Channel	dc	200°C	43.7	3.9	39.6	5.1
SCCD P-Channel	dynamic	200°C	44.2	1.3	44.6	0.9
BCCD N-Channel	dc	125°C	47.3	1.3	53.1	2.1
BCCD N-Channel	dynamic	125°C	47.6	1.2	51.5	0.9
BCCD N-Channel	dc	200°C	45.0	3.1	27.0	5.0

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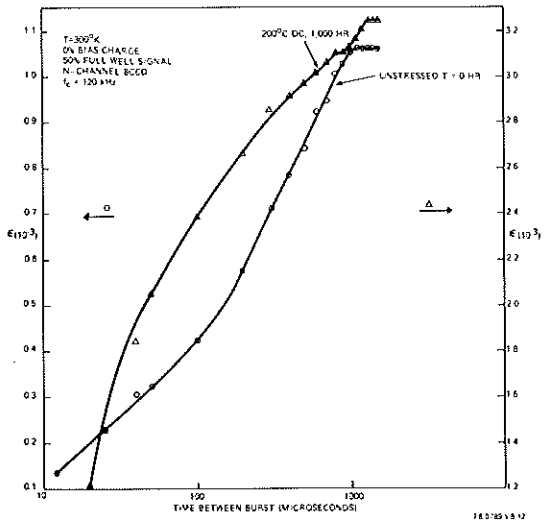

Figure 7. Double Pulse Experimental Results for the Unstressed and 200°C Stressed CCD-321 Devices

Device Type	Voltage Stress	Stress Temperature	Gate Threshold (volts)			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	14.9	0.2	14.9	0.1
SCCD P-Channel	dynamic	125°C	15.6	0.6	14.7	0.3
SCCD P-Channel	dc	200°C	15.6	0.2	15.0	0.2
SCCD P-Channel	dynamic	200°C	15.6	0.2	14.8	0.1

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Table 6
Input Gate "Threshold" Voltages for the SCCD Test Categories (Measurements Made at Room Temperature)

4.0 Conclusions

The results of temperature bias stress of p-surface channel CCD's and n-buried channel CCD's have been presented. A basic trend towards increased dark current and decreased charge transfer efficiency in the SCCD devices can be attributed to an increase in interface state density. A result of the stress testing on SCCD's is that dynamic testing appears to degrade parameters faster than dc stressing. A decrease in charge transfer efficiency under 200°C stress for 1,000 hours for the BCCD remains unexplained with the data currently available. The room temperature operating time necessary to achieve the worst case values is in excess of 5×10^6 hours.

Acknowledgement

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