A Bipolar Current Amplifier/Buffer Output for Very Small Geometry CCDs

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ABSTRACT

A reliable and sensitive charge detection scheme for very small charge packets is described. This scheme integrates a bipolar pnp device into the output gate of a CCD using one extra mask and two ion implants. The charge packet flows into the base causing a large emitter current flow in the bipolar device. This emitter current flows into the substrate. A simple analysis of the operation is presented. Trade offs of high β and low current β fall off are presented. Bipolar devices with β as high as 800 and base width of ~1500A have been fabricated. It is shown that good low current β fall off is more essential than high β. Finally various clocking schemes for this output are discussed.

INTRODUCTION

CCD's have now been established as a viable technology for memory applications. The trend towards higher density has resulted in very small geometry sizes and correspondingly small charge packets which must be transferred and detected reliably to meet the desired performance goals. The reliable detection of extremely small charge packets over a wide range of temperature and noise requires elaborate circuitry to provide the desired gain (viz regenerator circuits for 64k bit CCD memories). Charge detection schemes used with CCD's at present employ a capacitive voltage change of a floating node due to the signal charge packet. For small geometry CCDs (cell sizes of $\leq 50\mu m^2$) the charge packet size is decreased ($\lesssim 5 \times 10^{-15}$ coulombs) with a corresponding decrease of the output voltage swing. In this paper we describe a CCD output structure which utilizes a bipolar current amplification to achieve reliable detection of very small charge packets. The bipolar device is integrated at the end of the CCD channel. This structure is realized by adding one mask and two extra ion implantation steps at the end of the CCD process to fabricate a p^+ injector (emitter) and a non-depleted n-base region under it, at the output end of the CCD. The combination forms a vertical PNP structure with the substrate serving as the collector. The emitter

is biased through a depletion load, and its voltage is sensed through a source follower. The schematic diagram of this structure is shown in Figure 1.

When a charge packet flows into the base region of the PNP transistor, it turns on and draws emitter current which is β times the base current equivalent of the signal charge. This current gain allows a much larger drive capability. When the charge packet is annihilated by recombination in the base, the PNP transistor switches off and is automatically reset for the next charge packet. Contrary to floating node schemes, there is no precharging necessary and no clock feedthrough at the output when no charge packets are sensed in this mode of operation of the bipolar output detector. This feature is expected to result in reduced fixed pattern noise.

The capability of integrating bipolar buffer devices on the same chip as MOS/CCDs provides the current drive capability that allows this technology to compete with bipolar technologies for VLSI logic, memory and signal processing applications.

BIPOLAR OUTPUT CONCEPT AND DESIGN CONSIDERATIONS.

Figure 1 shows the cross-section of a CCD channel which incorporates a bipolar charge detection element at the output. This detection element is shown for a buried channel CCD structure. It can in principle be used with both surface and buried channel CCD's. The two phase coplanar electrode [1,2] CCD shown in Figure 1 is representative of the CCD structure which was used to demonstrate the concept. The concept is by no means limited to this CCD structure and may be used with other two, three or four phase versions as well.

The bipolar element is fabricated at the end of the CCD process by opening a window in the polysilicon output gate electrode. The n-type base region implant is performed through the same opening. In principle, the lateral straggle of the implants [3] should be adequate to ensure that no emitter collector shorts occur at the edge of the window. To guarantee this, however, a low temperature heat step ($\lesssim 200°C$) may be used to flow the resist into the window to provide additional margin.

The detection scheme presented here is designed to operate at very low current levels. The effective base current into this device may be computed from the dynamics of a charge packet being transfered

into the base region through the output gate. It has been shown, [4] that the charge transfer in a CCD is approximately exponential and electrode has a time constant τ_f which may be described by

$$\frac{1}{\tau_f} = C_1^2 \frac{\pi^2 D}{4L^2} + \frac{\mu^2 E_y^2}{4D} \qquad (1)$$

where

D = electron diffusivity

μ = electron mobility

L = length of the gate electrode

E_y = lateral fringing field

C_1 = a parameter that varies from 1 to 2 as the normalized fringing field varies from 0 to ∞.

The charge $Q_B(t)$ flowing into the base is represented as

$$Q_B(t) = Q_o A_{well}(1-e^{-t/\tau_f}). \qquad (2)$$

In this expression Q_o is the charge capacity per unit area and A_{well} is the area of the CCD storage well.

The base current in the bipolar device will then be given by

$$i_B = \frac{dQ_B(t)}{dt} = A_{well}\frac{Q_o}{\tau} e^{-t/\tau} \qquad (3)$$

This exponentially decaying pulse of i_B is fed into the bipolar device which is normally off.

The transient response due to this current may be estimated from the charge control analysis of the bipolar transistor. The charge packet will supply the base recombination, and charge the emitter and collector junction capacitance as well as the output gate capacitance connected to the base. The differential equation describing this process may be written as

$$\frac{d}{dt}(Q_B+Q_{Te}+Q_{Tc}) + \frac{Q_B}{\tau_B} + \frac{d}{dt}C_g v_{be} = -i_B \qquad (4)$$

where

Q_B = base minority charge

Q_{Te}, Q_{Tc} = junction transition capacitance

C_g = output gate capacitance

v_{be} = base emitter voltage

Following the standard charge control treatment [5] equation (4) may be written for our configuration as

$$i_B = \left(\frac{1}{w_T} + \frac{1}{w_g} + \frac{C_L R_L}{\beta}\right)\frac{dic}{dt} + \frac{i_c}{\beta} \qquad (5)$$

where $w_g = \frac{g_m}{C_g}$ for the output gate and $w_T = 2\pi f_T$ where f_T is the short-circuit current gain bandwidth product. The collector resistance is assumed to be zero, and $C_L R_L$ represents the emitter load.

We may now solve (5) and (3) to obtain the emitter current as

$$i_e(t) = \beta Q_o A_{well}\left[\frac{e^{-t/\ell.c.}}{\tau_f+k\beta} - \frac{\{(\beta-1)\tau_f+k\beta\}}{\beta\tau_f(\tau_f+k\beta)} e^{-t/\tau_f}\right]$$

where $k = \left(\frac{1}{w_T} + \frac{1}{w_g} + \frac{C_L R_L}{\beta}\right)$. (6)

It is obvious from (6) that the emitter current provides a factor of β increase in

the charge available to drive the next stage. Alternatively, the load capacitance is now reflected to the base node as $\frac{1}{\beta}$ times what it would be in a simple precharge circuit. Base widths of ~1500Å, as fabricated in our structure, would lead to an w_T of much greater than 1GHZ. So, in typical layouts, the total effective node capacitance of this output device is dominated by the enlarged output gate needed to enclose the base structure. Hence frequency response of this output structure would be limited by the output gate.

In Figure 2(a) we show a theoretical evaluation of the emitter current waveform based on (6) for a charge packet size of ~1.6 fc. The assumed parameter values are shown in the figure. The simple theory presented here is compared also to a numerical simulation using SPICE circuit simulator and typical MOS parameters (Figure 2b). For the SPICE simulation we have used a simplified current pulse as the input and plotted the emitter voltage as the output. The emitter voltage follows the emitter current prediction of Figure 2(a) based on the charge controlled model. It has been assumed in this calculation that minimum geometry output gate node can be built. In practice the output gate capacitance is larger since it surrounds the bipolar. This will limit the turn off characteristics of the bipolar device.

This application of the bipolar transistor as the output of the CCD shift register requires that the β fall off at low currents be minimized. It has been very well known that the low current β fall off is dominated primarily by injection efficiency considerations. The generation component of current in the emitter base depletion region and the surface recombination component play a very important role in the determination of the low current fall off characteristics of the bipolar transistor. The incorporation of a bipolar device in a CCD process has some very significant advantages. CCD's are built on (100) silicon to obtain low surface state density. Gettering sequences designed into the process allow very high bulk lifetimes to be achieved in processed devices [6,7]. Bulk lifetimes of ~1msec and surface recombination velocity of $\lesssim$ 1cm/sec have been measured in our devices. In addition Hansell and Fonstad [8] have shown that the β linearity at low currents is affected most significantly by decreasing emitter doping to take advantage of the increased mobility. They show that β at very low currents is obtained at the expense of the absolute β value.

We have fabricated bipolar structures

with a β of ~800 as well as those with ~100-150. The variations in β were achieved by varying the base implant dose. The typical implant distribution calculated for bipolar devices with β ~100-150 is shown in Figure 3. The estimated f_T of this pnp transistor from theoretical consideration is > 1GHZ. However, frequency response of the bipolar device by itself cannot be measured since it si integrated with a FET device at the base. The β vs. I_c characteristics of these devices is shown in Figure 4. For a typical charge packet size of ~4×10^{-15} coul. and a gate length of ~4μm the effective base current pulse is about 26nA. Thus for β ~ 100 the typical operating region is at I_c ~26μA. It is obvious from Figure 4 that our design for β ~100 has adequate low current β linearity.

OPERATION AS CCD OUTPUT AMPLIFIER.

The bipolar device concept and design discussed in the previous section may be operated in three distinct modes at the output of a CCD shift register. In the simplest mode the bipolar device is operated with a fixed emitter bias obtained through the depletion device which acts as an emitter load. In this mode, the charge packet turns on the bipolar as was described in the previous section, and a large current gain is obtained. However there is no voltage gain available because the emitter voltage follows the base voltage. The effective charge to voltage ratio, of course, depends on the ratio of the net output node capacitance to the capacitance of a storage well. The use of the bipolar device provides an impedance transformation so that the load capacitance on the emitter node is reflected as a βtimes smaller capacitance at the base. Thus for a given load an effective increase in the net voltage swing may be obtained for a given charge packet size. This increase is partly offset, however, by the increased capacitance components due to base emitter capacitance of the bipolar device. The operation in this mode has the advantage of very low coupling of clocks and precharge pulses compared to a normal precharged output. A large current drive capability is obtained but the voltage swing is not significantly increased. We have found an effective current gain at the output of ~ β in CCD operation in this mode. Figure 5 shows the output of a CCD register and the input pulse. The input and output occur simultaneously by choosing the number of bits between input pulses to be equal to the length of the register.

The second mode of operation uses a dynamic emitter biasing or precharging of the emitter node before the charge packet flows into the base. In this mode the emitter is floating when the charge flows into the base and the transient emitter current proportional to $(\beta + 1)I_B$, produces a transient emitter voltage spike which may be much larger than ΔV_{be}. Thus a large transient voltage swing is available on the base which may be used as a latching signal. We have measured ~400mV signals on 4×10^{-15} coulomb of charge using this clocking scheme compared to 55mV output swing using the dc scheme.

The bipolar output may be operated in a non-destructive mode also. To achieve this, the device is built into one of the electrodes of the shift register. The charge packet flows into the base and remains there for the clock period. During this time the bipolar is turned on. The next phase clocks the charge out of the base into the next storage location. Thus the signal charge may be propagated after the read operation using the bipolar device. The signal charge used to provide the output signal corresponds to the fraction of the charge packet which recombines in the base during the read cycle. Since all base charge does not have to recombine, this mode of clocking may provide an extremely high speed output.

The bipolar output scheme described in this paper has an added advantage for memory applications. The change in base voltage ΔV_{be} is proportional to the charge packet, and the collector current is proportional to $\exp(q\Delta V_{be}/kT)$. Thus for the second clocking scheme where the emitter is floating, the transient spike is exponentially proportional to the charge packet, so that a '0' and '1' can be very easily differentiated.

SUMMARY

A bipolar charge detection concept has been presented. It is shown that the concept may be implemented in a CCD process at the cost of one mask and two ion implants. Design considerations for this concept are presented. CCD shift registers have been fabricated to demonstrate the concept. It is observed that output voltage signals ~x8 greater than the conventional precharge techniques may be obtained.

The integration of the bipolar output provides the capability of driving large loads with a small charge packet. This buffer capability may also be utilized for

high off-chip drive capability, which coupled with the advantages nMOS/CCD, provides a very high performance technology for logic, memory and signal processing.

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REFERENCES

1. A. F. Tasch Jr., R. C. Frye. "Improved Silicon Gate CCD Structure", U. S. patent no. 4027381.
2. P. K. Chatterjee, A. F. Tasch Jr., H-S Fu and T. C. Holloway, "The Enhanced Capacity CCD" to be published in IEEE Trans. Electron Devices.
3. J. F. Gibbons, W. S. Johnson and S. W. Mylroie., "Projected Range Statistics" Dowden, Hutchinson and Ross, Stroudsburg Pennsylvania, 1975.
4. Y. Diamon, A. M. Mohsen, and T. C. McGill, "Charge Transfer in Buried Channel CCD's" ISSCC Philadelphia, Digest of Tech Papers. p 146, 1974.
5. See for example J. Milman and H. Taub "Pulse Digital and Switching Waveforms" McGraw Hill Book Company, New York 1965, p 785.
6. H. S. Fu and A. F. Tasch Jr., unpublished.
7. P. K. Chatterjee, G. W. Taylor, A. F. Tasch Jr. and H. S. Fu, "Leakage Studies in High Density Dynamic MOS Structures" to be published in IEEE Trans. Electron Dev.
8. G. L. Hansell and C. G. Fonstad "A Bipolar NPN Transistor with reduced β Fall Off" Device Research Conference, Ithaca, New York, 1977.

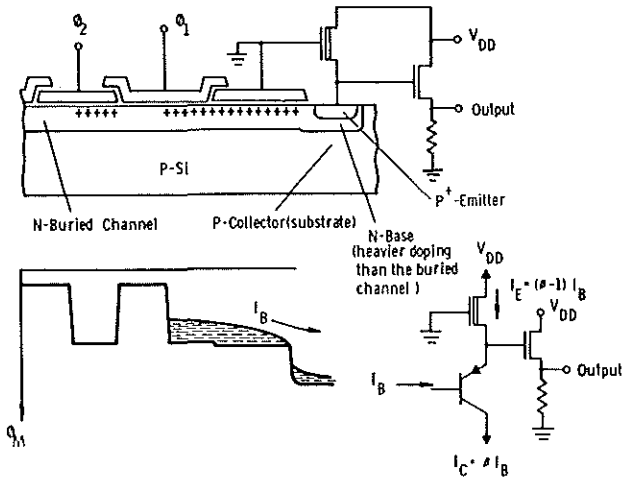

Figure 1 The structure and concept of the bipolar output for CCDs. The top figure shows the crossection of the output and the bottom shows the operation of this output scheme.

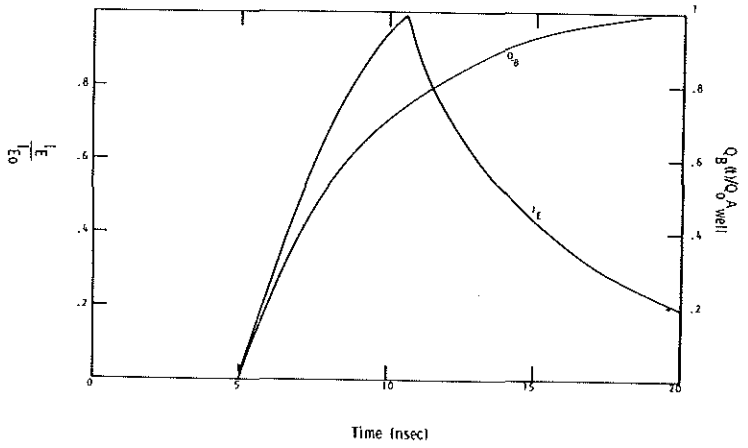

Figure 2(a) The emitter current response of the bipolar for a charge packet. The charge packet size ($Q_{A_{well}}$ = 1.6fc) and the maximum emitter current is I_{Eo} = 2.3μA. The calculations are based on β=100 and k=.09nsec.

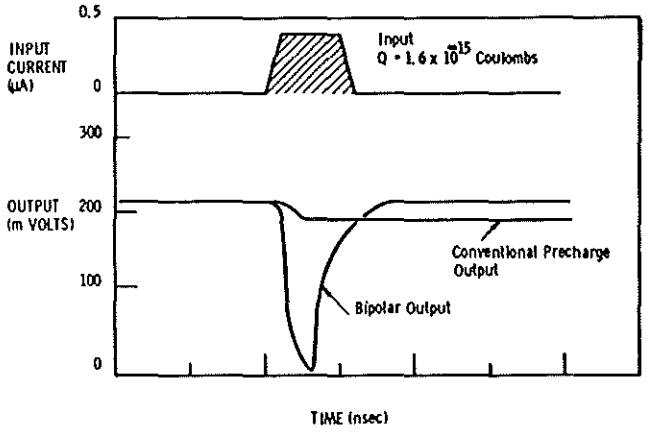

Figure 2(b) SPICE simulation of the bipolar output. The response to a current pulse I_B is shown. This simulation is more optimistic than the charge control theory because default parameters for the bipolar are used.

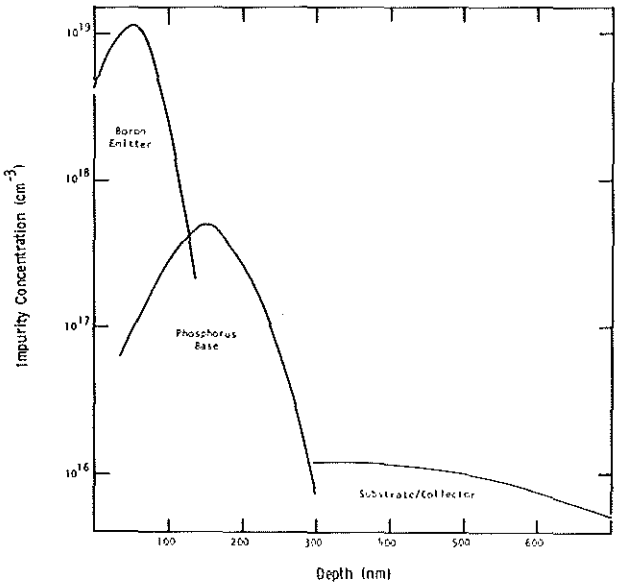

Figure 3 Doping distribution is due to the base and emitter ion implants forming the pnp bipolar. The collector distribution is non-uniform becuase of the channel implants required to avoid short channel effects and punch through.

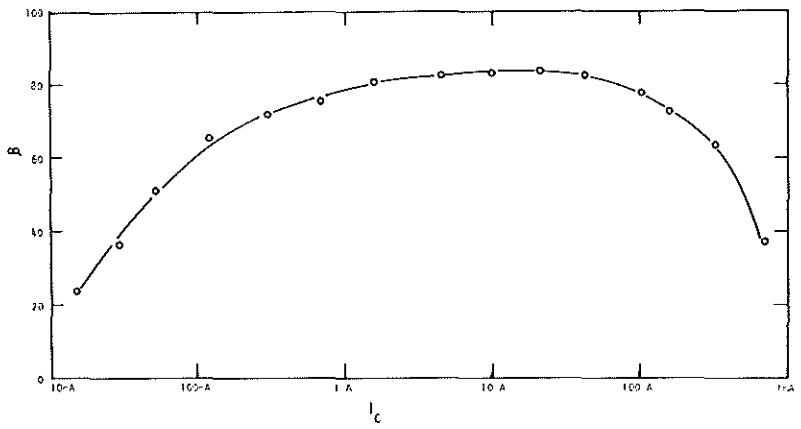

Figure 4 β vs. I_C characteristics of the output bipolar device.

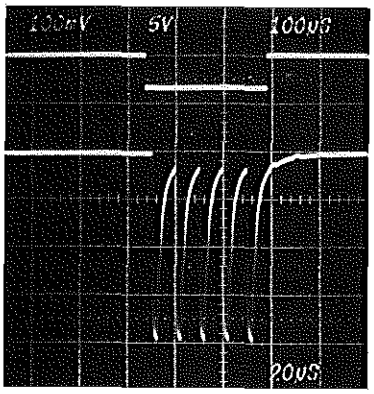

Figure 5 Input and output of a CCD shift register with a bipolar output.