DISPLACEMENT CHARGE SUBTRACTION CCD TRANSVERSAL FILTERS

P. R. Prince,
T. J. Mahony,
J. A. Sekula
Hughes Aircraft Co.
Culver City, Calif.

D. G. Maeding
Hughes Aircraft Co.
Carlsbad, Calif.

N. Ćuk
Hughes Aircraft Co.
Newport Beach, Calif.

ABSTRACT

One-sided CCD transversal filters with a tap weight structure that eliminates the "common mode" sense electrode area (and minimizes the corresponding nonlinear depletion capacitance) are described. The resulting low-capacitance sensing nodes allow these filters to be input noise limited.

Differential amplifiers are not required when displacement charge subtraction (DCS) is used; it provides inherent signal differencing on a single node connecting all floating sense electrodes. Signal packets enter under some electrodes when other signal packets leave from under other electrodes, thereby causing signal subtraction. And because the ϕ_1 and ϕ_2 clocks overlap the sense electrodes equally, clock pickup is eliminated.

DCS in combination with the one-sided structure can be implemented by separating negative and positive tap weight sections by one half clock cycle. One-sided DCS matched filters have been fabricated and tested. Measurements of a 62-tap p-channel device indicate a 91-db dynamic range (rms signal-to-noise ratio for a 0.6-percent total harmonic distortion) and 68-db common mode rejection for the subtraction function without the use of a differential amplifier.

INTRODUCTION

Charge coupled device[1, 19] transversal filters (TVF)[2-6] have shown very impressive potential in the fields of visible and infrared signal processing,[7, 8] radar signal processing,[9, 11] communications,[12-14] and spatial image processing.[29] Their inherent low noise, coupled with current transfer efficiencies and current and near future precision lithography[28] provides a solid foundation for a truly revolutionary signal processing device family. However, conventional two-sided split electrode structures, though providing impressive performance characteristics, are subject to several limitations, such as limited signal-to-noise ratio (S/N) caused by excess sensing node capacitance, difficulties with clock pickup, poor common mode rejection due to capacitance imbalance of the sensing nodes, differential amplifier limitations, and marginal linearity (or complex linearizing and output sensing schemes). This paper introduces a unique combination of simplifications to the basic split electrode TVF configuration that substantially reduces these limitations and improves performance while conserving silicon area.

Single-phase clocking simplifies floating electrode voltage reference setting.[5, 6, 15] In conjunction with single-phase clocking, a one-sided structure eliminates excess nodal capacitance and thereby provides the largest possible signal amplitude by avoiding connection of the sensing node to any unwanted fractions of the split electrodes and associated unnecessary nonlinear depletion capacitance. With these simplifications, the dominant noise of the device can be limited to the CCD input noise with small contributions from other sources.[11, 16, 17] A one-sided structure also facilitates device layout. Additionally, displacement charge subtraction can be used to obtain precision subtraction without the need for

relative gain adjustment, and can thereby eliminate the need for output differential or instrumentation amplifiers.

Combining DCS with the single-sided structure results in small, precision signal processing devices that will require only a minimum of support circuitry and power and provide a high process yield potential. The operating frequency is not limited by differential amplifier characteristics.

ONE-SIDED CCD TRANSVERSAL FILTERS

Figure 1 illustrates a conventional two-sided TVF structure(2, 18) of width W, with N weighted electrodes (47 shown). For simplicity, the CCD register input and output circuits are not shown. The upper (negative) split electrode portions are both connected to the negative input of a differential amplifier; likewise, the lower split electrode portions are connected to the positive differential amplifier input. A SET switch is used for defining the potential of the sense electrodes (and associated surface potential thereunder) between samples. The sense electrode node clamping function is referred to as SETTING to indicate that the electrodes are "set" to a reference voltage. Each output summing node has an average capacitance C_2 nominally equal to WNc/2, where c is the capacitance per unit width of a floating sense electrode which involves neighboring electrode overlap capacitance in parallel with the series combination of electrode oxide capacitance and depletion capacitance (which for this discussion is assumed to be constant). For a CCD signal charge of q* per unit width, the peak of the impulse response signal S_{P2} is $q^* W/C_2$. Therefore, the peak impulse response signal is

$$S_{P2} = 2q^*/Nc \qquad (1)$$

(and is independent of CCD width). This assumes C_A (amplifier and any added capacitance) is negligible.

As ϕ_1 rises (p-channel) charge is transferred over the d-c electrode potential and into the potential well that is forming under the floating electrode (see Figure 1c). At this time ϕ_{SET} is "off." Displacement currents flow through the depletion capacitance C_d to the substrate and through the oxide capacitance C_{ox} to the sense node and to the other electrodes, including the overlapping clock and d-c electrode capacitances. The resulting displacement charges are stored on the nodal capacitance and cause the sense node voltage to shift positively in proportion to the tap weight length (with nonlinearities of C_d).(2, 18-21) The bottom of the potential well also shifts in response to the voltage shift on the sense node. An examination of bit i of the structure shows that to obtain a small net positive signal, a large negative signal and slightly larger positive signal are processed and subtracted. The capacitance of the total signal is Wc, whereas the capacitance equivalent of the desired signal is h_iWc, where h_i (≤ 1) is the weighting coefficient. For i (as illustrated) this coefficient is equal to about +0.3. All shaded areas in Figure 1b are involved in the outputs and contribute to sense node capacitance.

Figure 2 illustrates a one-sided TVF in which all excess electrode area has been eliminated by connection to a bias voltage V_{DC}. Only the shaded areas in Figure 2 are involved in its outputs. A stop diffusion is located under the split electrode gap region (see inset in Figure 1b). It must extend slightly under the surface d-c electrode region ahead in order to ensure that lateral charge transfer does not occur during the transfer of charge under the sense electrodes. The use of stop diffusions under the electrode gaps allows a variation in potential between the two sides, thereby greatly simplifying the output sensing circuit. The stop diffusion separator also improves tap weight accuracy.(23) Two limitations of this technique must be considered. First, nonlinearity of depletion capacitance causes distortion, which may limit the useful dynamic range in some applications. However the one-sided TVF minimizes the depletion capacitance (for a given signal) under the sensing node so that any added capacitance to the sensing node is more effective in reducing nonlinearities. The second problem is related to lateral charge transfer between sense electrodes. If lateral charge equilibration is not completed before the subsequent charge splitting operation, splitting precision is affected at high clock rates.(20-22) These two limitations are being investigated.

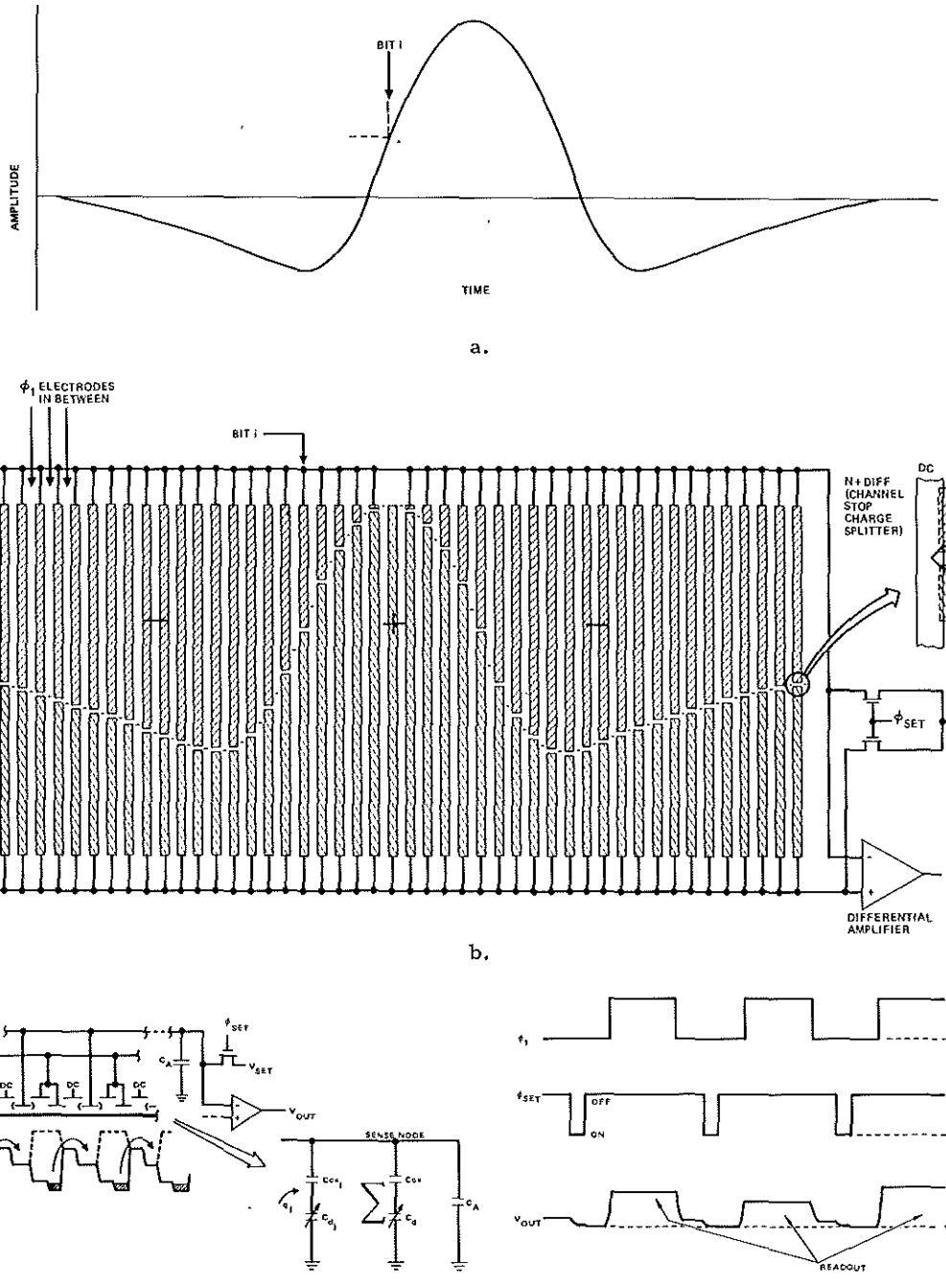


Figure 1. Desired impulse response waveform (a), conventional two-sided transversal filter, with stop diffusions located under electrode gaps (b), schematic/potential diagram (c), and clock waveforms (d).

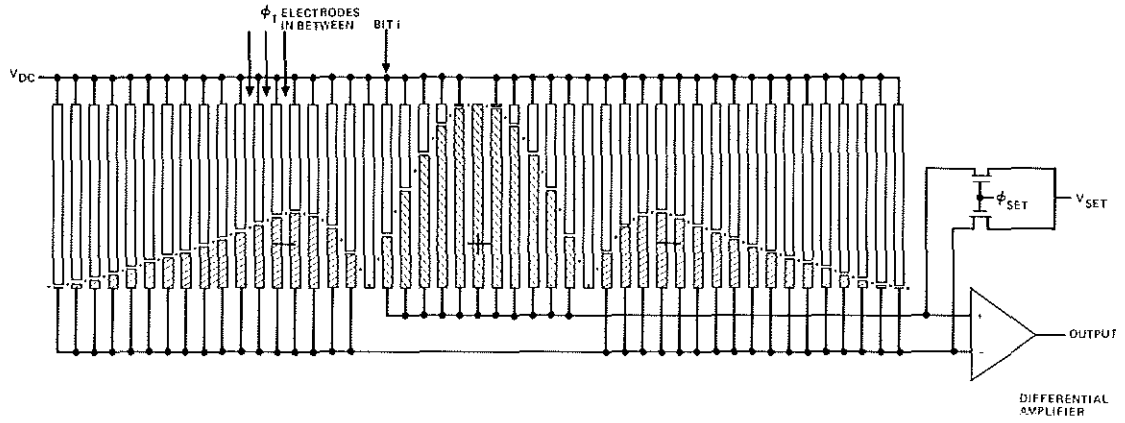


Figure 2. One-sided transfersal filter providing impulse response function shown in Figure 1a, with about three times the signal amplitude (h_m = 0.33) of the filter of Figure 1(b).

For a zero d-c response one-sided TVF of width W, each tap weight node has a capacitance C_1 equal to (neglecting C_A):

$$1/2 \sum_{i=1}^{N} |h_i| Wc = h_m NWc/2$$

where h_m, the mean tap weight, ranges from less than 0.1 to 0.7 for typical filter functions (h_m = 1.0 for digital transversal filters with discrete coefficients having values of ±1.0 only). The peak impulse response signal S_{P1} is $q^* W/C_1$, so that

$$S_{P1} = \frac{2q^*}{h_m Nc} \qquad (2)$$

A comparison of Equations (1) and (2) shows that an increase in signal by a factor of $1/h_m$ is obtained for the one-sided structure.

The width of the one-sided filter shown in Figure 2 is half the width of the two-sided filter in Figure 1 and generally provides a significantly greater signal amplitude, and equal tap weight mask resolution. This increase in signal amplitude can in turn increase the signal-to-output amplifier noise ratio by $1/h_m$. For a one-sided filter equal in width to a two-sided filter, the ratio of signal to reset noise for the sense node is improved by $1/\sqrt{h_m}$ and the tap weight resolution becomes twice as fine. As is the case with a two-sided filter, any additional capacitive loading in the output or clamping circuit reduces the signal and the S/N, but some additional capacitance may be necessary in order to reduce pickup from overlapping clock electrodes (non-DCS single-sided filters) or to reduce nonlinearity caused by depletion capacitance.

A microphotograph of a matched one-sided TVF is shown in Figure 3. The relative frequency response shape and measured noise spectrum (see Figure 4) indicate that the input noise is dominant and

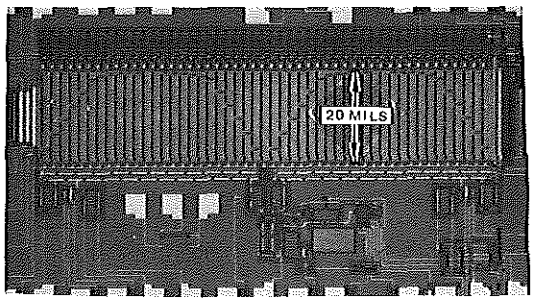


Figure 3. Microphotograph of a one-sided matched transversal filter (2091 chip).

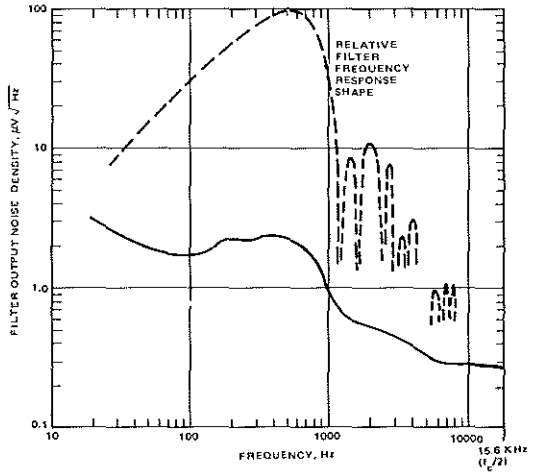


Figure 4. Relative frequency response and output noise spectrum of the one-sided filter of Figure 3.

can be clearly identified in the spectrum since it follows the frequency response shape. The noise integral of this curve is 79 μvolts rms. The filter output signal at its peak response point for low distortion was approximately 0.5 v rms, which provides a dynamic range of about 76 db (when measurements were made, no harmonic distortion data was taken).

DISPLACEMENT CHARGE SUBTRACTION

Figure 5a illustrates the charge flow with respect to a floating sense electrode whose voltage is "set" before the transfer of charge q_a (holes) under the sense electrode. After ϕ_{SET} goes off, ϕ_1 rises and charge flows according to the arrow, causing displacement currents to flow through C_d and C_{ox}. The resulting incremental voltage signal is positive for a p-channel CCD.

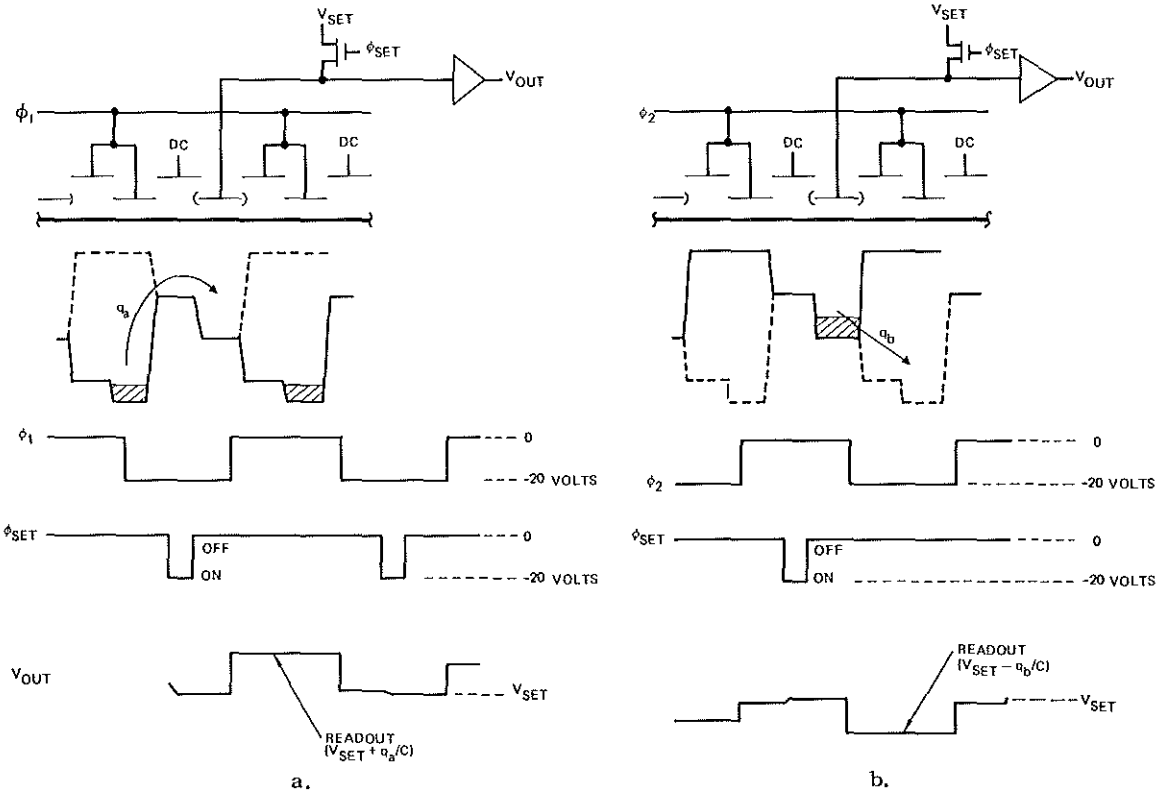


Figure 5. Displacement charge subtraction principle based on ability to set a floating gate voltage without signal charge underneath for positive excursions (a) or with charge underneath for negative excursions (b).

In Figure 5b, ϕ_{SET} is timed to set the voltage of the sense electrode while charge q_b is in the potential well that is formed under this electrode (i.e., when the neighboring clock ϕ_2 is high). When charge is subsequently transferred, it leaves the region and thereby induces a negative incremental voltage signal. If ϕ_2 is established as the complement of ϕ_1, the two floating sense electrodes (of Figure 5a and 5b) can be connected and will provide an incremental voltage signal of $(q_a' - q_b')/C_T$, where C_T is the combined floating sensing node capacitance and q_a' and q_b' are fractions of q_a and q_b (each of which divide and flow partially through the depletion capacitance to the substrate and partially through C_{ox} to the sensing node). C_T is common so that q_a' and q_b' subtract with substantially zero common mode error, because when they are equal the surface potentials and depletion capacitances are equal, whether high or low. Second-order effects, such as total positive and negative electrode area differences, appear to ultimately limit the common mode rejection ratio (CMMR).

THE DCS TRANSVERSAL FILTER

In general, transversal filters can have a number of sections of positive and negative coefficients. Four transition types can be defined: two with zero-value coefficients at the transitions (positive to negative and negative to positive), and two without zero-value coefficients at the transitions. DCS filters require unique structures and clocking for these various types.

Figure 6 illustrates a three-section, one-sided DCS transversal filter with two transitions. The normal ϕ_1 and ϕ_2 structure is used, with a d-c and floating gate pair substituted for ϕ_2 in the first and third sections and for ϕ_1 in the center section. As usual, the signal charge packets are separated by one structural bit (group of four electrodes). However, in the transition from the first tap weight section (positive) to the second section (negative), the signal packets are shifted in time with respect to the sense electrodes by one-half bit. This shift is accomplished by shifting the sense electrodes in the structure a half-bit closer at the transition. However, in order to provide charge transfer, an additional one bit delay is needed at this transition; otherwise two consecutive sense electrodes will occur. This extra bit provides a zero-value weighting coefficient. In the potential diagram, charges are shown at the time of the reference setting t_1, with ϕ_{SET} and ϕ_1 both negative. When ϕ_1 rises at t_2, all the charge packets simultaneously move according to the arrows. At that time ϕ_1 is going positive and the first and third tap weight section charges are entering the well under the sense electrodes. In the second section, charges are leaving (ϕ_2 is going negative). Note that all sense electrodes are connected together and to a simple source follower output.

For the transition from the second (negative) tap section to the third (positive) section, the floating electrodes are structurally a half bit farther apart. It is therefore unnecessary to add a delay bit at this transition to obtain charge transfer. To illustrate a symmetrical impulse response with a zero value coefficient, an extra delay is included. Without this delay, the filter would not provide a zero-value coefficient at this transition.

If it is necessary to generate impulse functions with more than one transition and without zero-value coefficients at the transitions, an additional clock $\phi_{1/2}$ is required. For the filter in Figure 6, the $\phi_{1/2}$ electrode pair of the first added delay bit can be momentarily held more negative than ϕ_1. The charge packet that leaves the last positive sense electrode in the first section is attracted by $\phi_{1/2}$ and then transferred to the first negative sense electrode without losing a clock period. Thus multiple-section impulse response functions can be implemented by means of simple electrode structures.

Since all sense electrodes are connected, the nodal capacitance is doubled with respect to a one-sided, non-DCS structure. Therefore, on this node the signal amplitude is half that of the one-sided filter. There is, though, only one sense node and one reset device. The reset noise decreases by $\sqrt{1/2}$ because of the increase in capacitance; hence there is a nodal $(S/N)_{reset}$ loss of $\sqrt{1/2}$. However, this S/N loss is similar to the S/N loss due to the rms combination in the differential amplifier of two reset noise sources of a non-DCS filter.

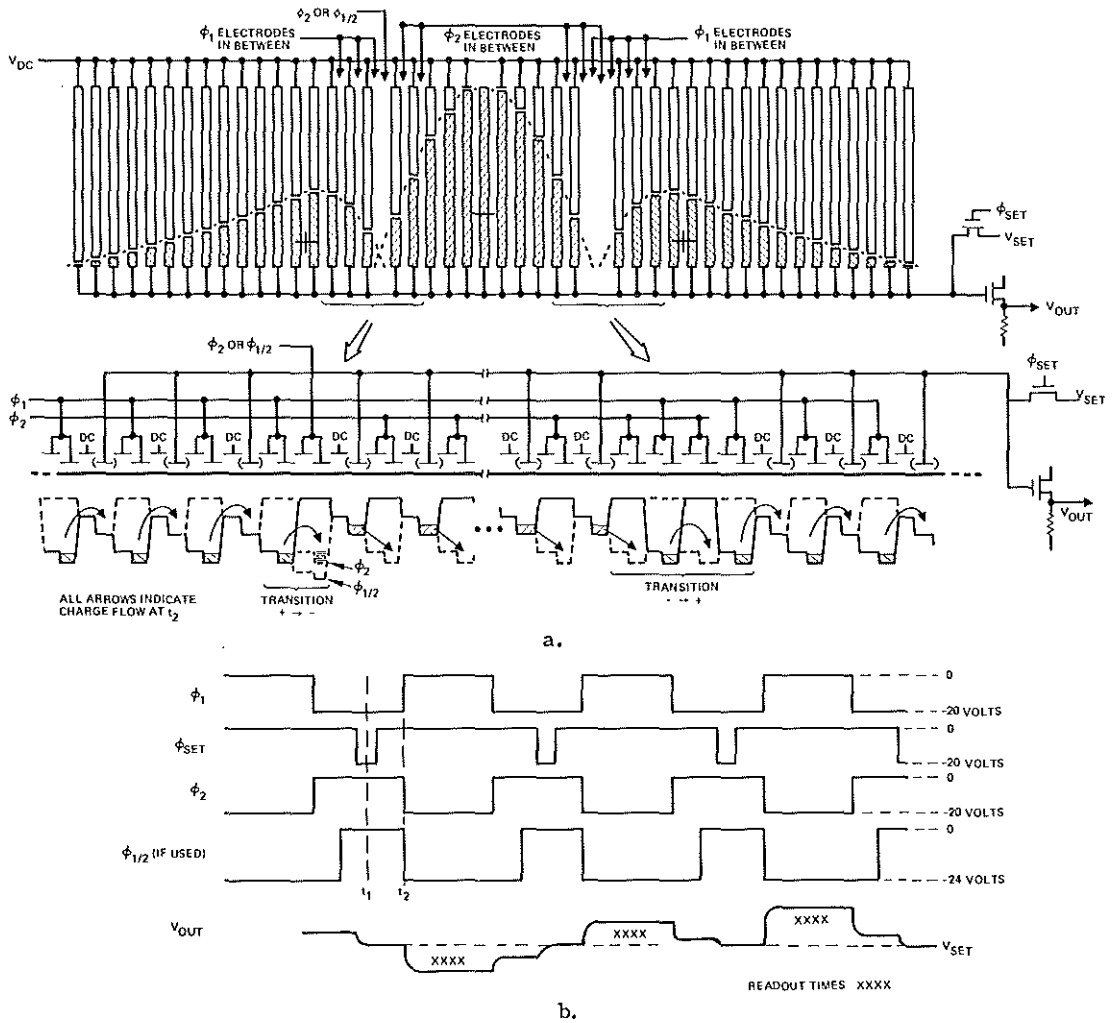


Figure 6. One-sided DCS transversal filter showing electrode structure and charge flow in (a) at time t_2 indicated in clock waveforms in (b).

For matched filters and bandpass filters that require zero d-c response, the sense electrode overlap of ϕ_1 and ϕ_2 will be equal in total length because $\Sigma + h_i = \Sigma - h_i$. Clock pickup is therefore substantially cancelled if the clock amplitudes and rise and fall times are equal. For filters requiring d-c response, simple coupling of the appropriate clock signal to the sense node can be used with only a small increase in sense node capacitance. Alternatively, a second, parallel filter with the impulse response function inverted and the input inverted (or V_{in2} rather than V_{in3} modulated) can be implemented with the sensing nodes of both filters made common. In this way the clock pickup will cancel for non-zero d-c response filter functions.

A single low noise operational amplifier charge integrator[19] can be used on the sense node if desired. This configuration minimizes the nonlinearity caused by depletion capacitance and it can be arranged to provide better thermal d-c

stability than a simple source follower. The advantages of DCS CMMR and the removal of clock pickup would remain.

DCS MATCHED FILTER TEST DEVICE

A p-channel two-level polysilicon DCS matched filter was fabricated on 3Ω-cm material using a 2X projection aligner according to the schematic/potential diagram in Figure 7. The filter provides a two-section 62-coefficient response (or 63 if clocked to provide a zero-value coefficient at the transition) with a 50-μm bit length and a 650-μm channel width, designed for low-frequency operation (i.e., <80 kHz). The total sense node capacitance is about 66 pf.

Stop diffusions 6-1/2-μm wide are located underneath the electrode gaps and extend forward to a point 8-μm under the 18-μm long d-c electrodes. All weighted coefficients are connected to a common sense node which is coupled to a source follower and to a one-stage sample/hold (S/H) circuit. The hold capacitance is 3.4 pf. The unused electrode areas on the other side of the sense electrodes (i.e., the $(1-h_i)$ parts) are connected to a common node and provided with a SET switch and a separate bias voltage V_{R2}. $\phi_{set\ 2}$ can be held at -20 vdc, and with V_{R2} anywhere between about -6 and -14 vdc there is no obvious effect on filter operation. The transition $\phi_{1/2}$ electrode was made externally accessible and was connected to ϕ_2 for all testing reported here.

Considerable excess capacitance was added to the sense node to ensure operability and to allow a direct comparison with similar non-DCS devices of the same design (not yet tested). Reducing the excess capacitance and providing less d-c electrode overlap would result in a significant signal swing and increase in S/N ratio at the expense of linearity (it is possible to reduce the nodal capacitance by about 30 pf). The SET switches were designed to restore V_{SET} on the sense node within 2 μsec. Table 1 lists the values of several other important parameters of the DCS filter described. A microphotograph of the DCS matched filter is shown in Figure 8. The nonuniform impulse response is an intentional match to the optical diffraction characteristics of an expected signal.

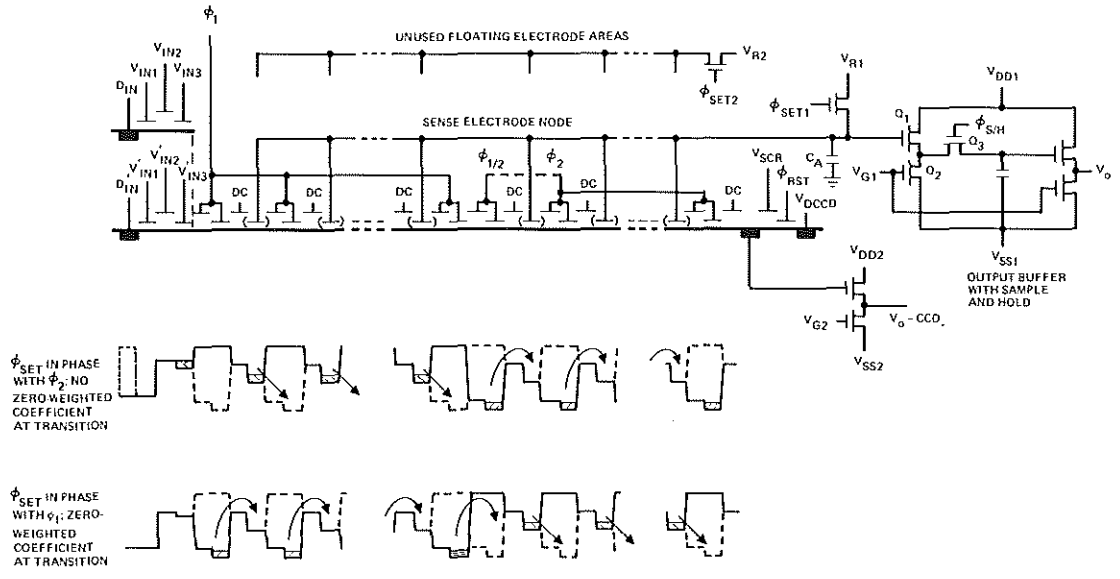


Figure 7. Schematic/potential diagram of DCS filter test device.

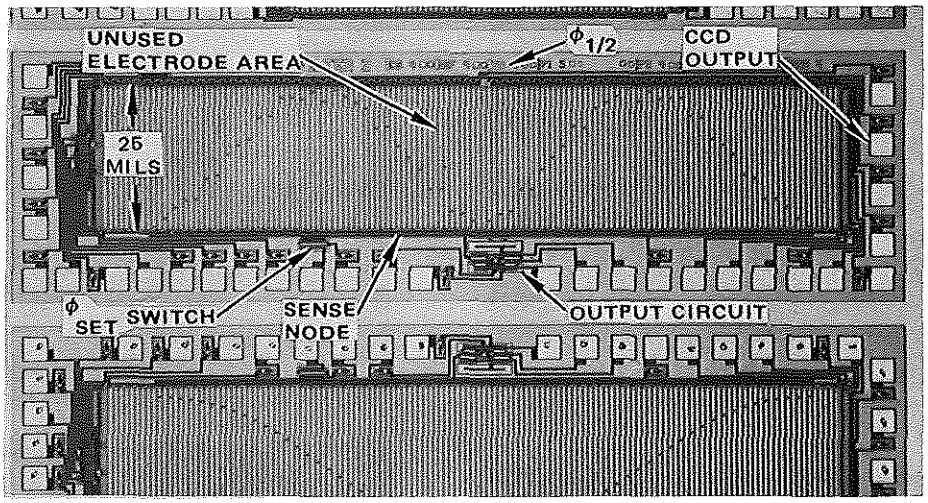


Figure 8. Microphotograph of DCS matched filter test device (2155 chip).

TABLE 1. DCS Filter Parameters

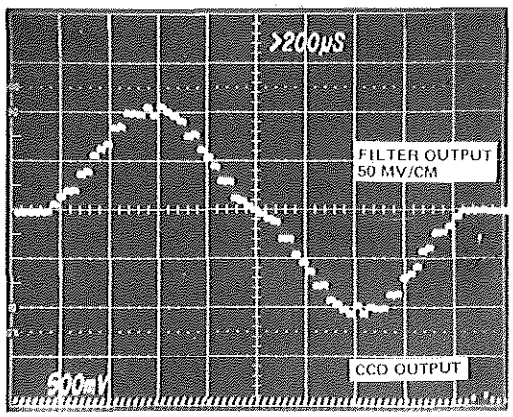
Register: 68 bits, 62 tapped; 2-mil bit length, 25-mil channel width. Capacitances, pf (calculated):			
Input electrode (of V_{in3})			2.0
Sense electrodes		8.2	
V_{dc} overlap		31.3	
ϕ_1, ϕ_2 overlap		9.8	
Excess added (over stop diffusions)		16.1	
Miscellaneous		0.4	
Total sense node			65.6
CCD output diffusion			2.0
ϕ_{sat} switch, μm	W = 120		
	L = 10		
Sample/hold			
Capacitor, pf			3.4
Source follower dimensions, μm	W = 68		
	L = 12		
Current source dimensions, μm	W = 48		
	L = 12		
Measured gain (overall S/H)		0.74	
Measured bandwidth with external cabling		100 kHz;	

EXPERIMENTAL RESULTS

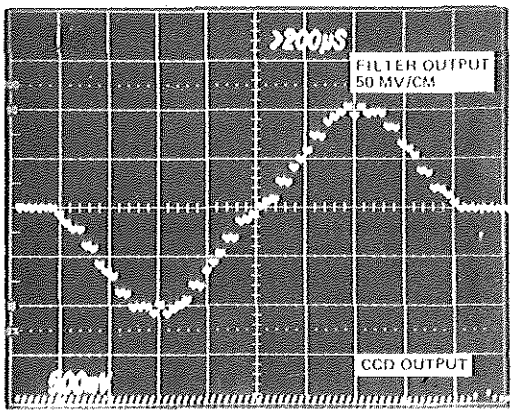
The key parameters of interest were cancellation of clock pickup, CMMR of the subtraction function, distortion, noise spectrum, and S/N. A charge equilibration input was used with V_{in1} fixed at a large negative potential, V_{in2} fixed and defining the "fat zero" (with V_{in3} d-c level), and V_{in3} modulated.[24,25] For higher gain, V_{in1} can be used to define the "fat zero" with V_{in2} biased highly negative. The primed inputs, a summing input arrangement, were simply paralleled for these measurements.

In Figure 9, the impulse response waveform with a zero-value coefficient at the transition (a) is modified by shifting ϕ_{SET} into phase with ϕ_2 thereby eliminating the zero-value coefficient at the transition (b). The pattern of the impulse response matches the pattern seen in the chip photo. Both cases are shown expanded in the double exposure in Figure 10a where the sample/hold circuit was disabled. The zero-value coefficient is seen in the upper trace at the center. Figure 10b shows a clock-triggered, expanded, multiple-trace filter output without the sample/hold operating with clock amplitude and rise times and fall times misadjusted. In Figure 10c clock amplitude and rise and fall times are properly adjusted to eliminate clock pickup.

The DCS filter step response is shown in Figure 11a to illustrate overall waveform linearity and CMMR. The long-term response to a step, as seen with a low-frequency square wave, should approach a constant value; this value can be estimated from Figure 11b on the 5 mv/cm scale.



(a)

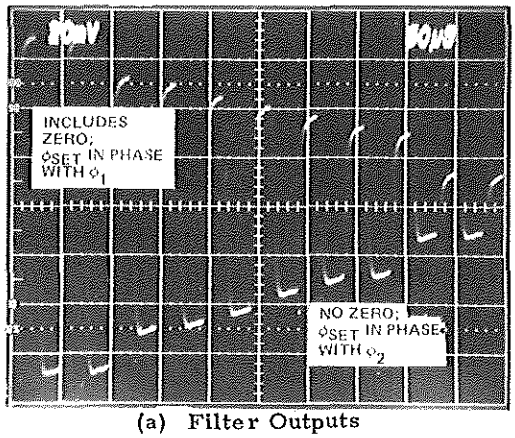


(b)

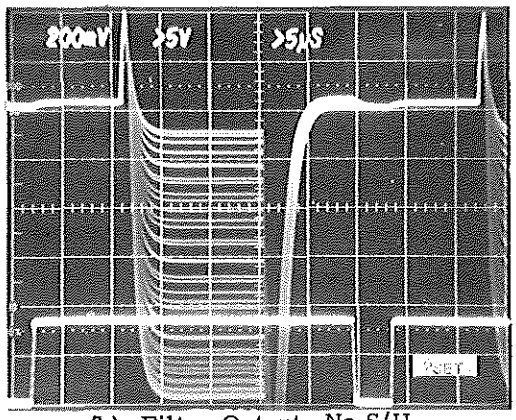
Figure 9. Impulse response waveforms of DCS matched filter with (a) and without (b) a zero-value coefficient at the tap weight section transition; f_c = 20-KHz.

DVM measurements for an input d-c level change providing a CCD output change of 1 volt (similar to the CCD output of Figure 11) caused a 0.6-mv d-c shift in the filter output. This shift corresponds to an equivalent common mode signal of 1.6 volts and a resulting CMMR of 68-db.

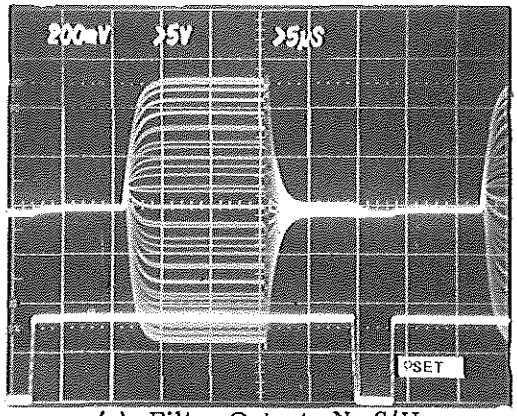
Figure 12 illustrates the calculated frequency response (tap weight digitization round-off was not included) and the measured response for operation at a 20-kHz clock frequency. Measurements were made using an HP3325A synthesizer function generator and a Quan-Tech 2449 wave analyzer using a 7 Hz bandwidth.



(a) Filter Outputs

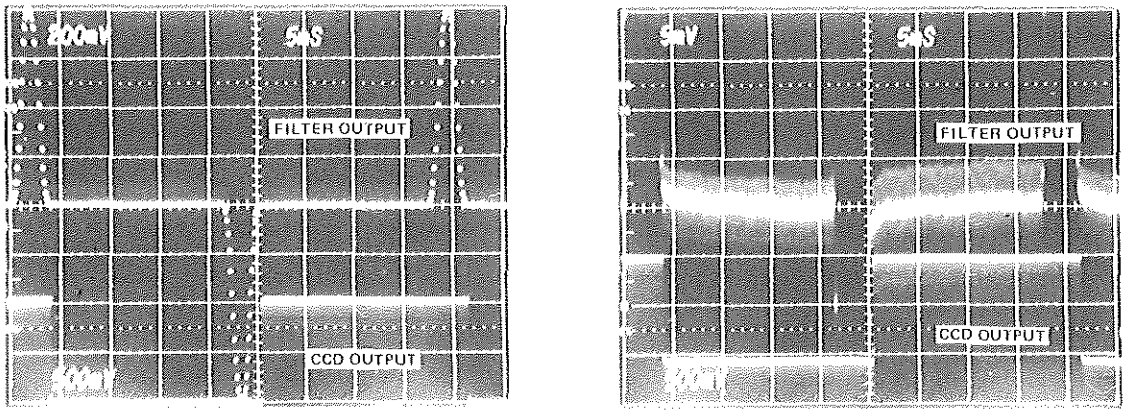


(b) Filter Output, No S/H



(c) Filter Output, No S/H (ϕ_1 and ϕ_2 Matching)

Figure 10. Double exposure of transition expanded without S/H (a) and multiple exposure showing clock pickup cancellation, signal modulation and ϕ_{SET} clamping (b). In (c), rise and fall times and amplitudes have been properly adjusted.



(a) (b)

Figure 11. Step response of DCS filter showing general linearity (a) and CMMR with filter output vertical scale expanded to 5 mv/cm (b).

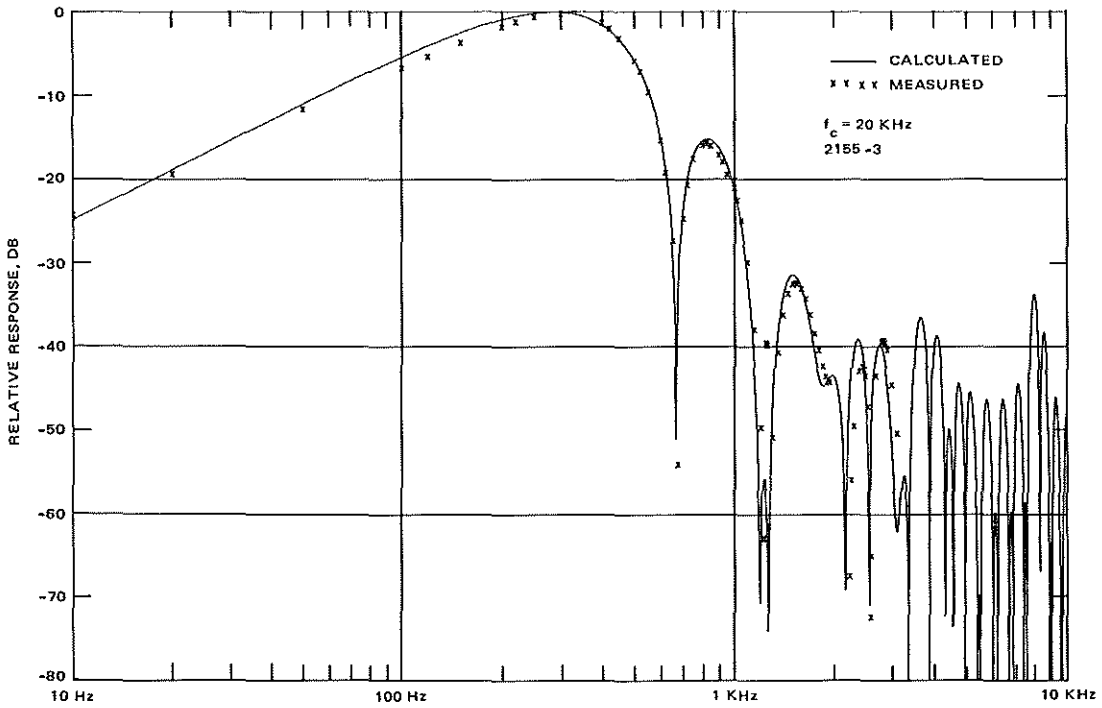


Figure 12. Calculated and measured frequency response of DCS matched filter operating with a 20-kHz clock.

Figure 13 illustrates four noise spectral density measurements that were taken. The upper curve (A) corresponds to operation with the on-chip S/H and has an integrated value of 134 μv rms, which provides an rms signal to noise ratio of 78 db for a filter output of 1.06 volts rms (3 volts peak-to-peak). Reset noise of the S/H is the dominant noise at high frequency in curve (A). This measurement was taken using a X100 nanovolt amplifier (Keithley 103A) following the filter output to provide sufficient amplitude for a narrow band (7-Hz) noise spectral density measurement. By disabling the on-chip S/H (set to -20 vdc) and disabling all clocks except ϕ_{SET}, the source follower 1/f noise and sense node reset noise seen in curve (B) was obtained.

To determine the inherent capability of the filter, a discrete S/H was placed after the X100 gain amplifier and the noise spectrum (C) was found to generally follow the shape of the filter function, indicating that the dominant noise is no longer output reset or S/H noise, but CCD input noise with contributions from 1/f, FIS, and charge splitting noise sources. A reduction of sensing node capacitance and/or a small on-chip gain followed by a correlated double S/H would reduce the effective 1/f and sensing node reset noise.

The low leakage on the DCS floating sense node provides an effective hold function during the readout portion of the clock

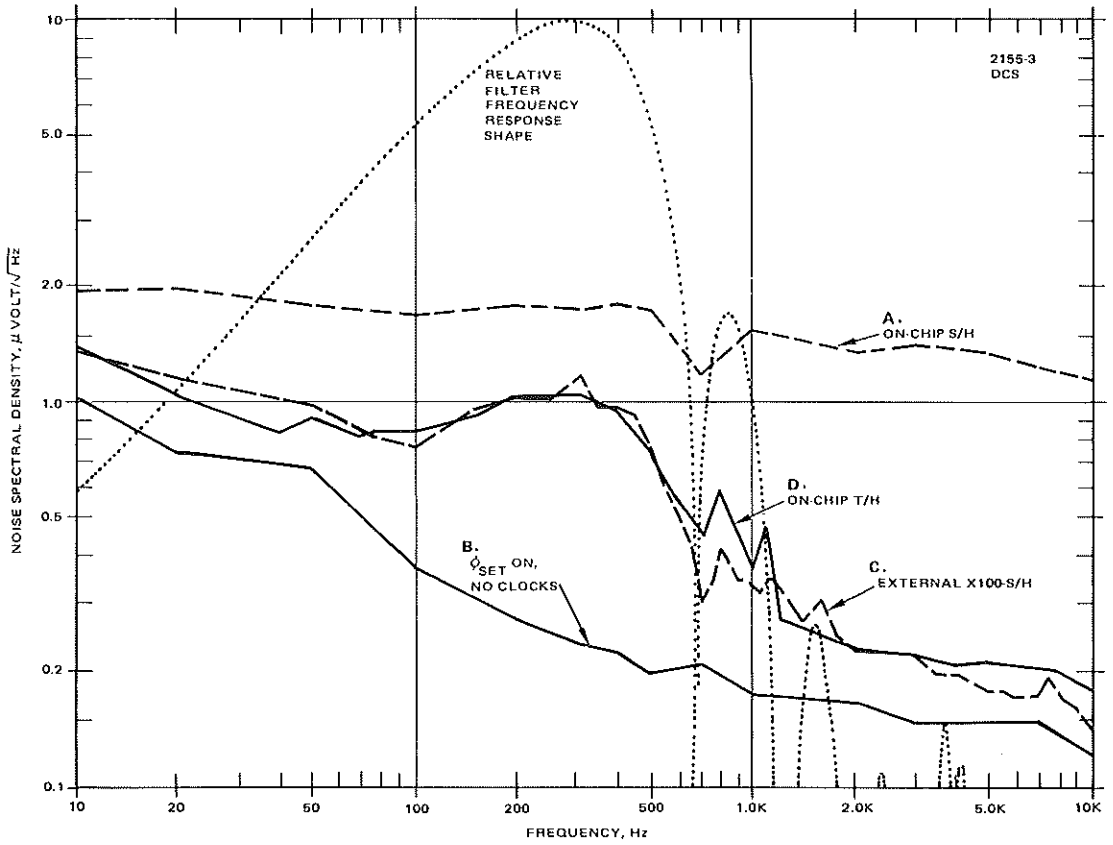


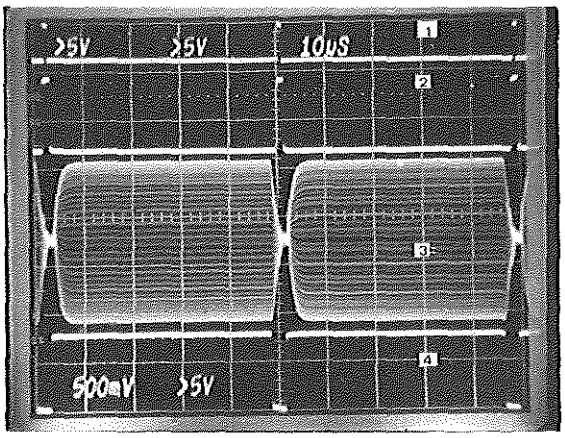
Figure 13. Noise spectral density curves of DCS matched filter operating with a 20-kHz clock, referred to filter output.

cycle. To reduce the effective noise contribution of the sample and hold, it can be changed to a track-and-hold so that it is held ON as long as the readout signal is stable. Then the noise of the S/H is only in the output signal during the hold time and not during the track time. Furthermore, the clocking can be greatly skewed so that the ϕ_1, ϕ_2, ϕ_{SET}, and the input diffusion clocks all occur over a relatively short time (compared to that of Figure 10) with respect to the readout time. Thus the track time can be made large and the hold time very small (in low frequency applications). Figure 14 (a) illustrates the input diffusion, ϕ_1 and ϕ_{SET} clocks for track-and-hold (T/H) skewed clocking, along with the filter output with the S/H switch held ON at -20 vdc. Figure 14 (b) shows the same filter output when the S/H switch is provided a track-and-hold waveform as shown (it was necessary to couple a small complimentary T/H pulse to the filter output with a resistor and a capacitor to cancel the capacitive coupling of the S/H switch.

The reset noise only occurs during the short hold time and therefore eliminates most of the S/H noise contribution. This is demonstrated in Figure 13, curve D, which is the measured noise spectrum for the DCS filter using its on-chip sampling circuit as a track-and-hold; virtually the same input noise limited performance as curve (C) is shown. Integration of this curve to 10 kHz ($f_c/2$) yields an rms noise of 31.4 μvolts. For a 1.06-v rms signal, the S/N is 91 db.

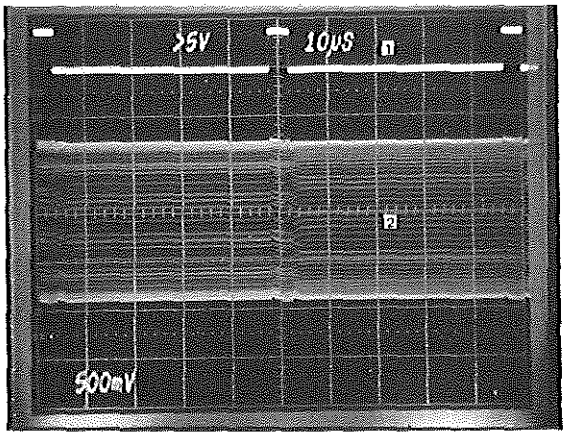
The availability of compatible MOS differential amplifiers and support circuitry[23, 26, 27] should provide the capability for temperature stable outputs that include linear gain, correlated double sampling, and the track-and-hold function followed with a band-limited output buffer to further improve S/N.

Distortion measurements were taken by setting the input sine wave source and



1) INPUT DIFFUSION CLOCK
2) ϕ_1 (= $\bar{\phi}_2$)
3) FILTER OUTPUT (NO S/H)
4) ϕSET

(a)



1) ϕT/H
2) FILTER OUTPUT WITH TRACK AND HOLD

(b)

Figure 14. DCS filter outputs showing clocks for skewed clock arrangement used for track-and-hold. In (a) the S/H switch is at -20 vdc while in (b) it is driven with a track-and-hold clock.

the wave analyzer to the peak response frequency f_o of the filter, and setting the input for the desired filter output amplitude. The filter response was considered the reference zero db level. The input was then adjusted to $f_o/2$, $f_o/3$, etc. (with no amplitude change) and the harmonic distortion was measured at f_o. The "fat zero" to provide the lowest second-harmonic distortion for a 2.5 volt p-p fundamental was determined at the beginning and used throughout for all harmonics and input levels. The harmonic distortion is plotted in Figure 15 against filter peak-to-peak output amplitude. The rms combination of all harmonics for a 3-volt peak-to-peak signal is 0.6 percent.

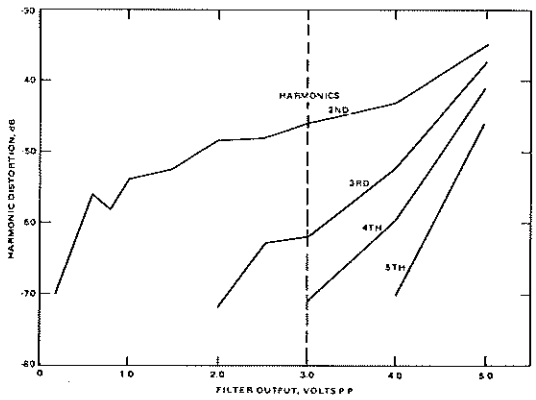


Figure 15. Harmonic distortion content in filter output at filter peak response frequency (for inputs at lower frequencies) vs filter output signal amplitude.

CONCLUSIONS

The operation of a fundamentally simple means for precision subtraction (DCS) on floating sense electrodes has been demonstrated and will open opportunities for a variety of charge transfer device structures and functions.

An optimized one-sided split electrode TVF design that eliminates unnecessary common-mode electrode structure and minimizes non-linear depletion capacitance has been demonstrated; it dislodges the output circuit from the position of dominant noise source in CCD transversal filters.

These schemes have been combined in a one-sided DCS matched filter with demonstrated input-noise-limited performance. The filter provides an rms signal-to-noise ratio of 91 db, 0.6 percent total harmonic distortion, and a subtraction common mode rejection ratio of 68 db. With the elimination of clock pickup, output circuit requirements have been simplified.

ACKNOWLEDGMENT

The authors would like to thank C. L. Jiang, P. A. Nygaard and E. K. Shelton for many helpful discussions and design consultation; C. Ahyow is thanked for dedicated processing of the 2091 chip, and A. F. Gillam is thanked for help with device testing.

REFERENCES

1. W. S. Boyle and G. E. Smith, "Charge-Coupled Semi-Conductor Devices," Bell Syst. Tech. J., 49, pp. 587-598, Apr. 1970.

2. D. D. Buss, D. R. Collins, W. H. Bailey and C. R. Reeves, "Transversal Filtering Using Charge-Transfer Devices," IEEE Journal of Solid State Circuits, SC-8, No. 2, pp. 138-146, Apr. 1973.

3. C. M. Puckette, W. J. Butler, and D. A. Smith, "Bucket Brigade Transversal Filters," IEEE Transactions on Communications, Vol. COM-22, No. 7, pp. 924-926, July 1974.

4. M. F. Tompsett, "Using Charge Coupled Devices for Analog Delay," Proc. NELC CCD Applications Conference, San Diego, CA., Sept. 1973.

5. A. Ibrahim, L. P. Sellers, T. Foxall, and W. Steenaart, "CCD's for Transversal Filter Applications," Tech. Digest, IEEE Election Devices Meeting, Washington, D.C., pp. 240-243, Dec. 1974.

6. D. J. MacLennan, L. Mavor and G. F. Vanstone, "Technique for Realizing Transversal Filters Using Charge-Coupled Devices," Proc. IEE, Vol. 122, No. 6, pp. 615-619, June 1975.

7. D. D. Buss, W. H. Bailey and D. R. Collins, "Matched Filtering Using Tapped Bucket-Brigade Daley Lines, Elec. Lett. 8, pp. 106-107, Jan. 4, 1972.

8. J. A. Sekula, P. R. Prince and C. S. Wang, "Non-Recursive Matched Filters Using Charge-Coupled Devices," Tech. Digest, IEEE Electron Devices Meeting, Washington, D.C., pp. 244-247, Dec. 1974.

9. W. H. Bailey, D. D. Buss, L. R. Hite and M. W. Whatley, "Radar Video Processing Using the CCD Chip Z Transform," Proc. NELC Conf. on the Appl. of Charge Coupled Devices, San Diego, CA., pp 283-290, Oct. 1975.

10. J. B. G. Roberts and R. Eames, "A Swept Delay Correlator," Proc. NELC Conf. on the Appl. of Charge-Coupled Devices, San Diego, CA., pp 319-321, Oct. 1975.

11. R. W. Brodersen, C. R. Hewes and D. D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE Trans. on Electron Devices, Vol. ED-23, No. 2, pp. 143-152, Feb. 1976.

12. D. D. Buss and W. H. Bailey, "Application of Charge Transfer Devices to Communication," Proc. NELC Conf. on the Appl. of Charge Coupled Devices, San Diego, CA., pp. 83-93, Sept. 1973.

13. T. A. Zimmerman and R. W. Bower, "The Use of CCD Correlators in a Spread Spectrum Communications Example," Proc. NELC CCD Appl. Conf., San Diego, CA., pp. 141-146, Sept. 1973.

14. R. D. Baertsch and J. J. Tiemann, "Applications of a CCD Low-Pass Transversal Filter," Proc. NELC Conf. on the Appl. of Charge-Coupled Devices, San Diego, CA., pp. 251-256, Oct. 1975.

15. R. D. Melen and J. D. Meindl, "One-Phase CCD: A New Approach to Charge-Coupled Device Clocking," IEEE Jour. of Solid-State Circuits, SC-7, pp. 92-93, 1972.

16. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Rev. 33, pp. 327-343, 1972.

17. A. M. Mohsen, M. F. Tompsett and C. H. Séquin, "Noise Measurements in Charge-Coupled Devices," IEEE Trans. on Electron. Devices, Vol. ED-22, No. 5, pp. 209-217, May 1975.

18. C. H. Séquin and M. F. Tompsett, Charge Transfer Devices, Academic Press, Inc., New York, 1975.

19. D. D. Wen, "Design and Operation of a Floating Gate Amplifier," IEEE Jour. of Solid-State Circuits, Vol. SC-9, No. 6, pp. 410-414, Dec. 1974.

20. R. D. Baertsch, W. E. Engler, H. S. Goldbery, C. M. Puckett and J. J. Tiemann, "The Design and Operation of Practical Charge-Transfer Transversal Filters," IEEE Trans. on Electron Devices, Vol. ED-23, No. 2, pp. 133-142, Feb. 1976.

21. J. J. Tiemann, W. E. Engeler, R. D. Baertsch and D. M. Brown, "Intercell Charge-Transfer Structures for Signal Processing," IEEE Transactions on Electron Devices, Vol. ED-21, No. 5, pp. 300-308, May 1974.

22. J. E. Carnes, W. F. Kosonocky and E. G. Ramberg, "Free Charge Transfer in Charge-Coupled Devices," IEEE Trans. on Electron Devices, Vol. ED-19, No. 6, pp. 798-808, June 1972.

23. C. R. Hewes, "A Self-Contained 800 Stage CCD Transversal Filter," NELC Conf. on the Appl. of Charge-Coupled Devices, San Diego, CA., pp. 309-318, Oct. 1975.

24. M. F. Tompsett, "Surface Potential Equilibration Method of Setting Charge in Charge-Coupled Devices," IEEE Trans. Electron Devices, Vol. ED-22, pp. 305-309, June 1975.

25. C. H. Séquin and A. M. Mohsen, "Linearity of Charge Injection into Charge-Coupled Devices," IEEE Jour. of Solid-State Circuits, Vol. SC-12, No. 2, pp. 81-92, Apr. 1975.

26. Y. P. Tsividis and P. R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation," IEEE Jour. Solid-State Circuits, Vol. SC-11, pp. 748-753, 1976.

27. D. A. Sealer, E. N. Fuls, P. M. Ryan, C. H. Séquin, J. L. Statile and M. F. Tompsett, "A Dual-Differential Analog Shift Register with a Charge-Splitting Input and On-Chip Peripheral Circuits," IEEE Jour. Solid-State Circuits, Vol. SC-12, No. 6, pp. 633-637, Dec. 1977.

28. R. C. Henderson, T. Reiner and P. J. Coopen, "The Use of Submicrometer Electron Beam Lithography for Fabricating 4-kbit CCD Memory Arrays," IEEE Trans. on Electron Devices, Vol. ED-25, No. 4, pp. 408-412, April 1978.

29. G. R. Nudd, P. A. Nygaard, C. L. Jiang, "Application of Charge-Coupled Device Technology to Two Dimensional Image Processing," NELC Conf. on the Application of Charge-Coupled Devices, San Diego, Oct. 1978.