DEVELOPMENTS IN RADAR DOPPLER PROCESSING

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The capability of performing wideband spectrum analysis in real time using surface acoustic wave (SAW) chirp filters presents an opportunity to apply a single spectrum analyser to multiple channels of low bandwidth data using time-compression. This technique is particularly appropriate to pulse doppler radar in which each range gate presents a separate sampled data time series for analysis. Given the SAW spectrum analyser, the radar signal processing problem centres on the store used to acquire the sampled video, re-order it into time sequences from each range gate and output it in a highly compressed time scale. This "corner turning" store has been realized in both digital and CCD forms. The digital store has been built in two versions, one, for low bandwidth, is inexpensive but relatively slow, the second, for high bandwidth radars, is both expensive and power consuming. A new integrated CCD store has been designed to solve these problems, incorporating a new mode of clocking, using novel clock drivers and minimizing external pin connections. Results from all these configurations, in which both real and simulated radar data are analysed, are given. Conclusions on their relative merits in terms of real world constraints such as power consumption, size, complexity and clutter levels are drawn.

1 Introduction

We have previously[1, 2] discussed approaches to the problem of processing pulse doppler radar signals. The basis of these has been to accumulate samples of radar video, either in a CCD analogue store or in digital RAM, to re-order the samples into time sequences from individual range bins, and to serially output these sequences into a spectrum analyser serving all range bins. The commercial availability of fast spectrum analysers using surface acoustic wave (SAW) filters now readily allows this type of multiple channel, compressed-time spectrum analysis. The problem is thus reduced to the implementation of a flexible store capable of accepting samples at rates dictated by the radar parameters [pulse repetition frequency (prf) and range bin spacing] and outputting them in bursts matched to the time scale of the SAW analyser. This paper compares digital and analogue CCD implementations of the storage function aimed towards providing modules adaptable to a variety of radar requirements using a standard SAW analyser and describes in some detail a new CCD under development for this.

2 The SAW Spectrum Analyser

The number of resolvable doppler frequencies or time-bandwidth product of the coherent processing, is limited to the number of pulse echoes available from the radar targets. This is a function of prf, beamwidth and scan rate for a scanning radar, and the number of pulses per beamwidth rarely exceeds 100. Because of this we have used an analyser of nominal time-bandwidth product (TB) 100, it being a simple matter to under-use its capability for radars with a smaller number of hits on target. TB products exceeding 100 are obtainable by relaxing the $\pm$ 0.5dB flat response requirement. The actual SAW time and bandwidth parameters are of only secondary importance because T and B scale inversely under time compression, the product being invariant. For our analyser, T = 25 μs and B = 4 MHz. The SAW filters used of course operate at IF frequencies in the 20 to 30 MHz range but by internal single-sideband mixing the

analyser covers the band ± 2 MHz when presented with a dual channel, I and Q (in-phase and quadrature) baseband input. Time weighting is included to suppress spectral sidelobes to approximately -35dB whilst the overall dynamic range is about 40dB. This is sufficient for some radar situations but in cases where the clutter signal ratio exceeds these parameters, some pre-filtering will be necessary to reduce the dynamic range of the radar video.

3 Digital Storage

The digital store has 3 dimensions: the number of range cells x the number of pulses coherently processed x the data word length. For the 40dB dynamic range analyser, 8 bit words are sufficient and the re-ordering, or "corner turning" function is accomplished by appropriate input and output addressing of RAM under the control of range cell and pulse counters. The use of digital storage implies the use of A/D and D/A converters at the input and output (the SAW analyser being analogue) and when approaching and receding velocities are to be distinguished both I and Q channels must be stored.

Two versions of the digital store have been constructed to match differing system requirements. The first is appropriate to a relatively high resolution in range and doppler utilising the full TB capability of the SAW spectrum analyser. The range cell spacing of 22m specifies a range counter running at 7.5 MHz on 'write' while during 'read', 128 samples are output at 5.12 MHz. TTL control logic and fast NMOS RAM is therefore used together with bulky and power consuming A/D converters. For a 16-range cell system, 40W is consumed excluding the SAW analyser. The time compression factor of $\sim 10^3$ would allow several hundred range cells to be added before a second spectrum analyser became necessary. Figures 1 and 2 illustrate some on-line range-doppler displays photographed with this processor used with a meteorological research radar.

A second store has been built for a radar of lower range resolution and fewer hits on target. This used 16 ranges x 32 pulses x 8 bits, I channel only, with a range counter running at only 200 kHz. This allowed CMOS control circuits and RAM to be used together with compact low-power A/D converters consuming only 3W in total.

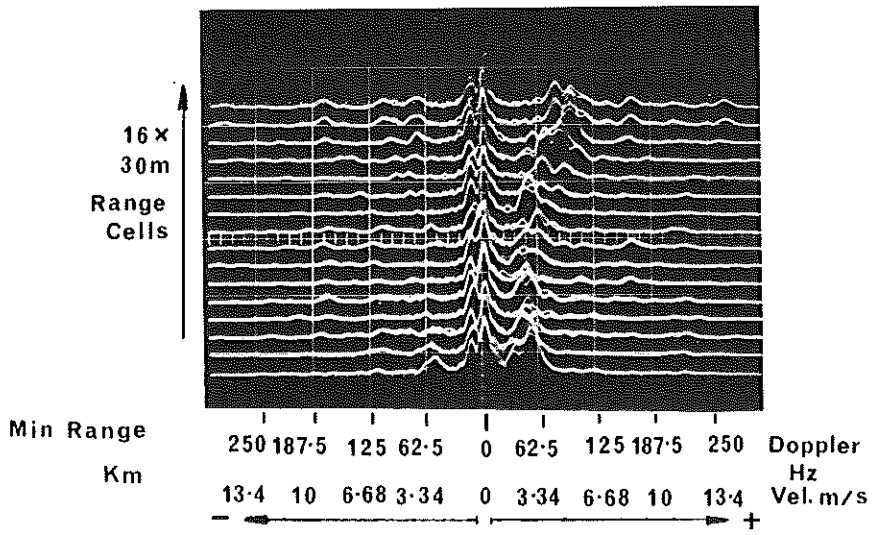


Figure 1 Range Doppler Display from meterological radar showing wind shear versus height/range.

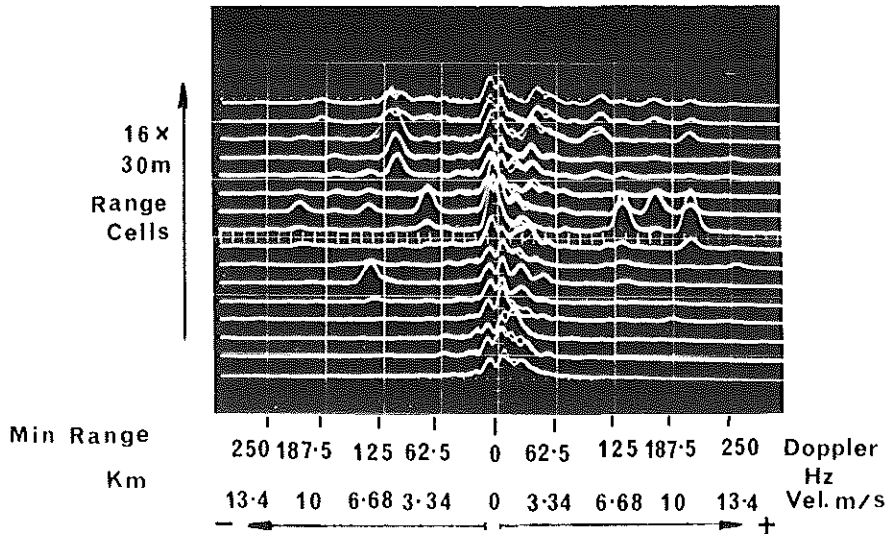


Figure 2 Similar display showing birds/ insects.

4 CCD Storage

The object in designing a CCD store is to produce a module structured to meet the radar problem but capable of adaptation to a wide range of radar parameters. A/D interconversions are avoided, an increasingly valuable feature for higher bandwidth radars. The number of range cells handled by the store module is a convenience factor only, dictating the number of modules needed in particular applications, whereas the pulse storage capacity should, like the spectrum analyser, match the highest TB product likely to be needed, eg 100, and the dynamic range should also at least equal that of the analyser.

Our first experimental CCD store was configured from discrete, already available devices: a 32-sample tapped delay line sampling the radar video in 32 range bins of 4 MHz following each pulse. 16 of the tap outputs were connected to each feed an orthogonal 100-sample linear CCD register clocked once per radar pulse to form I-channel time sequences from each selected range. These range bin stores were filled at a clock rate of 4 kHz (the simulated prf) and, when full, individually emptied at a 4 MHz rate to feed the SAW analyser. The layout of this system is sketched in Fig 3 and Fig 4 shows time-compressed ($\times 10^3$) waveforms and spectral outputs. This exploratory system of 16 range bins occupied a 30 x 35cm board and confirmed the expected difficulties in matching CCD gains and levels which would be multiplied for systems processing many range cells. However it allowed flexible control of the clock waveforms, for instance, to interleave the input and output functions to minimise the hold time when the signal is most liable to corruption by dark current, and established the feasibility of the CCD approach.

To implement these functions onto one chip requires (1) a register which takes in the radar data at a rate of 4 MHz (2) a sideways transfer structure which operates at $\leqslant 1/R$ of this rate where R is the number of range cells (3) a storage section implemented in the same fashion as the slow transfer part of an SPS structure and (4) a means of reading out each of the parallel channels individually and independently at a rate of 4 MHz, with a minimum of external peripheral circuitry.

The serial to parallel structure of an SPS array achieves (1) to (3) of these requirements, but in these structures the data cannot be read out of the parallel channels independently. We have adapted this type of structure into a new type of storage module. In our structure the phases 1 and 3 clocks in the parallel section of the

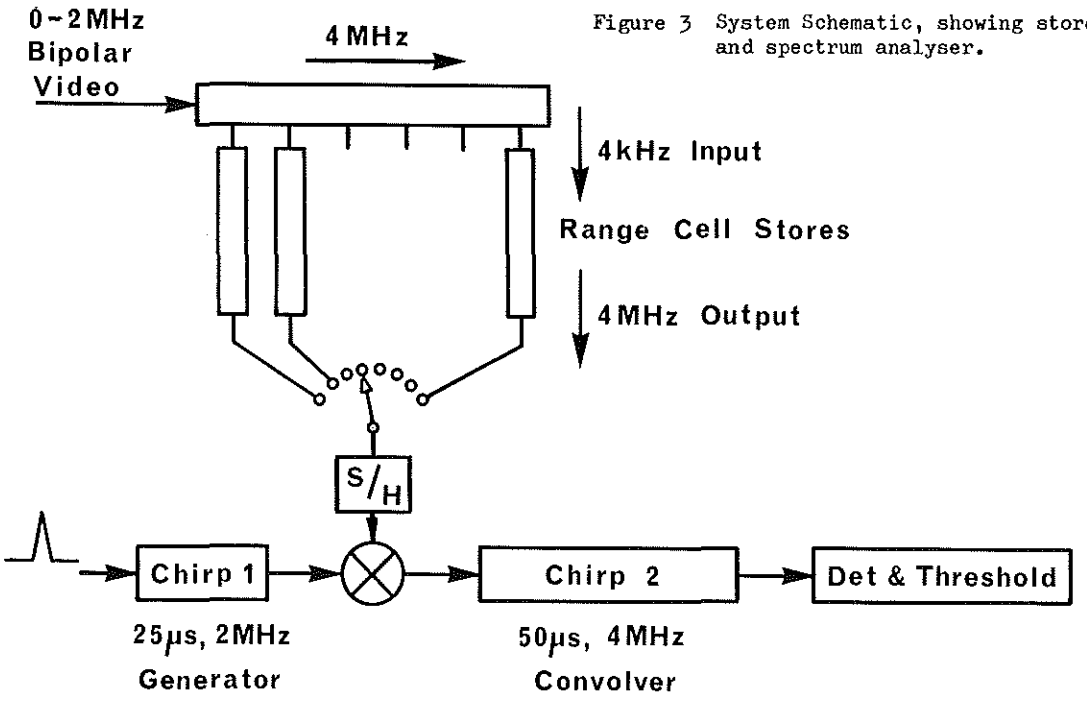
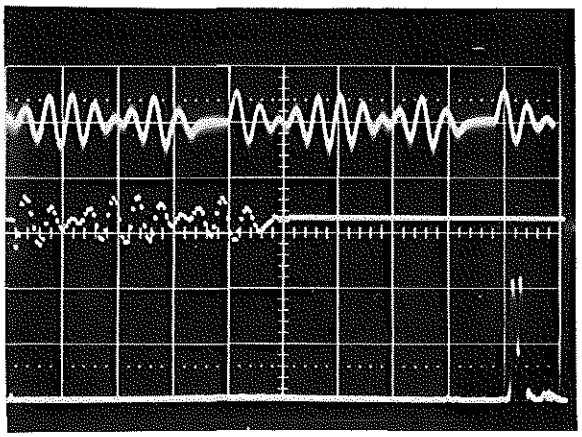


Figure 3 System Schematic, showing store and spectrum analyser.



Top trace: video, 5ms/div containing 400 Hz and 500 Hz components

Middle trace: time compressed video, 5μs/div

Lower trace: spectrum output 5μs/div or 800Hz/div

Figure 4

array (ϕ_{1P},ϕ_{2P}) Fig 5 are common to all the parallel sections. The phase 2 clocks (ϕ_{2nP}) are brought out individually to pads around the chip periphery. In contrast to an SPS structure, an output transfer gate common to all parallel channels feeds all channels into a common output amplifier. Fig 6 is a chip photograph, of a 16 x 128 bit version.

The input to this device operates in a conventional way, whereby the parallel clocks ϕ_{nP} are clocked with the input register clocks ϕ_{nS} to fill the array with data, the parallel clocks operating once each time the serial register is filled by R input clock cycles, corresponding to R range gates.

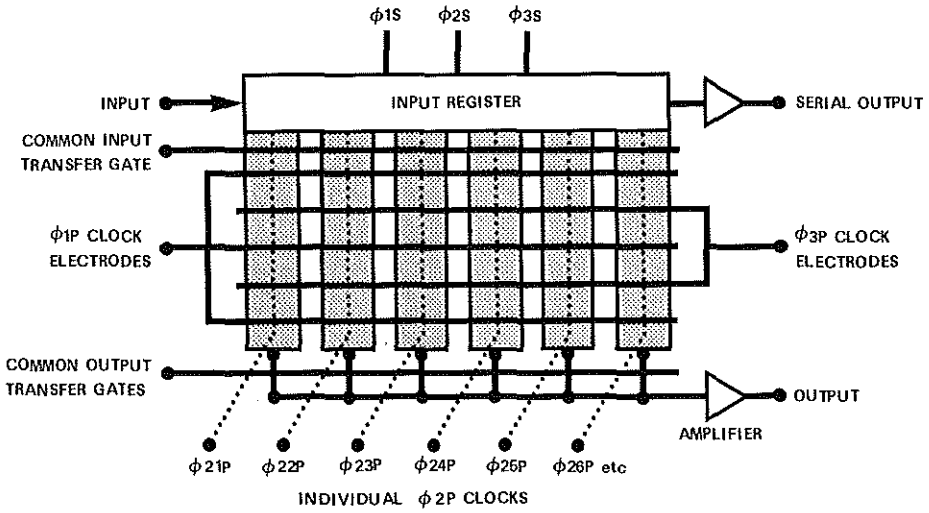
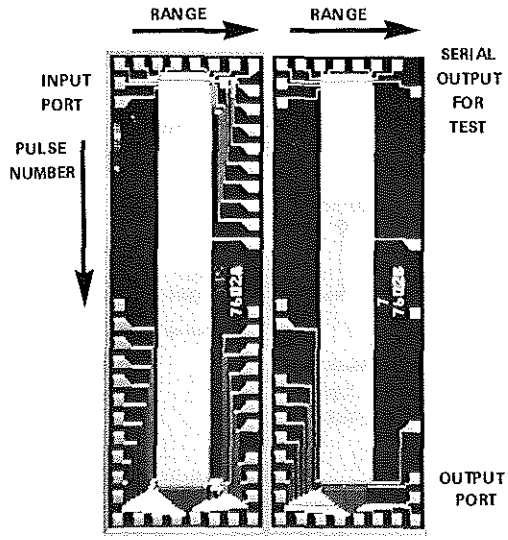


FIGURE 5

After P clock cycles, where P is the number of pulses to be analysed, the array is full of data. At this point the logic system associated with the parallel clocks switches the clocks to a new mode of operation. All parallel clock electrodes, save one, are driven to a high potential, up to twice the parallel clock swing. In the deep wells so formed, the charge held under every phase 2 electrode remains under these electrodes independent of the state of the phase 1 and 3 clocks. The desired range channel is clocked normally, together with the ϕ_{1P} and ϕ_{3P} clocks to read that channel out independently to the common output circuit, at 4 MHz, and so to the SAW analyser. The phase 2 clocks are then switched one by one in sequence to normal clocking, while all the others are held high. Thus the individual range cells are read at high speed in sequence to the SAW analyser.



ACTUAL CHIP PHOTOGRAPH OF 16 RANGE x 128 PULSE CHIP IN TWO VERSIONS
(a) WITH AMPLIFIERS
(b) WITHOUT AMPLIFIERS

FIGURE 6

Fig 7 illustrates the surface potentials for such a clocking scheme, where V_D is the deep well potential and V_C the normal clock potential (assuming for simplicity of explanation that ϕ_S, the surface potential, equals the applied voltage). During normal slow input clocking the three parallel phase clocks are run normally, all individual channels being clocked together. On readout one channel only clocks (rapidly) in the normal manner, while in the rest ϕ_{2P} is held high. No matter how ϕ_{1P} and ϕ_{2P} behave no forward or backward motion of charge occurs in these channels. In the actual device there is more complex timing of the sideways transfer into the parallel channel than has been suggested simply to ensure rapid initial sideways transfer of charge into the parallel array.

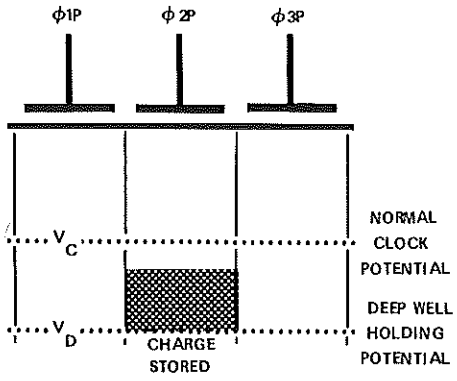


FIGURE 7

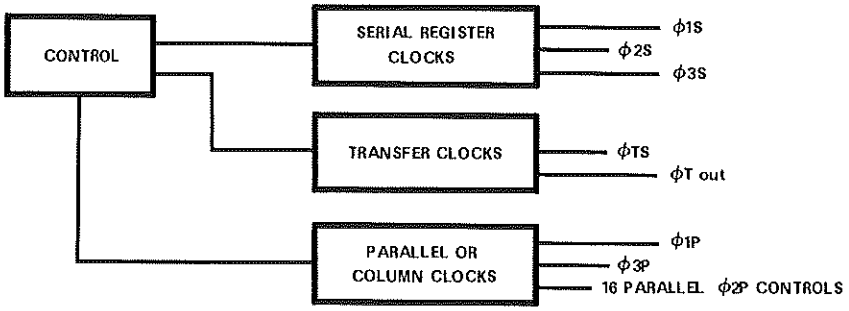


FIGURE 8(i) SYSTEM CONTROL

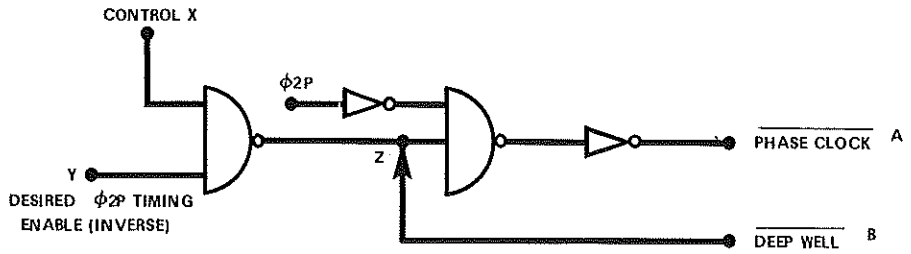


FIGURE 8(ii) SECTION OF LOGIC CONTROLLING ONE DRIVER

In order to drive and time the store in this way, appropriate novel three level clocks had to be designed and these are described in the next section.

5 System Control Logic

The control logic for the system is presently implemented in TTL using approximately 20 chips. It could currently be implemented in a ULA package or, indeed, designed directly onto the same chip as the drivers; packaging the whole with the CCD in a hybrid. Ultimately it could all be implemented on a single chip.

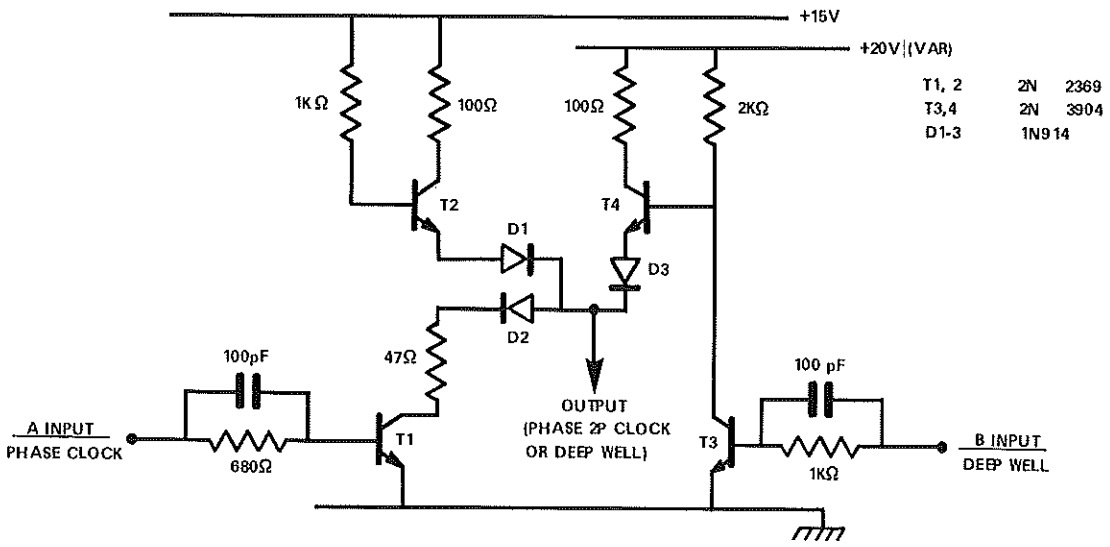


FIGURE 8(iii) DRIVER CIRCUIT

The basic control system is shown in Fig 8 wherein the serial register clocks, the transfer clocks and the parallel or column clocks are timed to read in data at a rate matched to the radar output, and to read out the data from each channel in sequence, at high speed, to the SAW spectrum analyser. The basic system timing can be arranged to either (i)read in data into the store until it is full, then read out each channel sequentially to the analyser or (ii) with a minor reconfiguration read out one or more channels between each radar return. This obviates a duplicate store operating in 'ping-pong' and minimises dark current effects. In addition (iii) since the read-in and read-out of data are separately controllable, and the chip configuration so arranged, having a transfer gate between the serial input register and the storage/read-out section, both the acquisition of data and the read-out from any channel or channels, can take place simultaneously without interference. Thus the chip itself and the control logic and driver system form a versatile module which can be used with various timing configurations to suit the radar system in use.

6 The Special 3-Level Clock Driver Circuit and its Operation

The driver circuit (Fig 8 (iii))is controlled by TTL level signals. The circuit gives out 15 volt clock waveforms or variable (typically 20 volt) deep well pulses according to the control signals from the control circuit 8(ii). The choice of deep level pulse amplitude is a compromise between signal handling and low dark current. These circuits have to drive the CCD store in one of two modes, (a) slow accumulation of data or (b) rapid read-out of one channel at a time. During (a) the control line X is asserted low, giving high output at Z. This causes the final output A to be asserted, which in turn gives a normally clocked output from the driver circuit (iii). This occurs simultaneously on all 16 driver circuits so that the store accumulates data. When the store is full condition (b) is invoked. On 15 channels at any given time output Z, which goes directly to input B of the driver circuit, gives a deep holding well on all 15 channels. On the sixteenth channel, selected by the logic pulse applied to input y, provided the input X is also

enabled by the general read-out system control pulse, the circuit gives an output A to the selected driver, causing that individual channel to be read out.

This special driver circuit, which could of course be used also in a 2 or 4 phase implementation of the device structure, has been tested to over 10 MHz clock rate. A number could easily be hybridized in a very small package, eg 8 in a package 2.5cm x 5cm. If the logic were to be implemented in a ULA, the whole system including the CCD would only take 4 packages, on a small board.

7 Results From the CCD Corner Turning Store

The principle of three level clock driving was initially established by driving a separate normal 32-bit linear device by the novel 3-level clock drivers developed for the pulse doppler chip. Using phase referred input[4] (referring the input diode to ϕ_1) requiring no extra 'fill and spill' pulses and automatically sampling at the correct time periods, together with the clocking scheme described above, the output shown in Fig 9 was obtained, the ϕ_2 clock being held high at DC≈30% above V_C for several milliseconds in this case. The phase 1 and 3 clocks were clocked at 1 MHz continuously, and the phase 2 clocks at 1 MHz when not at the deep well holding value.

In each output burst the first section of the data has been held in the device by the high ϕ_2 clock, held high during the 2 mSec period between outputs, with ϕ_1 and ϕ_3 running continuously. The second output portion of each burst was the normal output from the device, appearing 32 bits after the re-starting of the normal ϕ_2 running period. In a large store of course, the high clock storage period needs to be much greater, typically

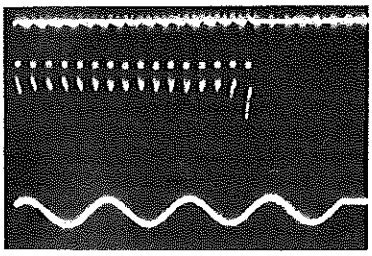


FIGURE 10

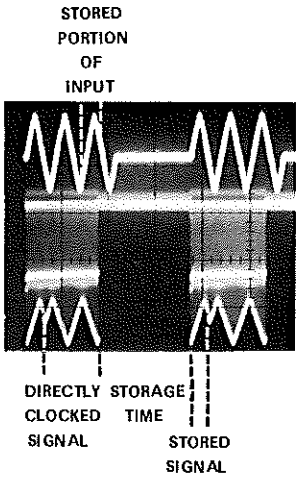


FIGURE 9(i)

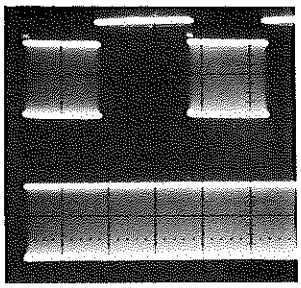


FIGURE 9(ii)

25-50 mSec, but still well within the dark current capabilities of this device.

Operation of a 16 range-cell by 32 pulse corner-turning processor of the type described earlier and shown in Figs 5 and 6 may most easily be illustrated by the input of repeated bursts of 1 kHz sine-wave data simulating a radar doppler signal at 1 kHz in every range cell, as shown in Fig 10. In this mode of operation read-in and read-out of data take place simultaneously. Read-in is at approximately 1 MHz. Fig 10 also illustrates how a dark current problem may show up - the 16th output channel of this particular device suffers from excessive dark current accumulation during the 20 mSec high-clock storage period before read-out, showing up as an excessively high output signal. In this figure the input and output signals are illustrated to the same timescale. Parallel transfer is at 4 kHz and read out at 1 MHz.

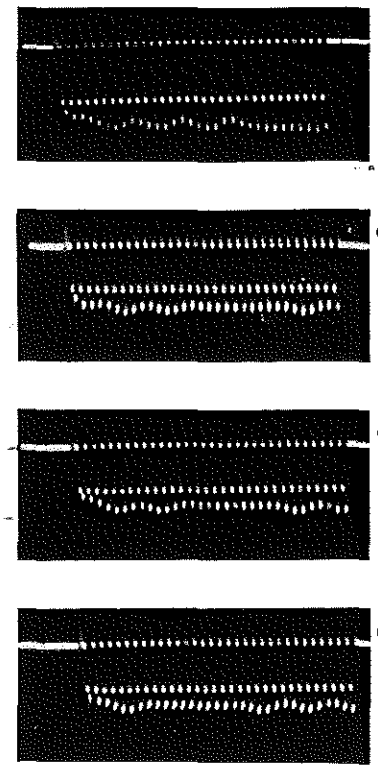


FIGURE 11 TYPICAL OUTPUTS

The data in each parallel channel is accumulated from 32 separate bursts of input. Each input is slipped slightly in time with respect to its predecessor so that in each parallel channel successive data points along the input waveform are taken just as would be the case with real radar data. Thus over 32 input bursts each storage channel (range bin) accumulates a history incorporating (in this case) a 1 kHz doppler signal. Due to this method of input each channel is slightly displaced in time with respect to its neighbours, leading to the outputs from channels 1, 6, 9 and 14 chosen by way of example, and shown in Fig 11 (i) to (iv). In (i), channel 1, the samples start from the beginning of the burst and include a lot of the dead time between the input bursts, at the right side of the picture. In (ii), channel 6, samples from both dead and active time are shown, as is the case in channels 9 and 14 (iii) and (iv), comparison between these pictures illustrating the slippage of sampling points from channel to channel in this mode of operation. On real radar data of course, there would be vastly different doppler signals from channel to channel unlike this simple illustrative simulated data. Finally Fig 12 shows the effect of overly large high-clock voltage; (i) shows normal operation using a high-clock DC value of 40% above normal clock voltage; in (ii) the DC high clock is increased to 2 x the normal clock voltage, which this particular channel cannot handle without dark current problems.

In summary then the pulse doppler corner turning store problem has been solved in a new way, using the 3-level clock principle for the first time to enable read-in and read-out from the store simultaneously at different rates in a complex manner with a minimum of external connections to the chip. The high-clock storage principle is as equally applicable to 2 phase or 4 phase structures. The new three level clock and logic design makes implementation easy and meagre in power consumption. Implemented in CMOS the whole system, operating at 4 MHz output for the SAW analyser will consume less than 2 watts in total.

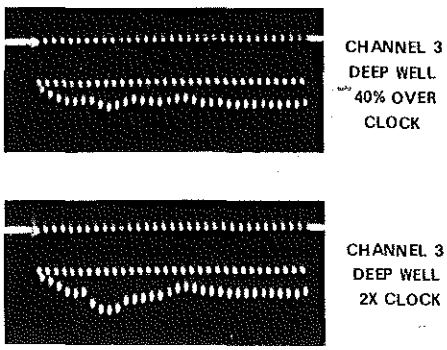


FIGURE 12 OUTPUT SHOWING STORAGE TIME EFFECTS

8 Conclusion

The applicability of a single wideband spectrum analyser to the multichannel narrowband radar doppler processing problem has been shown. In many cases the interface is conveniently made using a digital store. However for wideband radars, and when power consumption and size are controlling factors it appears that CCD storage will be increasingly attractive, partly through its avoidance of multi-bit storage per sample and partly through dispensing with A/D interconversions. This promise will only be realised through the development of a specially configured CCD storage module requiring a minimum of control connections and adaptable to differing radar bandwidths and prfs.

The new clock and device configurations we have described represent an advance towards this module. The logic and drivers for the CCD clocks are capable of integration to minimise power and size. The storage modules may be chained together (by staggered clocking which avoids signal degradation through inter-CCD transfers) to meet the range-bin requirement of particular radars.

The principle limitation of the all-analogue approach is probably the dynamic range of ~40dB. This prevents its use in strongly clutter dominated situations unless the processor is preceded by a clutter filter. However a digital or analogue 3 or 4 pulse canceller will often be sufficient to allow very high speed analogue spectral processing to replace digital FFT methods. The advantage of course increases with the number of resolved doppler frequencies and ranges. A feature of this processor is its ready applicability to jittered-prf radar. By reproducing the jittered timing of samples in the compressed-time output of the store, the required ambiguity function is preserved. The SAW spectrum analyser operating in continuous time handles this naturally whereas the discrete, equally spaced sampling necessary to FFT processing cannot.

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