A COMPLEMENTARY CCD/SAW RADAR SIGNAL PROCESSOR

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ABSTRACT: In recent years the size, weight, power, and cost factors of radar equipment have escalated sharply as the result of a demand for a greatly expanded operational capability. Multimode operation, enhanced resolution, improved detection capability, etc., have increased signal processing equipments to the point that neither evolutionary improvements nor innovative circuit designs and packaging techniques may provide practical solutions for implementation. Instead, step improvements must be made by finding new technological approaches to supplement or replace the conventional means of implementing desired functions. The charge coupled device (CCD) and surface acoustic wave (SAW) device technologies offer the opportunity of making such a step improvement in the size, weight, power, and cost of a radar doppler processor.

INTRODUCTION

Based upon the realization that a radar processor concept such as that contemplated utilizing CCDs is at least five years away from field deployment, a rather aggressive set of performance parameters were postulated as summarized in Table 1. The anticipated processor application is a high resolution airborne radar system capable of both search and track modes of operation.

Modes	Search & Track
Range Resolution	15 m
Range Sampling Factor	1.25
Range Bins	1000 Search 500 Track
Doppler Resolution	64 Points
PRF	Staggered
Dynamic Range	50 dB

Table 1. Basic Radar Characteristics

ARCHITECTURAL TRADE-OFFS

In an attempt to capitalize on the attendant size, weight, and power advantages of CCD based analog signal processing for an advanced, high performance, multimode radar processor, two basic configurations were carefully evaluated as summarized in Table 2. The two approaches evaluated were the range gated CZT bank approach[1] of Figure 1 and the corner turning memory/CZT approach[2,3,4] of Figure 2. The retention of phase information necessary to perform tracking using conventional monopulse radar techniques[5] becomes a significant factor in the architectural trade-offs. This requirement is particularly significant with respect to the range gated CZT bank approach since the "sliding" CZT[6] is no longer applicable. Additionally, this approach, while performing signal storage and convolution simultaneously within the CCD, is redundant in its storage of the in-phase (I) and quadrature (Q) signal samples. Therefore, the performance of a mathematically rigorous N point CZT requires approximately 8N CCD storage locations and provides a 50% duty cycle.

The corner turning memory (CTM) configuration which is architecturally similar to the conventional digital approaches requires only 2N storage locations to perform an N point complex transform with a 50% duty cycle. Calculation of an N point transform over M range bins with 100% duty cycle using "ping-pong"

Characteristics	MAGNITUDE ONLY		MAGNITUDE AND PHASE	
	RANGE GATED CCD CZT	CCD CTM SAW CZT	RANGE GATED CCD CZT	CCD CTM SAW CZT
Range Resolution	$c/2f_R$	$c/2f_R$	$c/2f_R$	$c/2f_R$
Doppler Resolution	PRF/N	PRF/N	PRF/N	PRF/N
CCD Data Rate	PRF	f_R	PRF	f_R
Duty Cycle	100%	50%	50%	50%
CCD Storage/Range Bin	4 N	2 N	8 N	2 N
Range Bins/CCD Chips	5	32/2	5	32/2

Table 2. Comparison of the Range Gated CZT and CTM/CZT Radar Processor Architectures

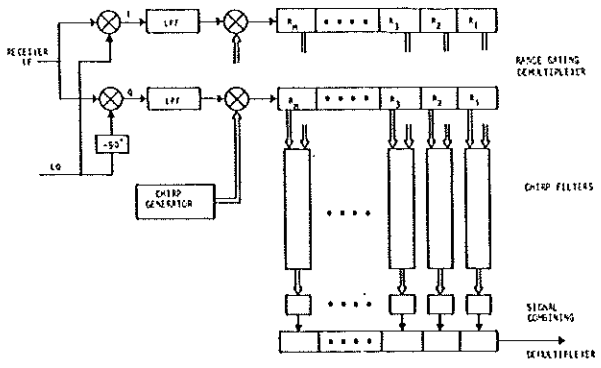


Figure 1. Range Gated Pulse Doppler Processor Utilizing the CZT.

techniques will require 16 MN storage locations for the range gated CZT approach and 4 MN locations for the CTM approach.

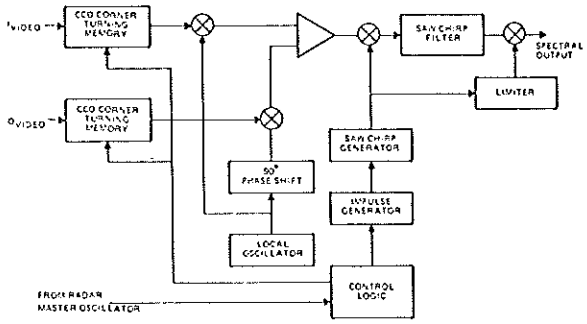


Figure 2. Radar Processor Architecture Using CCD Memory and SAW CZT

Either of the two approaches appears to provide adequate dynamic range. The range gated CZT processor's dynamic range is limited by the associated amplifier and/or multiplier circuitry. The wide bandwidths and attendant clock feedthrough difficulties will limit the achievable dynamic range of the CTM.

Operating speeds, power, and operational difficulties of the two approaches represent key issues which almost defy analysis. The range gated CZT architecture, which demultiplexes the signals into M parallel paths which are clocked at the PRF, provides the lowest CCD data rates. The CTM approach, in general, requires CCD data rates approximately equal to the range resolution (or sampling) rate, $f_R = c/2\delta_R$, where c is the speed of light and δ_R is the range resolution, which is normally commensurate with the radar's video bandwidth. However, the operating speed limitation in both cases is the multiplexer/demultiplexer circuitry which, due to system integration considerations, must be integrated on-chip with either processor configuration and must operate at the range sampling rate, f_R.

Power dissipation requirements based upon simple CV^2f considerations for the CCDs alone indicate the requirements for the CTM approach are 1/4 that of the range gated CZT approach if all unambiguous range bins are processed and equivalent if 1/4 of the unambiguous range bins are processed. This conclusion is based upon the clocking of 2N stages at f_R for the CTM and 8MN stages at the PRF for the range gated CZT. The power dissipation for both cases will be dominated by the clock requirements for the multiplexer/demultiplexer circuitry. Amplifier and other signal conditioning circuitry power requirements will, in all likelihood, exceed the theoretical CCD clock power requirements. Thus, based upon the system requirements outlined in Table 1, the two processor configurations are comparable in terms of power requirements.

The key considerations related to the choice of a system configuration are the cost and complexity of eventual system construction and integration. Cost is primarily influenced by the quantity and complexity of the ICs employed. Compared with the CTM, the range gated CZT IC is more complex and may be expected to exhibit a lower yield. Furthermore, due to the redundant data storage and additional circuitry components, a larger number of range gated CCD chips will be required (a factor of 3 to 6 is anticipated), thereby increasing system complexity. Although the CTM approach requires the additional investment in the surface acoustic wave chirp transform unit,[7,8] this technology is quite mature and the cost tradeoff appears reasonably favorable.

The combined CCD CTM/SAW CZT approach was, therefore, appraised as exhibiting the most promising overall cost/performance potential for the proposed high resolution, multi-mode processor, and a program to develop the required components was initiated. It should be pointed out that, for processors not requiring phase information, the range gated "sliding" CZT still represents a viable option due to its 100% duty cycle with its storage requirements of 4N samples. The remainder of this paper describes the component development and compares observed performance with design goals. In addition, preliminary results on a new CCD CTM configuration are presented.

CTM TRADE-OFFS

The CTM can be configured into N delay lines of length M or into M delay lines of length N as shown in Figures 3 and 4 respectively. In the former case, returns for sequential PRIs are loaded into sequential delay lines at the range resolution rate until all N delay lines are filled. Thus each delay line corresponds to range swath returns for a particular PRI. Locations within the delay lines correspond to range bins. The N samples from a given range bin are then sequentially read from the outputs of the delay lines at a rate commensurate with the CZT analysis bandwidth (i.e., B/N). The latter configuration loads a sample into each delay line once each PRI. Thus the contents each delay line correspond to returns from sequential PRIs for a particular range bin. The contents of each delay line must be sequentially read at a rate equal to the spectral analysis bandwidth, B, while the contents of the remaining delay lines are statically maintained.

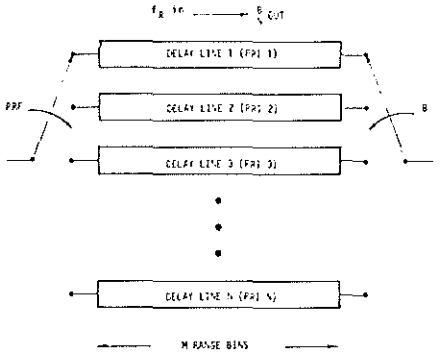


Figure 3. Serial In/Parallel Out CTM Configuration.

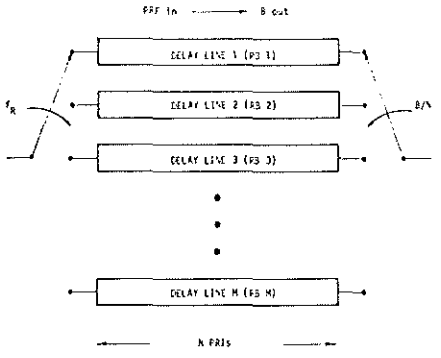


Figure 4. Parallel In/Serial Out CTM Configuration.

Therefore, the former configuration requires high speed CCD transfers for read-in while the latter requires high speed read-out transfers. Also since N is usually much less than M, CTE effects are less pronounced with the latter configuration.

Further consideration of the partitioning of the CTM indicates some potential advantages with respect to memory utilization may be accrued by partitioning the memory into square arrays. Proper design of the memory timing will permit each square array to be switched between the two configurations discussed above permitting simultaneous loading and unloading of the array which results in 100% memory utilization. Simultaneous data loading and unloading implies equal input and output data rates which further implies that the CZT spectral analysis bandwidth, B, must be equal to the range resoluton rate, f_R. This constraint may be avoided at the cost of additional input/output buffers and/or more complicated memory timing considerations.

An attractive alternative to the line addressable memory concept for implementation of the CTM is the two dimensional charge transfer structure[9] to be discussed in detail in a later section. The complexity of the design was considered to be a significant risk factor for this development and has been pursued under a separate program.[10]

CCD CTM IMPLEMENTATION

Based on the previously discussed architectural considerations, a processor brassboard has been developed based on the configuration illustrated in Figure 2. The I and Q components of the radar video are to be derived from a synchronous detector in the radar receiver and stored in separate memory (range store) modules. Each module consists of a number of 66x66 cell CCD memory blocks required to accommodate the range swath of interest. For the brassboard, two blocks per module were employed, although this is expandable to allow the desired coverage of the radar pulse interval. Thus the range stores in the brassboard can accommodate 132 range bins (I and Q) collected over 66 PRIs in the search mode and 66 range bins (I and Q for both Σ and Δ channels) over 66 PRIs in the track mode.

The range stores are emptied at a 12.5 MHz rate into I and Q up converters to generate single sideband doppler information at a 318 MHz IF for subsequent spectral analysis by the 64 point SAW CZT module. (The use of 66 cells in the range stores allows 2 "burn-pulses" for settling of transients before spectral analysis is initiated). The SAW CZT module

consists of two complex CZT channels which are commutated by processor timing to allow continuous system operation. The use of the complex CZT realization is required to maintain the desired phase information.

The organization of the CCD memory chip is illustrated by the block diagram in Figure 5. The configuration shown consists of sixty-six 66-stage CCD delay lines and the circuitry required to address individual input and output terminals on a line-by-line basis. The corner turning operation is performed by sequentially switching between a parallel mode in which consecutive samples are read into and out of consecutive delay lines, and a serial mode in which consecutive samples are read into or out of one particular delay line.

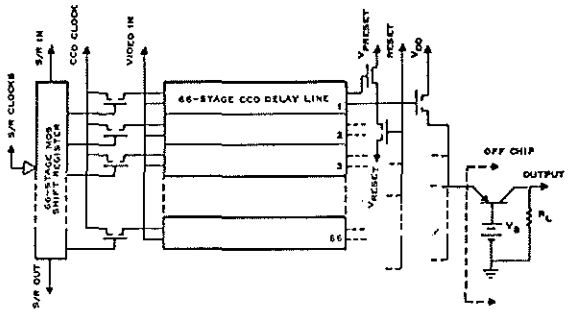


Figure 5. Block Diagram of Sequentially Line Addressable Memory Chip.

The design approach used in the range stores is based on the two phase CCD structure which can be realized with the double level polysilicon gate process developed at TI. These delay lines are operated in the so-called "phase and one-half" mode in which one set of gate electrodes is clocked while the other is maintained at an intermediate DC level. By properly designing the output circuit, the charge transfer and sensing operations can be controlled with a single clock pulse. When the CCD clock is off, the signal charge is stored in ion implanted potential wells beneath the non-clocked electrodes.

The efficacy of this structure is that it makes it possible to manipulate the data samples in the memory by enabling a single clock signal to the desired CCD delay line. All the delay line input terminals and output terminals can respectively be connected in parallel since charge is transferred into or out of a particular delay line only if its clock is enabled. Since the addressing required for the corner turning operation is always sequential (i.e., line m + 1 is always addressed after line m, unless a reset to m = 1 is required) the addressing function is implemented using a digital shift register operating synchronously with the CCD clock rather than the address decoder circuits typical in random access designs.[11] Thus, the memory is not randomly line addressable, but rather is referred to as "sequentially line addressable."

In the parallel mode the shift register clock operates at the same rate as the CCD clock with a logic "1" entered at the shift register input at the start of each radar pulse interval. In the serial mode, the shift register clocks operate at 1/66 the CCD clock rate with a single "1" entered at the start of the serial cycle. Thus the digital shift register must be capable of operating at the maximum data rate required of the memory and must also be able to retain a logic "1" in each cell for a large number of clock periods in the serial mode. Further, it is necessary to interface some type of switch to the shift register structure in order to enable the CCD clock line. All of these requirements are met with a dynamic MOS digital shift register which is implemented on chip with the CCD delay lines.

Referring to Figure 5, a logic "1" is entered at the input of the 66 stage MOS shift register and propagates through the structure sequentially addressing MOS switch transistors which couple individual CCD clock lines to the CCD clock busses. Serial or parallel oper-

ation is determined by the shift register clock rate. Signal charge is transferred down the CCD delay lines and detected at individual output circuits which include an additional reset switch whose operation will be described later. The commutating shift register is a standard dynamic MOS ratio-less configuration with an additional transfer switch connected to the CCD clock switch transistor which operates in a bootstrap mode.

The CCD delay lines are each 66 stage buried channel devices having 6 mil (152.4 μm) channel widths and 0.6 mil (15.24 μm) gate lengths. The input circuits are dual gate surface channel configurations and can be operated in either the "diode cutoff" or "potential equilibration" mode. The buried channel is coincident with the edge of the implanted well under the first clocked electrode.

In order to preserve dynamic range at the clock rates required, it was determined that each delay line should have an individual source follower output transistor. Furthermore, power dissipation requirements dictated that each output transistor should be turned off when not in use. This was accomplished with an additional reset transistor at the output of each delay line and the use of external current summing in the output circuit. As indicated in Figure 5, all output nodes are tied in parallel and connected to the emitter of a PNP common base current summing amplifier. The value of V_B sets the voltage at the emitter and hence the common output node voltage. This is adjusted such that the preset level at the output diode of the currently addressed delay line is sufficient to turn on its respective source follower.

The collector current of the summing amplifier then follows the drain current of the output follower and is sensed by R_L. Coincident with the operation of the shift register, a reset pulse is applied to the gate of the additional reset transistor. This pulls the output diode voltage at all delay lines down to V_{reset} which is adjusted to a level below the emitter voltage of the summing amplifier ($V_{reset} = V_B$ is sufficient) thereby turning off all output source followers. The next preset operation turns on the output circuit of the next delay line, and the output voltage follows the source follower drain current until the next reset pulse occurs.

This output scheme results in an excessive fixed pattern noise component observed during the parallel mode due to threshold voltage variations among the individual output circuits. In the serial mode, however, it results in DC level shifts between consecutive output data sequences which may be removed by subsequent filtering. Consequently, only the serial mode output can be utilized, and two units are multiplexed such that simultaneous read and write operations are possible in each memory block.

Figure 6 is a photomicrograph of the completed memory chip. Due to size limitations, the structure is composed of thirty-three 66-stage shift register addressed delay lines. An integral source follower is attached to the last stage of the shift register in order to couple it to a second bar thereby forming the full 66 x 66 memory array. The dimensions of the chip are 156 mils by 293 mils (3.96 mm x 7.44 mm).

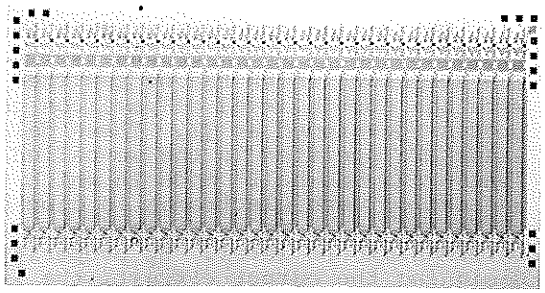


Figure 6. Sequentially Line Addressable Memory Chip.

Figure 7 illustrates the operation of two interconnected memory chips performing time compression of an analog test signal at a 12.5 MHz clock rate. The top two traces are, respectively, the test signal and memory output (before sample and hold) on the same time scale. The test signal is sampled during the parallel mode which can be differentiated from the serial mode by level variations in the latter due to threshold voltage variations.

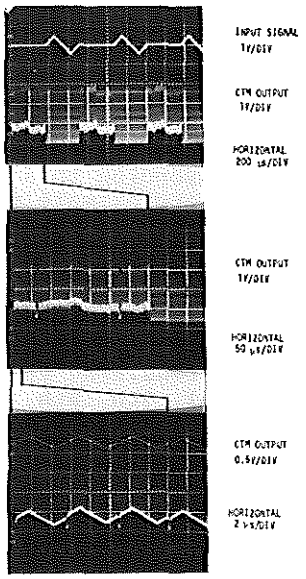


Figure 7. Sequentially Line Addressable CTM Operation at 12.5 MHz

Due to the organization of the memory it is not possible to make direct measurements of charge transfer efficiency (CTE) and dynamic range of the CCD delay lines. Instead, a separate CCD test structure was included on the chip in order to make meaningful measurements. Using this test structure the CTE was found to be 0.999 with the dynamic range in excess of 50 dB.

Clock waveforms for the commutating shift register and CCD delay lines were generated with standard Schottky TTL logic elements. The required clock drive levels were obtained with discrete clock drivers using medium power VHF transistors. Each 66 x 66 memory block (4 chips) dissipates approximately 15 watts, of which 12 watts are dissipated in the clock drivers with the remainder in various amplifier, switching, and control circuits.

SAW CHIRP Z TRANSFORM

The SAW CZT module utilizes a dual channel 64 point chirp Z transform to process the doppler information. A block diagram of the SAW CZT module is shown in Figure 8. In operation the in-phase and quadrature baseband doppler signals from the range stores are mixed with appropriately phased 318.75 MHz carriers to produce an IF signal that can be accommodated by the transform processor. The two channels of the processor are multiplexed in such a manner as to provide continuous processing, in 5.12 s time segments, of the time compressed and up converted video.

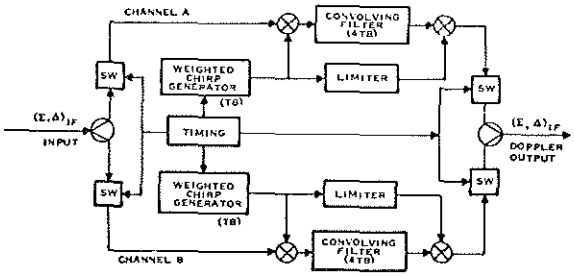


Figure 8. SAW CZT Module Block Diagram.

Operation of the SAW CZT is conveniently described by the frequency-time diagram shown in Figure 9. As a 5.12 µs data burst is switched into one channel, it is mixed with a synchronized linear FM down chirp having a 12.5 MHz bandwidth and 5.12 µs of dispersion about a center frequency of 175 MHz and weighted with a Dolph-Chebyshev function.

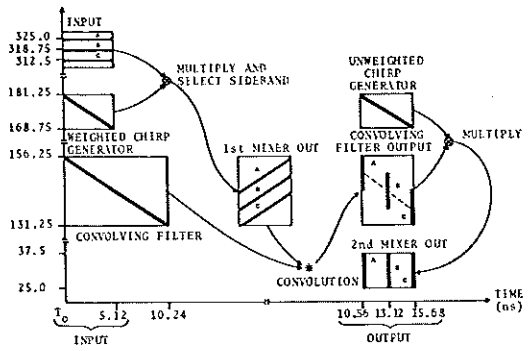


Figure 9. Frequency Versus Time Operation of CZT.

Note that the mixer output must be linear with respect to either input over a dynamic range which is the sum (in dB) of the dynamic range of the input signal and that of the weighting function. The lower sideband mixer product has a chirp sense opposite that of the premultiply chirp and is applied to the input of the compression filter which is a down chirp having 25 MHz bandwidth and 10.5 μs of dispersion about a 143.75 MHz center frequency.

Both of the SAW filters are constructed using a slanted transducer configuration on ST-quartz.[12] One major advantage in utilizing this configuration for the transducers in a pulse compression system is that the various frequency portions of the transducer are spatially separated and can be amplitude and phase compensated to minimize time sidelobes.

The compressed pulse output from the compression filter is then post multiplied with the chirp from the premultiply filter that has had the weighting removed by limiting. This process is facilitated by including a proper amount of flat delay in the compresson filter so that the filter output aligns with the synchronous post multiply chirp to produce a fixed output frequency of 31.25 MHz from the post multiplier.

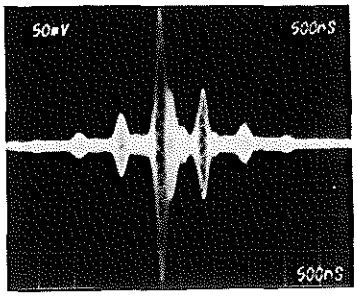
The SAW CZT module exhibits in excess of 60 dB dynamic range (peak signal to noise floor) with a power dissipation of 16 watts. It appears possible to achieve 80 dB dynamic range with an optimized design. Sidelobe levels fall below 40 dB at frequencies two to three doppler bins removed from an analyzed signal. The nearer sidelobes were only suppressed 26-30 dB due to pattern generator difficulties.

SYSTEM TEST RESULTS

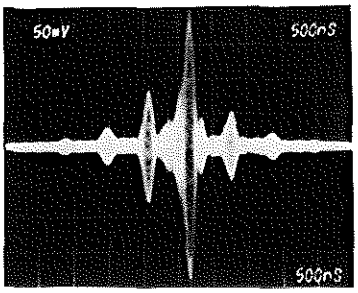
Preliminary system tests were performed using a partial range store (one 66 x 66 memory block, half used for the in-phase channel and half for quadrature) and a complete SAW CZT module. The repetition interval was 5.28 μs corresponding to a doppler resolution of approximately 3 kHz. Figure 10 illustrates the response due to a complex input signal consisting of a 6 kHz square wave applied to the in-phase channel with a similar waveform delayed by ± one quarter of a period applied to the quadrature channel. The resulting spectra with the fundamental, 5th, 9th, and 13th (barely visible) harmonics in one sideband and the 3rd, 7th, and 11th in the opposite sideband are clearly indicated in the oscillographs. The amplitudes of the higher harmonics are reduced due to the low pass filter response of the sample and hold circuit following the range stores.

Figure 11 illustrates 40 dB dynamic range achieved in the initial tests. The top trace is the response to an 18 kHz sine wave (single sideband) with an amplitude of approximately 1 volt peak to peak, while the bottom trace is the response on a more sensitive scale after 40 dB of attenuation was added in each channel. The signal is still visible (vis. detectable) above the noise floor.

System tests using a more complete range store (132 I, 132 Q, fully buffered) have proven moderately successful. The primary operational problems were the expected system related difficulties associated with circuit board layout and shielding.

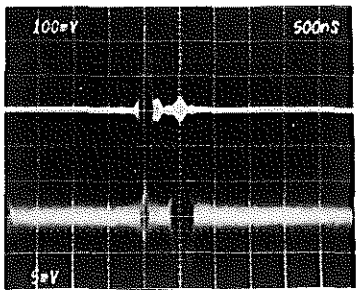


(a)



(b)

Figure 10. Response of CTM Chip and SAW CZT to complex Square Wave Input (f = 6 kHz) with Fundamental in (a) Lower Sideband and (b) Upper Sideband.



S_{MAX}

S_{MAX}-40 dB

Figure 11. Response of CTM Chip and SAW CZT to a 40 dB Change in Input Level.

Additional problem areas were related to distribution and buffering of critical waveforms to minimize both noise and waveform variations due to changes in buss loading. Solutions to these problems have been identified and will be incorporated in future designs.

The primary problem area related to the chip design resulted from gain variations between I and Q channels which are related, through the transconductance (g_m) of the individual output transistors, to MOS device threshold voltage variations mentioned earlier. In order to suppress the unwanted sideband in the SSB up conversion process by greater than 50 dB (the system dynamic range), the gains through the I and Q channels must be nearly identical. The unwanted sideband is suppressed by $20 \log [(G_I+G_Q)/(G_I-G_Q)]$ where G_I and G_Q are gains through the I and Q channels, respectively. To achieve 50 dB suppression of the unwanted sideband, G_I and G_Q must be within $\pm$ 0.63 percent of their nominal value ($\pm$ 0.06 dB variation). The achievement of the desired unwanted sideband suppression will require a redesign of the line addressable memory input/output circuitry. The two dimensional CTM discussed in the following section exhibits inherently better performance in this area.

TWO DIMENSIONAL CHARGE TRANSFER CTM

Since the "corner turning" operation can be visualized as loading a square memory array in a row-by-row fashion, then reading it column-by-column, the most direct realization involves a memory structure in which charge can be transferred either vertically (row-by-row) or horizontally (column-by-column).[8] Cell structures controlling the two dimensional charge transfer operation are complicated, and the potential advantage of a direct realization is lost in the higher risks associated with such a sophisticated design. The potential advantage of the two dimensional transfer memory is substantially improved with the addition of CCD multiplexers and demultiplexers to perform serial/parallel conversions

at the input/output ports. The resulting CCD structure has a single voltage-charge conversion at the input and a single charge-voltage conversion at the output thereby eliminating path dependent threshold voltage variations which proved troublesome in the line addressable approach.

A block diagram illustrating the operation of this two dimensional CCD memory appears in Figure 12. The input demultiplexer performs a serial/parallel conversion and loads the memory array row-by-row. During the load cycle charge is transferred vertically in the memory array. When all rows have been loaded, the array is switched to a horizontal transfer mode and the output multiplexer performs the required parallel/serial conversion of data stored in each column.

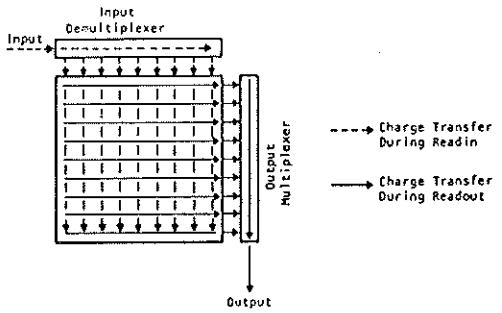


Figure 12. Operation of Two Dimensional Charge Transfer Corner Turning Memory.

Of course, as discussed previously, an additional demultiplexer can be added at the left of the memory array, and an additional multiplexer added at the bottom to permit 100% memory utilization (i.e., simultaneous load and unload).

A 32 x 32 element CCD memory based on this architecture has been designed and fabricated using the same process utilized for the line addressable CTM IC. The memory array is composed of 1024 three-phase two dimensional charge transfer cells placed on 2 mil centers. It operates as two interleaved two-phase structures with one common phase. The multiplexers and demultiplexers are four phase structures in order to match the pitch of the memory array and maintain short transfer lengths for good CTE. The structure is buried channel, with the exception of the demultiplexer input circuitry. A photomicrograph of the completed chip appears in Figure 13.

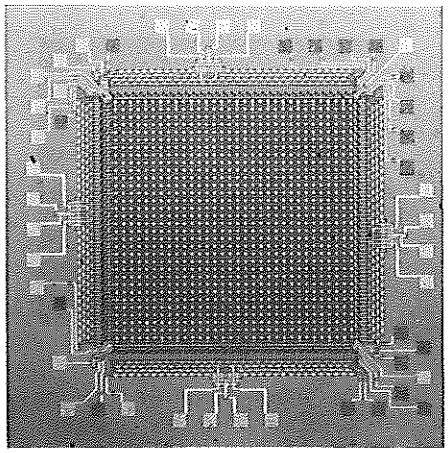


Figure 13. 32 x 32 Two Dimensional Charge Transfer Corner Turning Memory Chip.

Chip operation at a 600 kHz clock rate is demonstrated in Figure 14. Comparison with Figure 7 illustrates the dramatic improvement in fixed pattern noise performance. Dynamic range is still dictated by threshold variations in the multiplexer and demultiplexer channels, however, nearly 40 dB is maintained across an entire frame as compared to less than 20 dB observed in the best case for the line addressable CTM.

The two dimensional charge transfer CTM has been operated with data rates in excess of 5 MHz, although dynamic range is degraded due to capacitive coupling of the memory array clock pulses into the output circuit. The data rate employed in

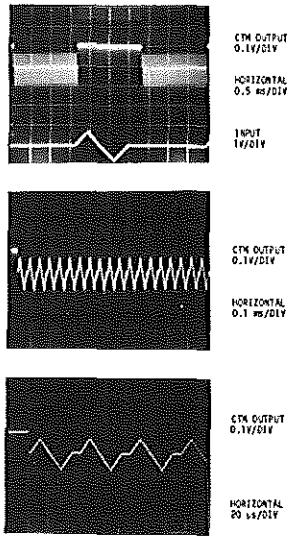


Figure 14. Two Dimensional CTM Operation at 600 kHz.

Figure 14 is due to the frequency limitation in an external circuit used to suppress this noise component. It is anticipated that the clock feedthrough problem can be remedied in future designs. The two dimensional structure has the potential for higher data rates than the line-addressable approach since the input demultiplexer function is realized with a high speed CCD structure, rather than with an MOS shift register.

Since each cell in the memory array is bounded in two dimensions, maximum charge capacity is limited to less than 1/3 that available in the line addressable design. As a result the two dimensional structure offers higher density at the possible expense of dynamic range due to comparable thermodynamic noise sources in both designs.

Although the two dimensional CTM requires a substantially larger number of clock waveforms as compared to the line addressable CTM, only the transfer gates which interface the multiplexer and demultiplexer to the memory array require precise control by system timing. The memory array clocks operate at 1/N times the data rate and are conveniently driven by standard TTL-MOS drivers at even the most ambitious data rates. The multiplexer and demultiplexer clocks run continuously and are eminently suited to resonant driver techniques at high data rates.

CONCLUSIONS

The CCD CTM/SAW CZT approach to radar signal processing provides an attractive option for improving resolution capabilities over the next few years without tremendous size, weight, and power disadvantages. SAW technology can readily provide increased throughput rates. Technological development in high speed CCD design and applications areas currently underway at many device research laboratories are expected to be key to resolution capabilities of this approach.

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REFERENCES

[1] W.H. Bailey, D.D. Buss, L.R. Hite, and M.W. Whatley, "Radar Video Processing using the CCD Chirp Z Transform," Proceedings of 1975 International Conference on the Application of Charge Coupled Devices, San Diego, October 1975, pp. 283-290.

[2] J.B.G. Roberts, R. Eames, and R.F. Simons, "A CCD SAW Processor for Pulse Doppler Radar Signals," Proceedings of 1975 International Conference on the Application of Charge Coupled Devices, San Diego, October 1975, pp. 295-300.

[3] J.B.G. Roberts, R. Eames, D.V. McCaughan, and R.F. Simons, "A Processor for Pulse-Doppler Radar," IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, Feb. 1976, pp. 100-104.

[4] R.J. Kansy, R.C. Bennett, W.H. Bailey, and L.H. Ragan, "An Analog Doppler Processor using CCD and SWD Technologies," 1977 Ultrasonics Symposium Proceedings, IEEE Cat. No. 77CH1264-1SU, pp. 952-956.

[5] M.I. Skolnik (ed.) Radar Handbook, Ch. 21, McGraw-Hill, New York, 1970.

[6] R.W. Brodersen, C.R. Hewes, and D.D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, Feb. 1976, pp. 75-84.

[7] J.M. Alsup, "Surface Acoustic Wave CZT Processors," 1974 Ultrasonics Symposium Proceedings, IEEE Cat. No. 74CHO896-1SU, pp. 378-381.

[8] R.M. Hayes, W.R. Shreve, D.T. Bell, Jr., L.T. Claiborne, and C.S. Hartmann, "Surface Wave Transforms Adptable Processor System," 1974 Ultrasonics Symposium Proceedings, IEEE Cat. No. 75CHO994-4SU.

[9] C.H. Seguin, "Two Dimensional Charge Transfer Arrays," IEEE Journal of Solid State Circuits. Vol. SC-9, No. 3, June 1974, pp. 134-142.

[10] Rome Air Development Center, Contract No. F19628-77-C-0234.

[11] K.C. Gunsagar, M.R. Guidry, and G.F. Amelio, "A CCD Line Addressable Random Access Memory (LARAM)," IEEE Journal of Solid State Circuits, Vol. SC-10, No. 5, Oct. 1975, pp. 268.

[12] B.R. Potter and C.S. Hartmann, "Surface Acoustic Wave Slanted Correlators for Linear FM Pulse Compressors," 1977 Ultrasonics Symposium Proceedings, IEEE Cat. No. 77CH1264-1SU, pp. 607-610.