PROGRAMMABLE TRANSVERSAL FILTER USING CCD COMPONENTS

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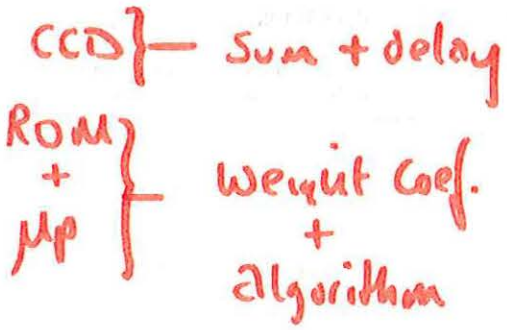
Over the past few years, CCD transversal filters have demonstrated their ability to perform several signal processing functions. The normal method of fabricating these devices involves the definition of the required weighting function in the electrode structure. Thus the technique is only applicable where (1) large volumes of a particular filter function are required and (2) there is no operational requirement to change the filter function. There are many filtering applications which are suited to CCDs but these requirements are not fulfilled. This device is aimed at applications with bandwidths below approximately 20 kHz (e.g. Sonar, Audio and Radar range bin processing) which fall into these categories. These applications do not normally utilise the bandwidth available from CCDs and in this device this bandwidth is traded for external programmability. Within the performance limitations any function which can be carried out with a transversal filter can also be realised with this device.

The transversal filter block diagram can be reconfigured such that the filter tap weight coefficients can be stored in a R.O.M. and applied to the input signal by means of a multiplying D.A.C. A CCD can then perform the necessary signal delay and summation functions. In this way the filter characteristic can be changed simply by changing the R.O.M. Alternatively, if some alterable form of storage is used, the filter characteristic can be operationally modified. A microprocessor can conveniently be used here to calculate the necessary changes in weighting coefficients and thus make an adaptive filter.

A CCD chip has been designed to perform the delay and summation function. The R.O.M. and multiplying DAC are readily available at low cost. This paper describes the concept of the device and the design of the CCD chip. At the time of writing, however, experimental results were not available.



1. INTRODUCTION

Where a fixed filter function is required a CCD split electrode transversal filter offers a low power, low weight, and, if the quantities are large enough, a low cost solution. However, if (i) the quantities do not warrant the production of a specialised mask set or (ii) there is an operational requirement to change the filter function the split electrode filter is not suitable. Such applications can be satisfied with a CCD analogue correlator structure using analogue multipliers. The problems involved with such a system include:-

(a) four quadrant analogue multipliers must be provided and these will limit the effective accuracy of the weighting coefficients. The dissipation of the multipliers will also be significant.

(b) the on chip storage time for the analogue reference channel will be limited.

Thus provision must be made for some more permanent form of storage for the weighting coefficients and a system of periodic refresh. Filter configuration considerations apart, it is often convenient to use a DAC and store the coefficients in digital form, either in a R.O.M. or as calculated by a microprocessor as part of an adaptive system.

These problems are not insoluble. The alternative presented here is based on the fact that CCDs are well suited to:-

(a) series to parallel data stream conversion and

(b) merging of charge packets to perform summation.

2. PRINCIPLE OF OPERATION

Fig. 1 shows the transversal filter block diagram as adopted by the split electrode CCD filter. This system is described by:-

$$Vout = \sum_{n=1}^{N} an\ s(t - [n - 1]\ \tau\ )$$

where s(t) is the input signal and τ is

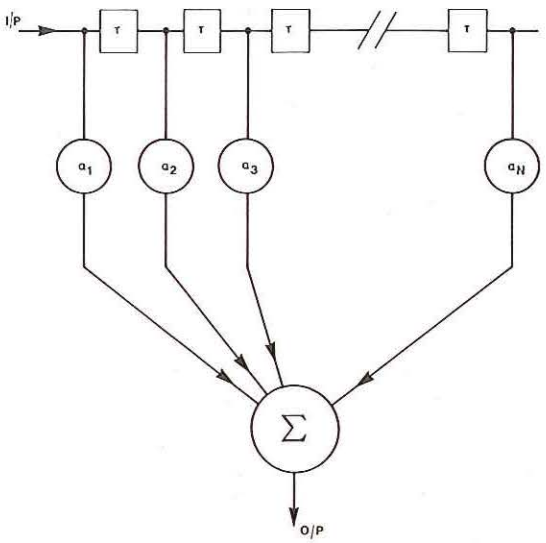


Fig. 1 Block diagram of conventional transversal filter

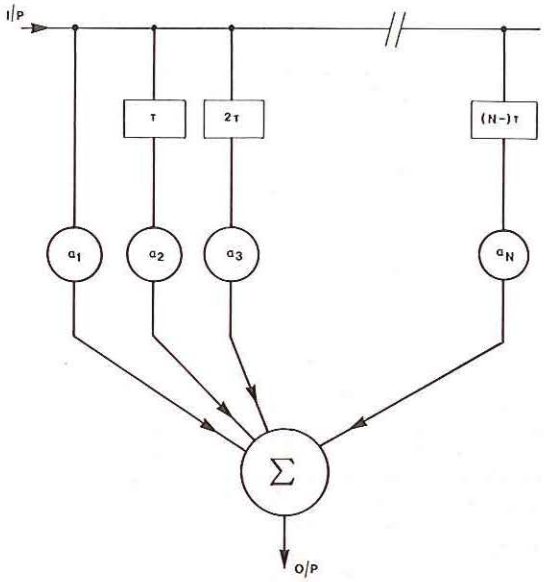


Fig. 2

the stage delay (clock period). This series realisation can be converted into the parallel realisation of Fig. 2. This is functionally the same as Fig. 1 but, of course, requires many more delay elements.

For most filtering applications the reference is stationary or quasi-stationary. This means that the delay elements and multipliers can be interchanged (Fig. 3).

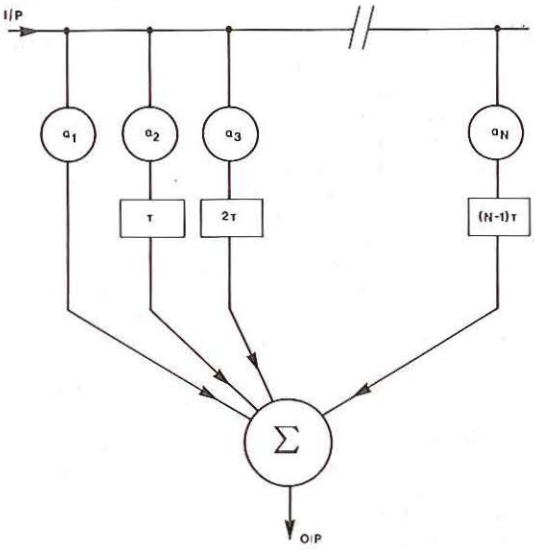


Fig. 3

This scheme is not very attractive since it involves a large number of multipliers and delay elements. The delay and summation elements of Fig. 3 can, however, be rearranged (Fig. 4) to reduce the number of delays without changing the function performed.

N multipliers are still required. However, for applications of modest bandwidth one multiplier can effectively be multiplexed. This can be achieved (Fig. 5) by using a CCD to transport the N outputs of the multiplier to the correct summation elements (Fig. 4).

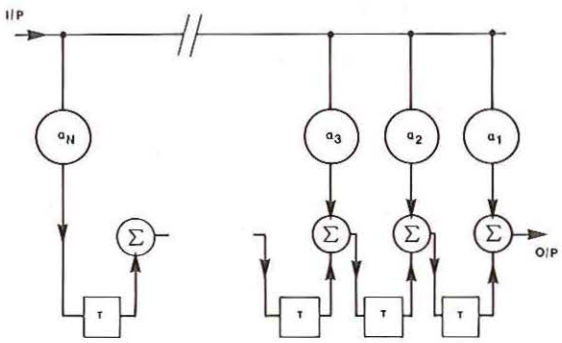


Fig. 4

This system is again described by:-

$$Vout = \sum_{n=1}^{N} a_n \; s(t - [n - 1]\,\tau)$$

This scheme can now be partitioned as shown in Fig. 6. The CCD chip performs the following functions:-

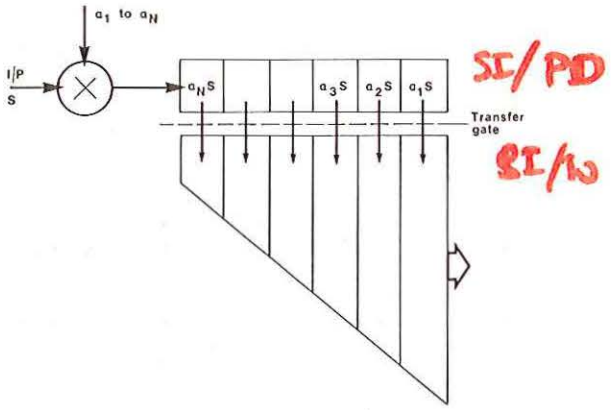


Fig. 5

(a) serial to parallel conversion necessary to multiplex the multiplier,

(b) summation function (see Fig. 4),

(c) delay function (see Fig. 4).

The multiplier can be a multiplying DAC, the digital port being fed with weighting coefficients as stored in the ROM. A sample and hold circuit is necessary to hold the input signal stationary whilst it is multiplied by all of the N coefficients.

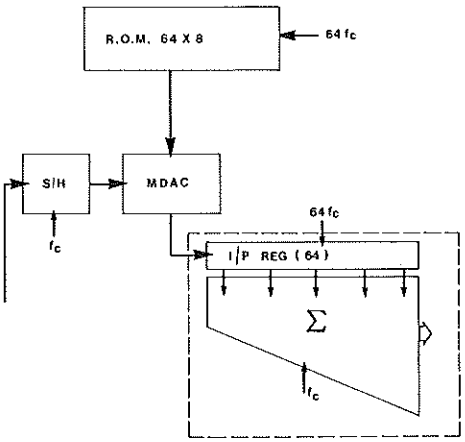


Fig. 6 Block diagram of Programmable Filter

The chip has been designed primarily for filters of N = 64. The operational sequence is as follows:-

(a) the sample and hold circuit samples the input analogue signal and presents this to the analogue port of the M.D.A.C.

(b) the 64 weighting coefficients (a_1 to a_{64}) are read out of the ROM and presented serially to the digital port of the M.D.A.C.

(c) the CCD i/p register is clocked so as to sample the 64 M.D.A.C. output products.

(d) the 64 products are transferred to the summation CCD register.

(e) the summation CCD is clocked once, thus advancing its contents by one stage.

(f) a new sample of the analogue i/p signal is taken by the sample and hold circuit and items (b) to (e) are repeated.

3. CCD CHIP DESIGN

The chip has been designed for the two-level polysilicon gate N channel CCD process which incorporates an auto aligned implanted barrier. Both surface channel and buried channel versions are being fabricated. Fig. 7 is a photograph of the check films for the first level polysilicon and metal layers. Across the top of the chip can be seen the input serial register and a second level polysilicon gate controls the transfer of charge from this register to the summation register. The width of the summation register varies from five times to fifteen times the width of the input register. This was chosen after considering the different filter functions which might be implemented with the device and allowing for the use of a background charge in both registers.

Single phase clocking has been adopted for both registers and on-chip circuitry has been incorporated to generate the additional clock phases necessary for the CCD input and output functions. Thus the chip requires three externally applied clock waveforms i.e.

(a) summation register at f_c,

(b) input register at Nf_c and

(c) parallel transfer clock at f_c.

The chosen value of N is 64, so conceivably on-chip divider circuits could have been incorporated to generate the summation register clock and parallel transfer clock from an applied clock for the input register. As will be seen later, chips can be cascaded to make filters of length greater than 64, thus changing the required division ratio. For this reason the slow clocks were not generated on chip. The serial input register requires an input technique which has a linear voltage to charge conversion, because any error here will have an effect similar to weighting coefficient error. Since the

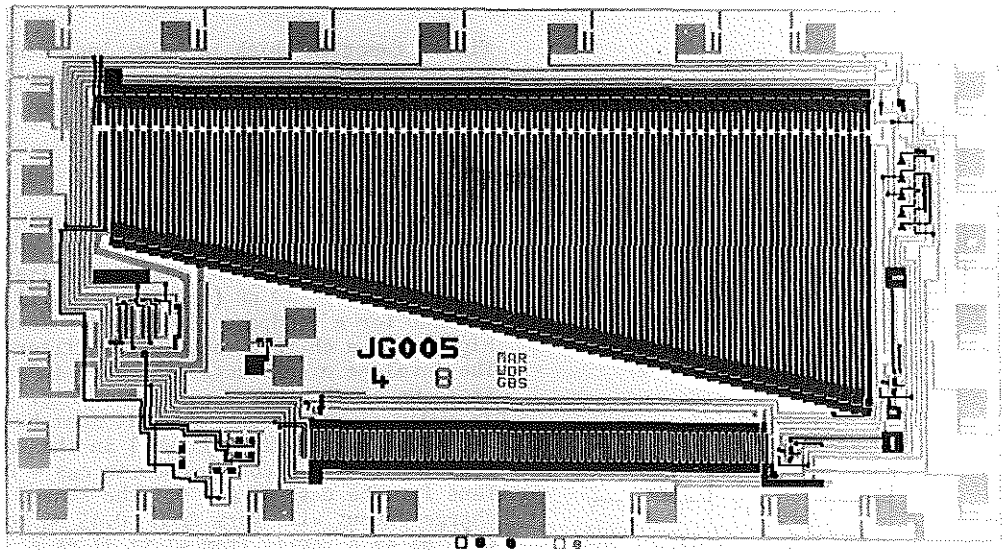


Fig. 7 Chip Layout

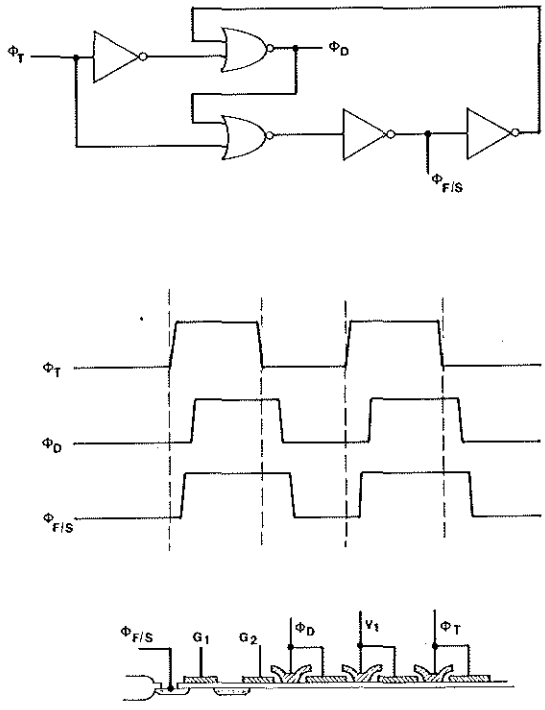


Fig. 8 CCD Input Scheme

operating frequency of 4 MHz was regarded as too high for the phase referred technique (Ref 1) to exhibit good linearity, the fill spill technique was chosen. The gating circuitry shown in Fig. 8 generates the fill and spill clock which is applied to the input diode, and a delayed clock which is applied to the first stage of the CCD. This arrangement is necessary to preserve the correct timing.

Fig. 9 shows the timing of all the clock waveforms associated with the output of the summation CCD register and the following sample-and-hold circuit, and the gating circuitry used to generate them. The output buffer circuit is designed to have good linearity as this is particularly important when chips are cascaded. The chip also incorporates several bias chains in order to further reduce the number of peripheral components required to operate the device.

Fig. 7 also shows an additional 64 stage CCD to be on the chip. This is provided for cascading purposes. By using this delay as shown in Fig. 10, a 128 stage filter can be constructed, and this principle can be extended to even longer filters. The problem, of course, is that as the filter is lengthened the available bandwidth is reduced. Since the maximum designed frequency for the input serial

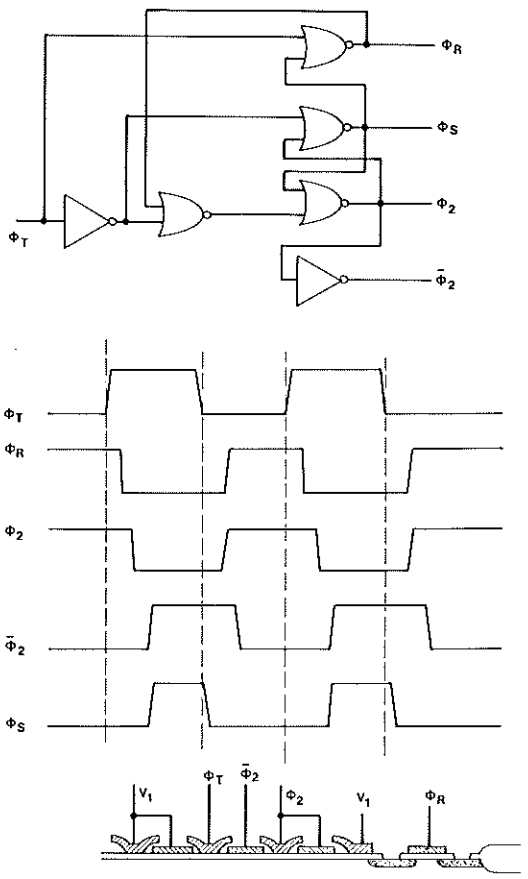


Fig. 9 Output Scheme

register is 4 MHz, $f_c = 4\ \frac{\text{MHz}}{N}$ i.e. 60, 30, and 20 KHz for a 64, 128 and 192 stage filter respectively. The cascading delay line adopts the same output scheme as the summation register (Fig. 9) and since it operates at a relatively low clock frequency the phase referred input technique (Ref 1) has been used. The phasing of the input has been arranged such that this input can be connected directly to a summation register output.

4. DYNAMIC RANGE

The output dynamic range available will depend upon the gain of the particular filter function which is being implemented. Let us consider the case of a low pass filter. If we define gain as:-

$$G = \frac{1}{s(t)N} \sum_{n=1}^{n=N} a_n\ s(t - [n-1]\ \tau)$$

where s(t) is an input signal within the passband, then a typical low pass filter might have G = -20 dB (this figure will be similar for a bandpass filter and somewhat higher for a chirp Z convolution filter). The envelope of products a_n s for $-1 < s < +1$ is shown by the shaded portion of Fig. 11a. In order to accommodate this, it must be arranged that a half full well in the input register (say q/2) corresponds to $a_n s = 0$. Thus for the case of G = 0.1 the summed charge output will vary from 0.45 Nq to 0.55 Nq as s varies from -1 to +1 at a frequency within the passband. This means that the peak to peak range of the output signal can only be $\frac{0.1}{0.55}$ (i.e. approx -15dB) of the total signal handling capability of the summation CCD. Thus for a given dimension of summation register we have lost 15 dB of dynamic range. This loss is due to the inputting of the 'unwanted' charge represented by the dotted section of Fig. 11a.

This 'unwanted' charge can be reduced as follows. If a fixed profile, equal to the modulus of the weighting coefficients (Fig. 11b) is generated and added to the $a_n s$ products before they are inputted to the CCD the $a_n s$ envelope becomes as shown in Fig. 11c. Clearly the bias can now be adjusted to subtract the pedestal and with it the 'unwanted' charge. This cannot be done completely since we must retain some background charge in the CCDs, but if 10% background charge is used the above mentioned 15 dB loss can be reduced to a 6 dB loss. The addition of the fixed profile (Fig. 11b) will, of course, result in a certain D.C. offset at the filter output, and if the weighting coefficients are changed then this offset could change. This does not usually present a problem. The addition of this fixed profile does not affect the filter function being performed.

This scheme is relatively simple to implement (see Fig. 12). The only additional

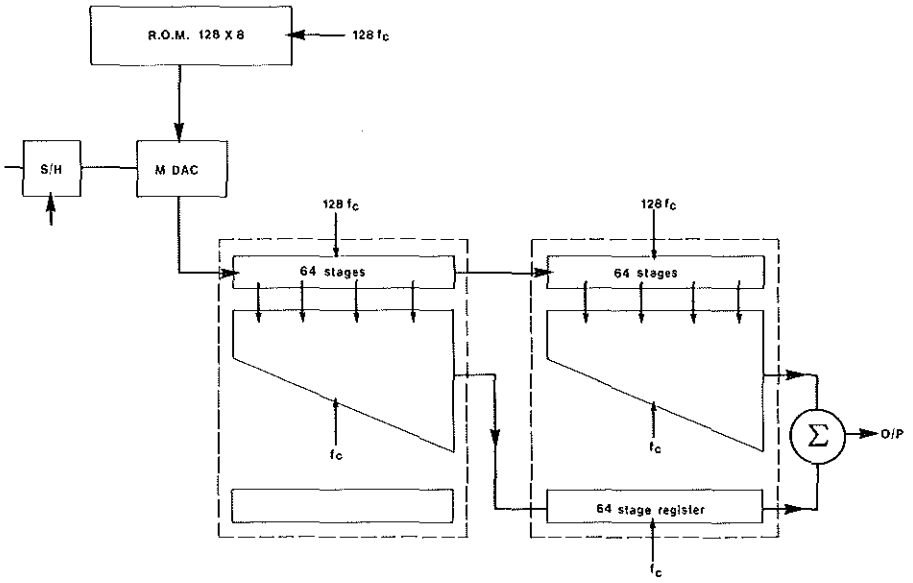


Fig. 10 Cascading of programmable filter chips

component required is a second M.D.A.C. The weighting coefficients are already available and their modulus can be obtained by omitting the sign bit. Summation of the outputs of the two MDACs is also simple since MDACs normally provide current outputs.

5. CONCLUSIONS

System functions which can be implemented with the device include:-

(a) low pass and bandpass frequency filtering,

(b) chirp Z filters for spectral analysis,

(c) correlation,

(d) adaptive filtering (including adaptive equalisation).

The flexibility of the approach has created interest particularly in the sonar field, where many different filter functions are required but only in small quantities.

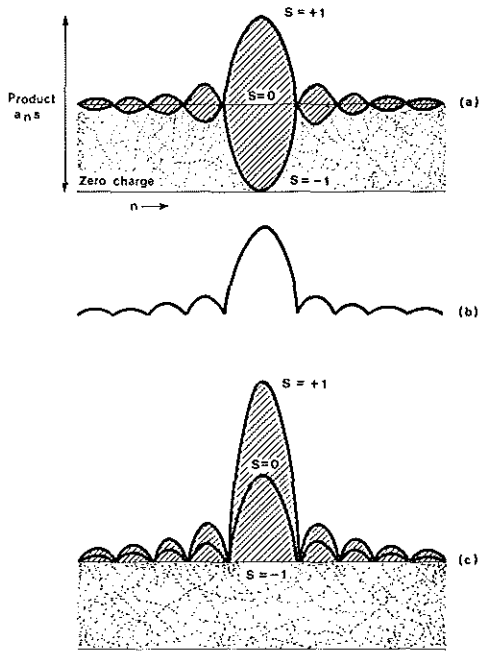


Fig. 11 Charge profile in CCD input register

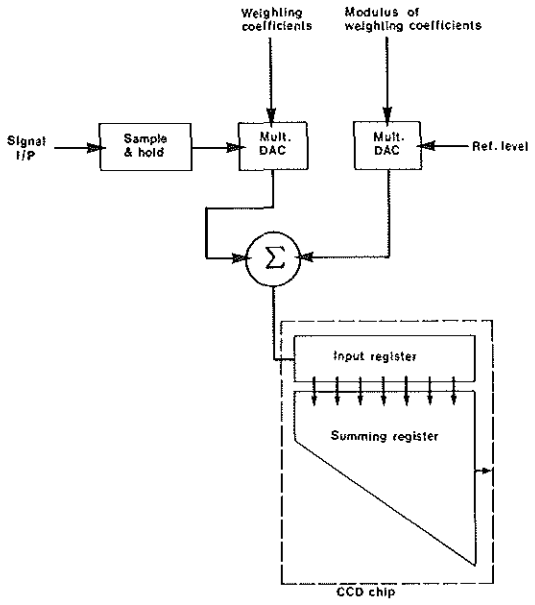


Fig. 12 System to achieve improved dynamic range

Acknowledgement

This work has been carried out with the support of the Procurement Executive, D.C.V.D, Ministry of Defence.

*Ref 1 Harp G. and McCaughan D., December 1976 "Phase-referred Input - A simple new linear CCD input method". Electronics letters Vol. 12 No. 25.