DESIGN, OPERATION AND APPLICATION OF A HIGH-SPEED CHARGE COUPLED PROGRAMMABLE TRANSVERSAL FILTER

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ABSTRACT: A monolithic 511-tap CCD programmable transversal filter (PTF) designed to function as a pseudo-noise matched filter is described. It is designed to operate at a sampling rate of 8 MHz; it is organized for staggered dual-channel operation. Experimental results on a 127-tap prototype are reported, including a 56 dB output dynamic range at 8 MHz and a 60 dB dynamic range at 4 MHz. Linearity over this range was good to ± 1%. The application of the PTF type of device in spread spectrum communication systems is discussed. Particular examples are JTIDS (Joint Tactical Information Distribution System) and the GPS (Global Positioning Satellite) system.

I. INTRODUCTION

Charge coupled device technology, due to the simplicity with which it provides delayed, sampled, analog signals and can perform a large number of multiplications of these signals with weighting coefficients, has been widely used in various kinds of transversal filter designs. Numerous split-electrode transversal filter designs have been reported; these utilize a near-continuum of weighting coefficients, (Ref. 1). When the tap weight coefficients take on binary values of + 1 of - 1, the device is a binary-analog matched filter, generally used to convolve an analog signal with a binary pseudo-noise (PN) code, (Ref. 2). When the binary code is electrically alterable, the filter is called a programmable transversal filter (PTF) which is used as a PN matched filter (PNMF). This type of filter finds application in spread spectrum receivers used for anti-jam, multiple access, and precision navigation systems.

This paper describes a high-speed CCD PTF which is organized for staggered dual-channel operation. A functional block diagram of the device is shown in Figure 1. After first loading binary codes into the two MOS shift registers the analog input signal is sampled and then transported through the tapped CCD delay line; simultaneously the odd and the even sample correlations take place. The staggered tap architecture offers both the layout advantage that the pitch of the MOS shifter register can be twice that of the CCD delay line, and several operational advantages. These include (1) allowing the PTF to respond to incoming analog waveforms which are encoded by a pair of interlaced orthogonal PN codes, and (2) multiplexing a single PN code into the two reference registers so that the maximum code loading rate is twice that of a single MOS register.

Section II describes the design and the operation of the PTF device. Some experimental data are presented in Section III. Based on the results of a prototype PTF device (PTF-1), the linearity characterisitcs of a tapped buried channel CCD are examined. In Section IV, some applications of the PTF to coded communications are presented.

II. DESIGN AND OPERATION

General

A block diagram of the monolithic PTF circuit is shown in Figure 2. The circuit consists of a tapped CCD delay line, two static MOS registers, two binary latches, two tap-summing networks, two pairs of buses, four signal output circuits, and other support circuitry. FET switches in the summing network connect

each tap to one or the other of two buses. Thus, tap weights of + 1 and - 1 are realized. The latches which control these switches temporarily store a first set of logic states from the MOS register so that the PTF can function while a second set is being loaded. The MOS register is split into an odd-tap register and an even-tap register. The associated bus pairs have independent outputs. In addition to the correlation outputs, there are correlation magniture outputs for the two channels. The magnitude signals are used for initial signal acquisition and for synchronization. Other support circuitry includes the clock generators and drivers for the MOS shift registers and the CCD structure.

CCD and MOS

The CCD delay line consists of a surface channel injection port, buried channel tapped stages and a gated-charge-integrator output amplifier. A cross-section view of the CCD delay line is shown in Figure 3. The register design is of the two-phase implanted barrier type and is operated 1-1/2 phase. Two barrier gates and two well gates form one cell. In each cell, one barrier gate and one well gate are tied together to form the clocked phase ($\emptyset_T$). The other barrier gate is tied to a dc source and the other well gate is the tap. The potential of the tap is controlled by the summing network and bus circuits. The length of each cell is 32μm making the total length of the 512 stage delay line equal to 16.38mm. The CCD delay line is designed to run at 8 MHz.

For the MOS shift registers, a 3-phase seven transistor quasi-static MOS shift register cell configuration is employed, (Ref. 3). Two clocks are needed for loading the code, while the third clock is used to provide the latch function.

Bus Output Charge Sensing

A functional schematic of bus sensing circuit is shown in Figure 4. In operation, the dc level of the buses is maintained by a pair of reset switches, which are closed during a portion of each transport clock ($\emptyset_T$) high period. After the reset switches are opened, the buses are floating. Thus, when the transport clock goes low, i.e., at the moment when the charge packets are moved under the sense electrodes, signal voltage develops between the buses. This differential voltage is proportional to the correlation coefficient of the PN code and the signal amplitude in the CCD register at the time. In the correlation output circuit, the bus voltages are first sampled by two sample and hold switches and then sensed by a differential voltage amplifier. The differential amplifier is followed by a 3-stage source-follower output buffer.

For the correlation magnitude circuit the bus pair is connected to a one-stage CCD register with two inputs which are complementary. One CCD input or the other always contains charge proportional to the magnitude of the bus voltage difference. The two CCD inputs are combined after one clock of delay. This circuit provides high common mode rejection of transients on the buses.

Clock Timing and Waveforms

Master clocks f_1 and f_2 are supplied to the PTF for the MOS shift register and the CCD, as shown in Figure 2. All clock and driver signals are produced by clock generators on the monolithic PTF circuit. There are five MOS shift register clocks controlled by f_1 and four CCD clocks controlled by f_2. Four MOS shift register clocks load the two registers in interlaced mode, and the fifth holds the codes in place. The four CCD clocks are the transport clock ($\emptyset_T$), the sampling clock ($\emptyset_S$), the reset clock ($\emptyset_R$) and the sample-and-hold clock ($\emptyset_{SH}$). The relative timing is shown in Figure 5. $\emptyset_S$ drives the input diode, injecting charge when it is low. The $\emptyset_T$ and $\emptyset_R$ functions have been described above.

$\emptyset_{SH}$, the inverse of $\emptyset_S$, samples the bus signals during its high period and holds them for the low period. Three bus signal waveforms exhibiting the positive correlation, no correlation and negative correlation cases are also displayed in Figure 5. With the aid of the $\emptyset_{SH}$ clock, output signals are valid for a full clock cycle. However, the magnitude correlation is delayed one clock period because of the one-stage CCD employed in each detection circuit.

III. EXPERIMENTAL RESULTS

Laboratory measurements were made with a prototype PTF (PTF-1), a 128-cell, 127-tap CCD PN matched filter without peripheral circuitry. A circuit schematic of the PTF-1 is shown in Figure 6.

Linearity Characteristics of the Tapped, Buried-Channel CCD

One source of nonlinearity is known to be the variable distances between a charge packet, its overlying tap, and its underlying neutral substrate as the size of the charge packet varies. These variations effect the fraction of the charge in the packet that is mirrored on the tap. In this circuit the nonlinearity of concern is between the signal voltage input and the induced signal charge on the taps. In the initial characterization of this device we also measured the nonlinearity relative to the peak displacement current in the buses associated with the induced signal charge.

The schematic for current sensing is shown in Figure 7. The bus output, V_{OB}, as well as the CCD current, plotted against input voltage, is shown in Figure 8. Here the input signal is a square wave representing the code 11110000... The amplitude of the signal is V_{in}; the signal is applied to the IG gate of the CCD. Since a surface channel structure is used for the CCD input, a relatively linear characteristic is observed for current versus V_{in}. However, a pronounced nonlinearity is exhibited in the lower portion of the V_{OB} versus V_{in} plot. This nonlinearity is attributed to the relationship between bus voltage and signal charge.

The plot in Figure 8 also suggests that when a proper offset voltage is applied between the IR and IG gates the nonlinearity can be minimized. In Figure 9, V_{OB} is plotted as function of V_{in} for the bias conditions $V_{IR} - V_{IG}$ = 1.3 V, 1.5 V, and 1.7 V. Comparing Figure 8 and Figure 9, it is noted that a significant improvement in linearity is achieved in the latter. In order to obtain more accurate linearity data, differential linearity characteristics were also investigated. A typical linearity plot is shown in Figure 10. It is seen that better than 1% linearity has been realized in this buried channel structure over a major portion of the CCD charge range, i.e., over a 1.1 V input range. It is within this range that the following dynamic range characterization was made.

Multiple Access and Dynamic Range

Figure 11a. shows simultaneous autocorrelations of two overlapping PN signals differing in power by 24 dB. The two codes are both 127-chip maximal codes; the PTF-1 was operated at 4 MHz. One autocorrelation is at a 60 dB measured S/N; the other is at 36 dB. The peak-to-peak input signal in this test was approximately 1 volt. Figure 11b. shows the same two signals with an expanded scale to illustrate autocorrelation of the weaker signal in the proximity of the stronger signal. Figure 11c. shows the same two signals with the vertical scale expanded even further to show the CCD noise level against which the signal autocorrelations are measured. CCD clock noise has been suppressed by a correlated-double-sampling charge sense circuit.

IV. APPLICATION OF THE CCD PN MATCHED FILTER

The CCD PNMF is particularly suited to certain classes of coded communications sometimes referred to as "spread spectrum". These communications systems are used for their desirable properties of

- Resistance to enemy jamming
- Multiple access with randomized combinations of time and code division
- High resolution navigation

Two important examples of these are: JTIDS (Joint Tactical Information Distribution System) and the GPS (Global Positioning Satellite) system. JTIDS is an airborn network allowing simultaneous communication using multiple data pulses, each coded by a 32-element binary pseudo noise (PN) code. Binary elements of code are called "chips", with "bits" reserved for binary data. The GPS uses very long PN code sequences correlated for a large time-bandwidth product so as to give large processing gains needed for worldwide navigation using the weak satellite-transmitted signals.

These systems can be characterized by the use of "non-repeating" PN codes which the receiver must synchronize to within some range-time ambiguity. The use of PN matched filters helps

to assure rapid synchronization. Also, by being tolerant of some timing ambiguity, PN matched filters lead to receiver simplification. Because it is a monolithic device, the CCD PNMF is well suited both for filters of long code length and for arrays of filters.

An example of spread spectrum modulation is shown in Figure 12 for MSK (Minimum Shift Key) modulation used in many systems, JTIDS being a current example. Binary data and a higher speed binary PN code are multiplied and phase-modulated onto an IF sinosoidal signal, converted to RF and radiated.

A typical receiver is shown in Figure 13. The receiver signal, downconverted to IF, is spectrally filtered by a "chip matched filter" and synchronously demodulated to baseband as in-phase (I) and quadrature (Q) components.

A pair of identical CCD PNMF's, programmed with the PN code correlates the I and Q signals. The autocorrelation R(t) is produced by the two filters as I and Q components,

$$R(t) \cos \phi \text{ and } R(t) \sin \phi$$

where ϕ is a random phase angle. Squaring, or taking the magnitude, and summing recovers $|R(t)|$, the autocorrelation magnitude. This noncoherent demodulation is used for synchronization and where data is modulated as a pulse position. Using the PTF-2 in this application, one of the monolithic circuits would be required for each of the I and Q channels.

Other PNMF Circuits

Figure 14 shows a CCD PNMF for correlation of a 32-chip PN code modulated in MSK, which is a version of CPSM (Continuous Phase Shift Modulation). The PN chip modulation in MSK is in two groups offset by T sec with each chip 2/T wide. The CCD shown is designed for the minimum 1/T sampling rate, containing 32 CCD delays and 32 taps. Figure 15 shows a CCD PNMF with 64 CCD delays, 32 taps and 2/T sampling for double the sampling resolution.

Figure 16 shows how the sampling loss is reduced by increasing the CCD sampling rate from 1/T (5 MHz in this JTIDS case) to 10 MHz, or more.

It is often necessary to noncoherently sum several PNMF autocorrelations by first squaring and then summing through appropriate delays. When this is done there is a loss in signal due to charge transfer inefficiency in the PNMF's which depends on the number of autocorrelation pulses being summed. The loss also depends on the SNR of the individual PNMF autocorrelations. This latter relationship is shown in Figure 17. Here a 1024-chip PN code correlation is analyzed for the case of 32 subcorrelations (32 groups of 32 chips each).

The arraying of several CCD PNMF's for increased sampling resolution is shown in Figure 18. For a 5 MHz chip rate PN code, 10 MHz sampling (2/T) gives 100 ns resolution. Two CCD's with 10 MHz sampling, offset 50 ns (T/4), can achieve 50 ns resolution. 25 ns resolution can be obtained by analog interpolation or using four CCD PNMF's each clocked at 10 MHz, but staggered in 25 ns delays (T/8).

CONCLUSION

A monolithic 511-tap CCD PNMF circuit has been designed which includes peripheral circuits. It is designed to operate at a sampling rate of 8 MHz. Excellent performance was reported on a 127-tap prototype, including a 60 dB output dynamic range at a 4 MHz sampling rate. A discussion of spread spectrum applications of this type of circuit has shown how filtering actually is done.

REFERENCES

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2. E. P. Herrman, P.A. Gandolfo, A. Boornard, and D. B. Stepps, "CCD Programmable Correlator", Proc. CCD Applications Conference, 1976.

3. W. N. Carr and J. P. Mize, "MOS/LSI Design and Application", McGraw-Hill Book Company, 1973.

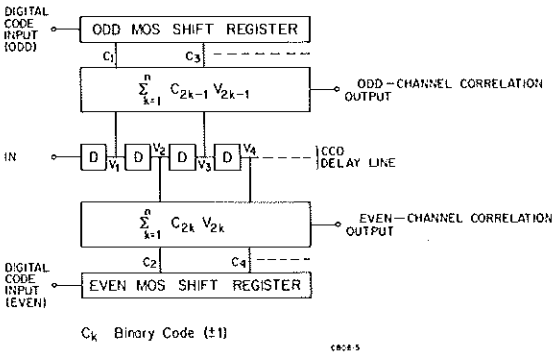


FIGURE 1 FUNCTIONAL BLOCK DIAGRAM OF THE PROGRAMMABLE TRANSVERSAL FILTER

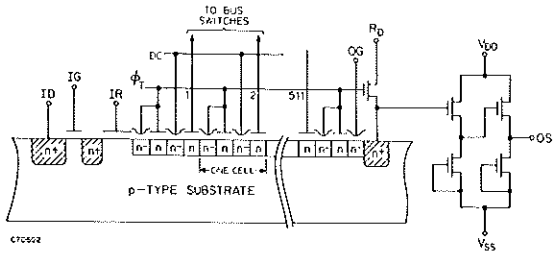


FIGURE 3 CROSS-SECTION VIEW OF THE CCD DELAY LINE

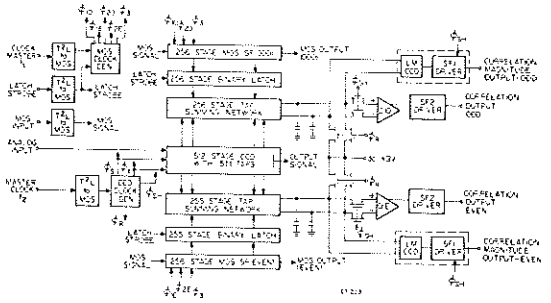


FIGURE 2 COMPLETE BLOCK DIAGRAM OF THE PROGRAMMABLE TRANSVERSAL FILTER

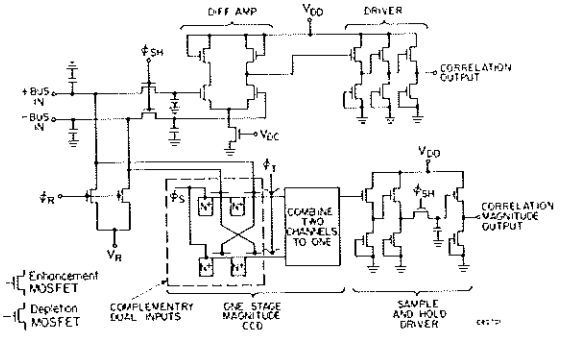


FIGURE 4 PTF BUS OUTPUT SENSING CIRCUIT SCHEMATIC

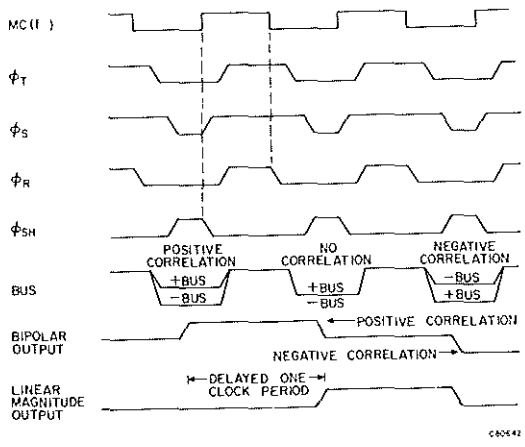


FIGURE 5 PTF CLOCK AND SIGNAL WAVEFORMS

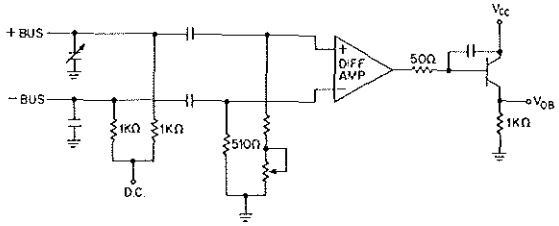


FIGURE 7 OFF-CHIP BUS OUTPUT CURRENT SENSING FOR THE PTF-1

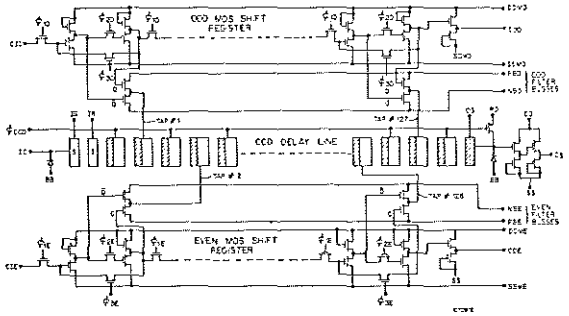


FIGURE 6 CIRCUIT SCHEMATIC OF THE PROTOTYPE PROGRAMMABLE TRANSVERSAL FILTER

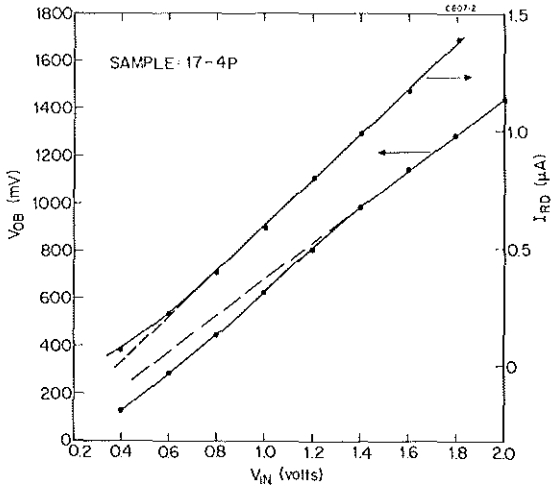


FIGURE 8 BUS OUTPUT, V_{OB}, AND CCD CURRENT, I_{RD}, VS. INPUT VOLTAGE, V_{in}. (THE DEVICE SATURATES AT V_{in} = 2.2 V)

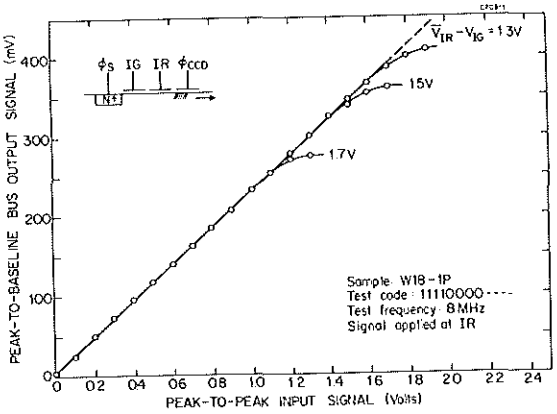
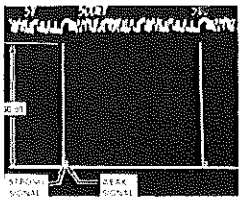
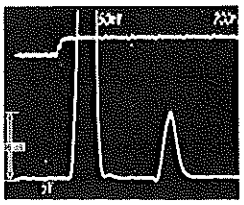


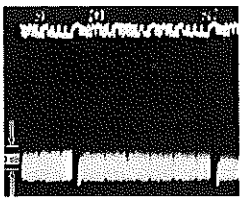
FIGURE 9 LINEARITY OF THE PTF-1 AT THREE DIFFERENT BIAS CONDITIONS



(A) SIMULTANEOUS AUTOCORRELATION OF TWO OVERLAPPING PN ENCODED SIGNALS



(B) VERTICAL SCALE EXPANDED TO SHOW RESOLUTION OF WEAKER INPUT SIGNAL



(C) VERTICAL SCALE EXPANDED AGAIN TO SHOW CCD INTERNAL NOISE LEVEL

FIGURE 11 CCD PN MATCHED FILTER AUTOCORRELATION PERFORMANCE OF THE PTF-1 AT 4 MHz

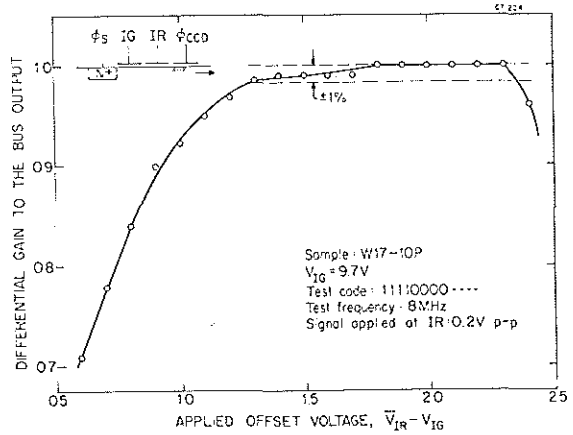
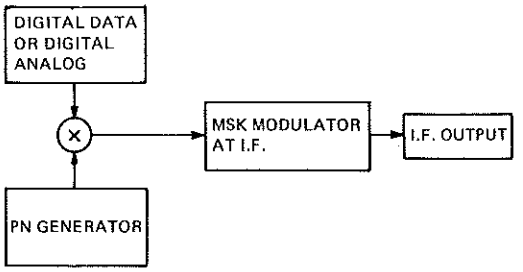
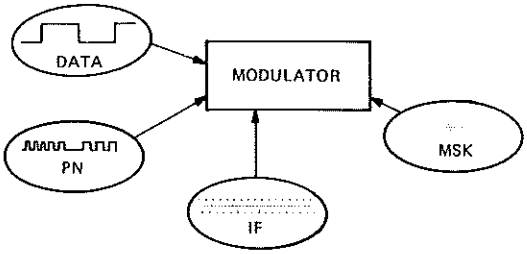


FIGURE 10 DIFFERENTIAL GAIN VS. APPLIED OFFSET VOLTAGE



A. BLOCK DIAGRAM



B. SIGNAL

FIGURE 12 MSK MODULATION

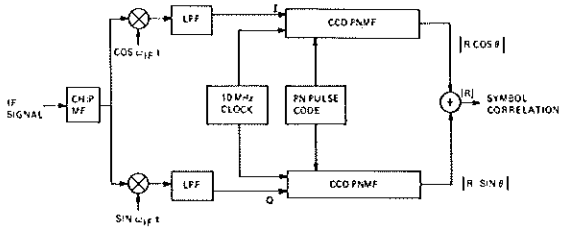


FIGURE 13 SYMBOL DEMODULATION (10 MHz RESOLUTION)

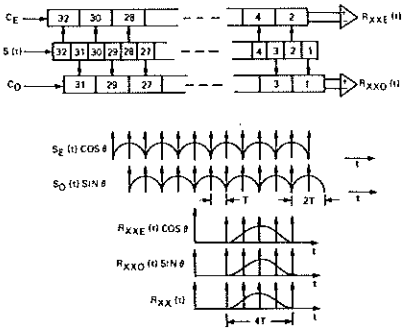


FIGURE 14 CCD PNMF FOR CPSM (1/T SAMPLING)

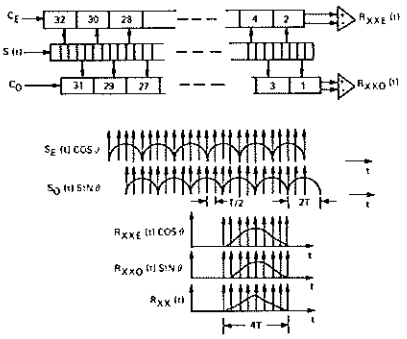


FIGURE 15 CCD PNMF FOR CPSM (2/T SAMPLING)

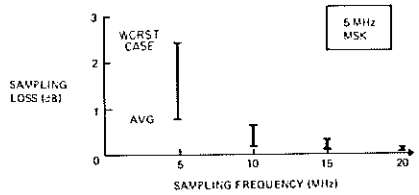


FIGURE 16 CCD PERFORMANCE LIMITATIONS

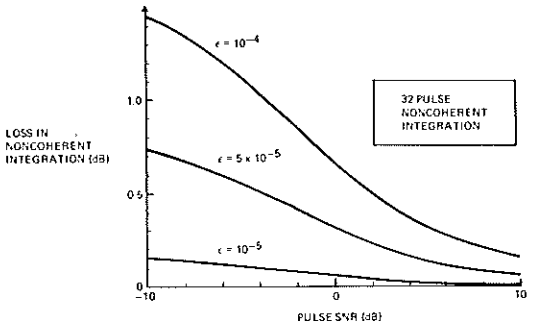


FIGURE 17 CCD CHARGE TRANSFER INEFFICIENCY (ε)

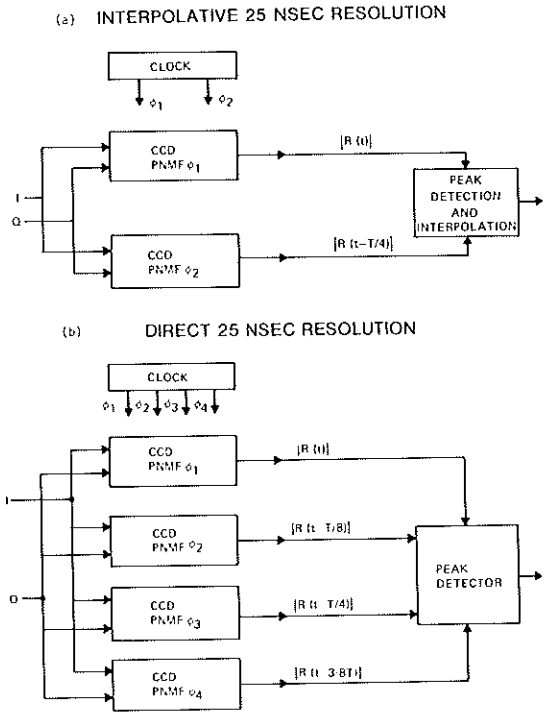


FIGURE 18 INCREASED SAMPLING RESOLUTION WITH CCD PNMF'S