THE EOP – A CCD-BASED ELECTRO-OPTICAL PROCESSOR

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Introduction

The electro-optical processor (EOP) developed by the authors is a compact, flexible device designed for use in many signal processing applications. Prior advances have been described in references 1-6. This paper will provide an overview of the history and mathematical basis of the device, present the current state of implementation, and indicate promising new investigation areas.

The EOP consists of an incoherent light source (e.g., an LED), a photo-generated mask, and an area-array charge coupled device (CCD). The package which encloses these elements is approximately two cubic inches in volume. Supporting circuitry is contained on three printed circuit cards. The current implementation is capable of performing 5×10^9 analog multiplications per second.

Development History

During the mid-1960's the scientific literature on optical signal processing emphasized the usefulness of *coherent* optical methods in performing various mathematical operations such as two-dimensional Fourier transforms and matched spatial filtering. Investigations in this regard have continued, at an increasing pace, with good results achieved. Somewhat later, investigators, disturbed by the expense, size, and critical environmental controls usually necessary in coherent systems, recognized that in some applications a non-coherent approach could be substituted. This involves simply decomposing all complex bipolar signals and operations into their real non-negative parts, as is done in digital computers, thereby eliminating the need to operate directly with complex quantities.

Early in the development of non-coherent optical processors, systems utilizing television cameras and line-array CCD's in conjunction with oscillating mirrors were successfully demonstrated.[1,2,3] The availability of area-array CCD's operating in the shift-and-add (or time-delay and integration) mode permitted removal of the oscillating mirrors.[4,5,6] But even with this elimination of the mechanical moving parts these experimental systems still required a significant amount of space to accommodate the condensing and imaging optics necessary to image the mask onto the face of the CCD. Now, the masks are fabricated directly onto the CCD obviating the need for any lenses and thereby allowing non-coherent processing modules to be packaged in just a few cubic inches.

Mathematical Basis

The generalized equation for a linear transformation

$$\int h(m,n)\, f(n)\, dn = g(m) \tag{1}$$

can be rewritten in its discrete form as

$$\sum_{n=1}^{N} h_{m,n}\, f_n = g_m \quad . \tag{2}$$

This can be further stated as a series of sums of products,

$$\begin{aligned}
&\sum_{n=1}^{N} h_{1,n}\, f_n = g_1 \quad , \\
&\sum_{n=1}^{N} h_{2,n}\, f_n = g_2 \quad , \\
&\qquad \vdots \\
&\sum_{n=1}^{N} h_{M,n}\, f_n = g_M \quad .
\end{aligned} \tag{3}$$

Some of the forms of the matrix $h_{m,n}$ used to perform various linear transformations are

Impulse Response	Transformation
h_{m-n}	Convolution
h_{n-m}	Cross-correlation
f_{n-m}	Autocorrelation
$\cos(2\pi mn)$	Cosine transform
$\exp(-2\pi imn)$	Fourier transform
$\exp(-mn)$	Laplace transform
$2\pi J_o(2\pi mn)n$	Hankel transform

The EOP, as shown schematically in Figure 1, performs any of these transformations as determined by the mask inserted between the LED and the CCD. That is, each of the M columns of the mask and CCD performs one of the M sums of products of Eq. (3). The following paragraphs qualitatively show the EOP's operation. References 4 and 5 contain a more rigorous analysis.

In the EOP, the multiplications indicated occur as light passes through a partially transparent mask containing the matrix $h_{m,n}$ as its transmittance function. The intensity of the light emanating from the mask is indeed the product of the irradiance of the original light and the intensity transmittance of the mask. Summation occurs through the ability of the CCD to convert these photons into charge packets, with a direct linear relationship between total light impinging on a cell and the amount of charge accumulated. By shifting the charge packets vertically upward by one resolution cell per input sample to the LED, addition of the proper terms through the addition of these charge packets is accomplished.

To illustrate the principal of operation consider the most trivial cases in which M = 1 (i.e., consider only a single column of the mask and CCD) and N = 3. The light source is consecutively intensity modulated by three input samples f_1, f_2, and f_3. This light illuminates a mask with transmittance values h_1, h_2, and h_3 and falls upon the three CCD cells c_1, c_2, and c_3. Since the incoming light floods the mask, at the end of the first period the charge in cells c_1 through c_3 is proportional to f_1h_1, f_1h_2, and f_1h_3 respectively. After a shift of packets from c_1 to c_2, c_2 to c_3, and from c_3 out to the horizontal shift register, and another flood illumination by the input signal f_2, the charge in cells c_1 through c_3 is proportional to f_2h_1, $f_1h_1 + f_2h_2$, and $f_1h_2 + f_2h_3$. Another shift and illumination yields three charge packets proportional to f_3h_1, $f_2h_1 + f_3h_2$, and $f_1h_1 + f_2h_2 + f_3h_3$. Upon the next shift, this last value is shifted into the horizontal shift register and read out of the CCD. It should be recognized as one of the sums of products of Eq. (3). By extension, it can be seen that an M X N resolution-cell CCD, with an appropriate mask can be used to generate a series of M sums of N products.

To continue the trivial example considered above, if a fourth input sample modulates the LED and a fourth shifting of charge packets takes place, the resulting values in c_1 through c_3 will be proportional to f_4h_1, $f_3h_1 + f_4h_2$, and $f_2h_1 + f_3h_2 + f_4h_3$. This last value, which will be read out of the CCD on the next vertical shift, is again one of the sums of products of Eq. (3) but with the time variable of the input sequence incremented by one. After the initial

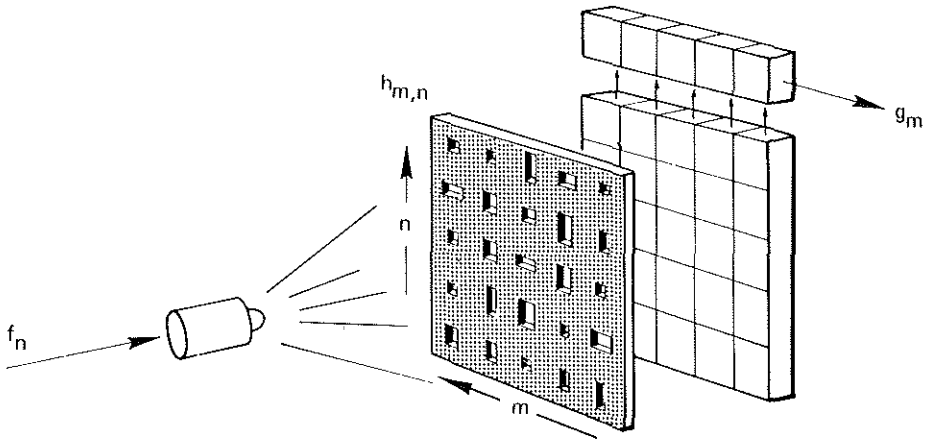

Figure 1. An Electro-Optical Processor (EOP).

start-up transient, each new input sample to the EOP produces a set of sums of products terms of Eq. (3) but where the summation takes place over the *previous* N input samples. In other words, the EOP performs *sliding-window* transformations. Or, in a pattern recognition operation, the EOP generates the complete cross-correlation *function* (i.e., the cross-correlation *value* for all time delays) between the input and each member of the library of reference signatures on the mask.

It was mentioned earlier that signal decomposition was required in those classes of linear operations which call for both real and imaginary and/or positive and negative components. In the EOP, this decomposition is achieved by using separate areas of the mask for each component, and by biasing the light source, with the results appropriately combined by electronic circuitry at the output of the CCD.[6]

Current State Of Development

In 1977, RCA Laboratories (David Sarnoff Research Center, Princeton, New Jersey) under contract to the Naval Ocean Systems Center (San Diego, California) fabricated masks onto RCA's commercially available model SID 52501 CCD. These devices have N = 512 by M = 320 resolution cells on 1.2 mil centers. The first step in the process was the preparation of a photolithographic mask containing the desired 512 by 320 element matrix of apertures $h_{m,n}$. The remaining steps consisted of (1) depositing a protective oxide layer on the CCD structure, (2) depositing an opaque 1200 Å thick chromium film onto this layer, (3) imaging the photolithographic mask onto this film and etching away the mask apertures using standard photoresist techniques, and (4) covering the resulting device with a protective 10,000 Å thick SiO_2 layer. The range of aperture sizes achieved in this effort was 100 discrete distinguisable levels and improvements in the technique are in progress to push this to about 256 discrete levels.

Figure 2 shows a corner of the resulting "masked CCD". It is interesting to note the three-phase electrode structure of the horizontal shift register at the top of the photograph and the electrode structure (3 electrodes per resolution cell) of the vertical registers showing through the transparent apertures of the mask.

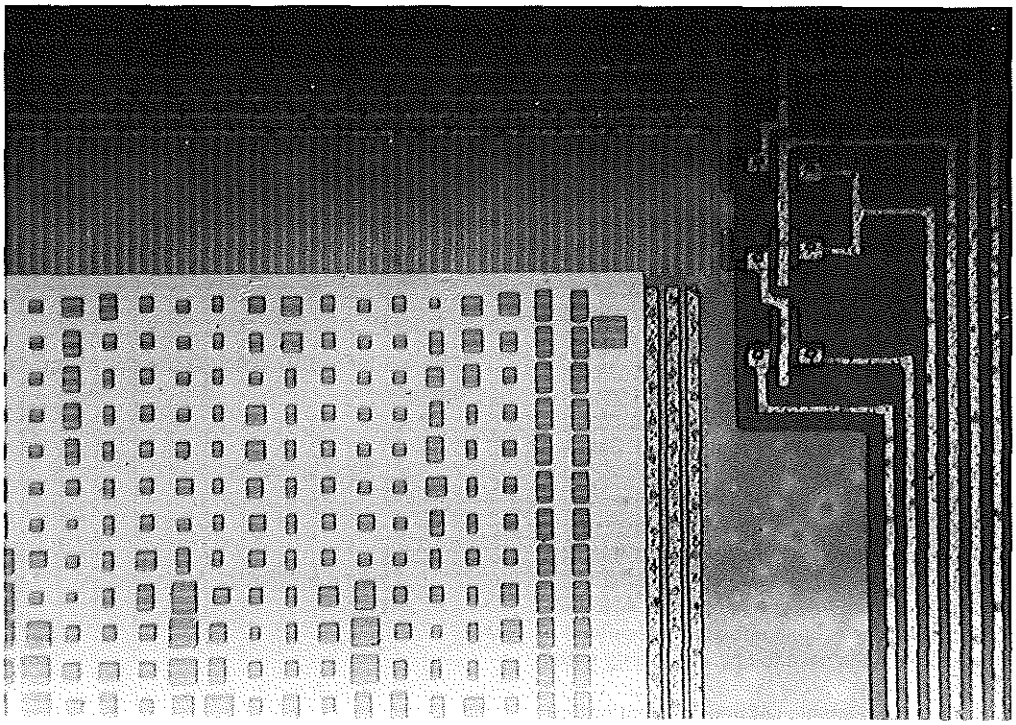

Figure 2. Photomicrograph of a corner of the mask/CCD combination.

With such a "masked CCD" the only remaining component in Figure 1 is the illumination device. Successful results have been obtained with the Monsanto MV-4 visible LED. The housing which holds the LED and CCD also serves as an optical cavity to help provide a uniform illumination across the CCD surface. Several optical cavity geometries are currently being theoretically and experimentally investigated with respect to maximizing uniformity and efficiency in a minimum size. As discussed more fully in reference 7, both the cylindrical and spherical geometries with appropriately placed baffles appear capable of reducing illumination nonuniformities across the CCD surface to under 1% in a housing size of 2 cubic inches.

This processor, with a cylindrical cavity geometry, is currently being tested and evaluated. Factors which adversely affect performance and which therefore need to be measured and controlled, are

- LED linearity,
- spatial uniformity of illumination,
- CCD spatial variations in sensitivity,
- optical crosstalk between CCD cells
- CCD charge transfer efficiency, and
- CCD dynamic range.

Expected performance parameters are

$v_{in} = v_{ver} = 32{,}000$ samples/sec
$v_{hor} = 10{,}240{,}000$ shifts/sec
dynamic range > 50 dB, and
nonlinearity $< 1\%$.

Such a processing module has a processing rate of $32{,}000 \times 512 \times 320 \approx 5 \times 10^9$ multiplications/sec.

The following section discusses the external circuitry designed to drive this EOP unit. No attempt has been made to miniaturize this circuitry; instead the intention has been to produce a general-purpose module in which changes in timing and operation could be incorporated by simple rewiring or changing a few components without the need for new printed circuit boards. This modular design approach, in which the circuitry used to operate the EOP as, say, a Fourier transformer is only a slightly modified version of that used to operate the EOP (with a different mask) as, say, a multi-channel cross-correlator, has saved considerable time in fabricating and verifying new processing systems.

An Overview of System Implementation

In the present implementation, the external circuitry required to operate the EOP is partitioned into three functional subsystems. These are: (1) master timing, (2) processor driving, and (3) signal conditioning. As their names imply, the master timing circuit provides the required synchronization signals for the overall system, the processor driver controls the LED operation and generates the necessary clocking waveforms for the CCD, and the signal conditioner refines the CCD read-out to be suitable for display and/or further processing. Each subsystem occupies one 10 in. by 4 in. printed circuit card. In the following paragraphs, the function and design of each card is described in detail.

Master Timing

There are two functions for the master timing card. First, it defines the clocking intervals for CCD operation. Therefore in this respect, the design is device dependent. The RCA CCD (SID52501) employed requires both vertical and horizontal clocks to operate. The alternating intervals of vertical and horizontal clocks comprise the Horizontal Gate as shown in Figure 3. The vertical clock is active only between the horizontal clock intervals.

Secondly, the master timing provides the markers required to relate the CCD read-out to the mask columns or references. The CCD read-out is the computational result, g_m, from the EOP; that is, it is a sequence of M-element vectors in the form of

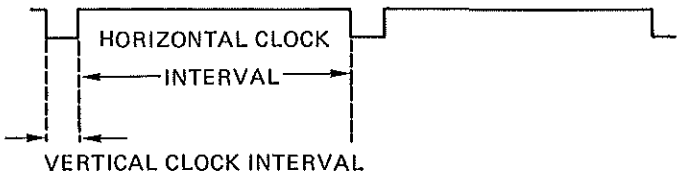

Figure 3. Horizontal Gate.

a time-varying analog waveform. These markers enable the system to recognize which point in time on this analog waveform represents the result of the running sum of products of the input sequence f_n and the m^{th} mask column. The numbers and kinds of timing markers required are application dependent. The card under discussion is designed for general-purpose usage, in that only minor wiring modifications are required to provide the markers appropriate for, for example, spectrum analysis, finite impulse response (FIR) filtering, or cross-correlation operations.

This card provides the following outputs:

(1) Horizontal Gate, shown in Fig. 3. This defines the active horizontal clock interval with a duration of 323 horizontal clock pulses and the active vertical clock interval with a duration of 7 horizontal clock pulses. (Each horizontal or vertical clock pulse results in one shift along the horizontal or vertical register respectively. However, as will be discussed later, a vertical clock pulse occupies 7 horizontal clock periods.)

(2) Valid Row Gate. This defines the location of the desired rows of the CCD output. In many applications only certain rows of outputs are wanted. For example, in an EOP performing a 512-point Fourier transform with a 75% window-overlap factor, only every 128^{th} row of output Fourier coefficients, g_m, would be desired.

(3) Valid Column Gate. This defines the location of the desired columns in the CCD read-out line. In many applications, only a specific sequence of columns are wanted. For example, in a spectrum analyzer, one may be interested in only a subset of the frequency components, or in a cross-correlator, one may wish to ignore the columns used to obtain normalization constants and zero levels.

(4) Normalization & Dark-Level Pulses. These are time signals indicating where the normalization value and dark-level value occur on a line basis. The former is simply the sum of the previous N samples of the input signal and can be obtained simply by letting $h_{m,n} = 1$ for one column of the mask. This value is necessary in normalizing a cross-correlation function. The dark-level value provides a convenient zero level. As stated earlier, there are 323 horizontal clock pulses, and 322 states in the horizontal register of the CCD. The one extra clock pulse is for shifting out the video black level (containing only thermally generated "dark current") to be used for dc restoration.

(5) Frame Synchronization Pulse. This occurs at the start of each 512-line frame and has a duration of one line (i.e., one period of the Horizontal Gate). A Frame Time is the time required to shift a charge packet from the bottom to the top row of CCD cells. When the electro-optical processor is operated in the so-called TV mode, for initial check out purposes, the Frame Synchronization Pulse is used as the input to the LED so that the LED flashes on only once during the entire frame. Conveniently, this results in an image of the mask being read out from the CCD (i.e., each mask column has been correlated with a Dirac delta function thus the correlation output is the mask pattern itself).

The circuitry to provide these outputs is shown in Figure 4. It consists of two sections: the horizontal clock section and vertical clock section -- each composed of counters, decoders and combinatorial logic.

The basic horizontal timing is maintained by a set of horizontal counters. They provide 330 distinct clock periods. With this configuration, any of the 330 clock periods composing the line can be pinpointed by the use of decoders and logic circuits. In this manner, the various horizontal timing signals are generated. Furthermore, the horizontal section produces a vertical pulse occurring at the line rate. This pulse is used to increment the line counters in the vertical section to maintain 512 distinct line periods. The counter output is decoded to produce the Frame Synchronization Pulse and the Valid Row Gate. Additionally a high frequency clock running at four times the horizontal clock frequency is available for producing the three-phase horizontal clocks in the processor driver card.

Processor Driver

The second card, called the processor driver, contains: (1) the LED modulation circuitry, (2) the EOP module itself, and (3) the circuitry to generate the CCD drive waveforms.

The input signal to the processor system is applied to the LED modulator which controls the optical output of the LED. The EOP module contains the LED and the masked CCD enclosed in an optical cavity, as described in an earlier section. The waveform circuitry is divided into the horizontal and

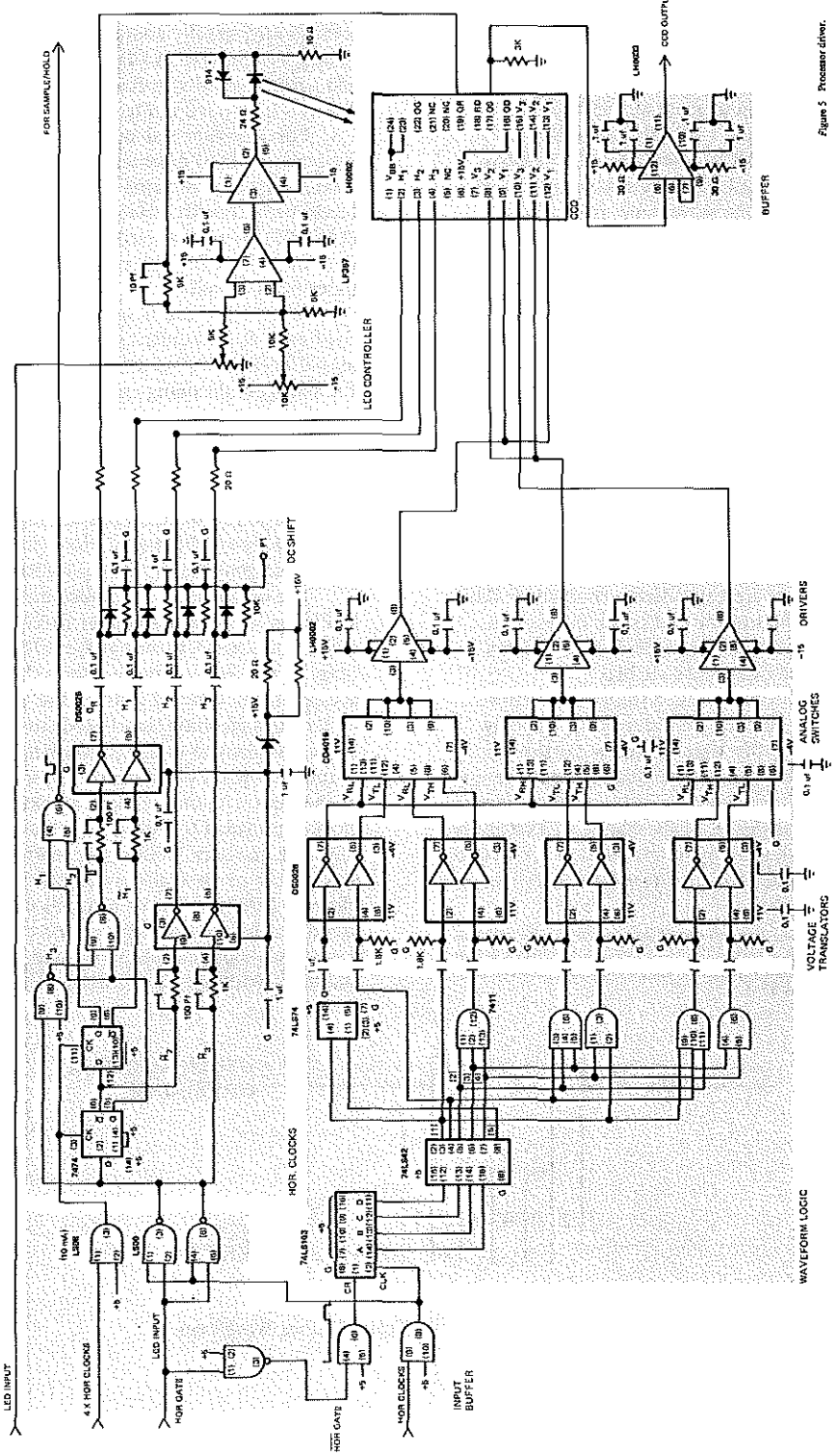

Figure 5 Processor driver.

vertical clocking sections. The former produces the three-phase, two-level horizontal clocks and the latter produces the three-phase multi-level vertical clocks.*

The circuit for the LED modulator and the horizontal and vertical clock sections of the processor driver are shown in Figure 5. As shown in the upper right hand corner of the circuit diagram, the LED driver consists of a gain element (LF357), a current driver (LH0002) and the LED (Monsanto MV4 or Texas Instruments XL12) connected in a negative feedback fashion. The LED current is sampled and forced to have the same waveshape as the input voltage. In operation, this circuit can produce a current pulse of 0 to 100 ma through the LED with a rise time of 200 nsec.

The top portion of Fig. 5 shows the horizontal clock section. After the horizontal clocks are enabled by the Horizontal Gate, the three-phase two-level clocking waveforms used to actually drive the CCD are generated by two stages of a flip-flop (74LS74) connected in a shift-register fashion. The amount of overlap among these phases is controlled by the phasing of the horizontal clocks and the 4X clocks (i.e., clocks running at four times the horizontal clock rate). Clock drivers (DS0026) are used to provide the horizontal drive capability. The outputs of the clock drivers are capacitively coupled to the CCD so that a dc bias to the clocks can be inserted. The entire waveform can be shifted up and down with respect to the CCD substrate bias.

The lower portion of Fig. 5 shows the vertical clock section. Each cycle of the vertical clocking waveform occupies the time of seven horizontal clock periods. Thus the vertical clock period is seven times that of the horizontal clock (i.e., It takes seven times longer to transfer all of the charge packets in the CCD vertical registers up by one resolution cell than to transfer those in the horizontal register to the right by one cell).

*The processor driver circuitry described herein is designed for use with the aforementioned RCA SID 52501 CCD. For a more detailed discussion of the required waveforms than space permits here, please refer to the RCA specifications sheet.

The Horizontal Gate enables a binary counter to maintain the seven district horizontal clock periods comprising each vertical clock cycle. The signals representing the timing of each of these distinct periods are logically combined to control a set of four analog switches (RCA CD4016), inputs to which are fed with the desired voltage levels. One of such waveforms is illustrated in Figure 6.

For experimental purposes, the circuitry to generate the CCD drive waveform has been made very flexible thereby allowing changes in various voltage levels to be readily effected. Current amplifiers (LH0002) are used as buffers between the switch outputs and the CCD. This circuit exhibits rise and fall times from –2 volts to +7 volts of 50 nsec.

Since each card is designed to be an independent unit, for modularity considerations, a buffer amplifier (LH0033) is used to interface the CCD with the signal conditioning card.

Signal Conditioner

The signal conditioning card performs: (1) amplification of the CCD output, (2) dc restoration, (3) a sample-and-hold operation on the amplified signal; and provides (4) output interfacing capability.

The detail circuit and block diagrams are shown in Figure 7. A vido amplifier (μA733) is used for amplifying the CCD output from the ten millivolt range to the one volt range. Since the CCD output is capacitively coupled through the amplifier, the dc level of this resulting signal needs to be re-established. It is convenient to utilize the dark level of the CCD output as a point of reference. As mentioned earlier in the master timing section, an extra horizontal clock is provided to shift out the dark level. During this time, the dark level is clamped to negative one volt by use of an analog switch (DG 187) and amplifier (LH0033). The dc restored signal is still contaminated by feed-through of the clocks, so these extraneous signals must be removed by using a sample-and-hold amplifier (Datel SHM-2) to obtain the

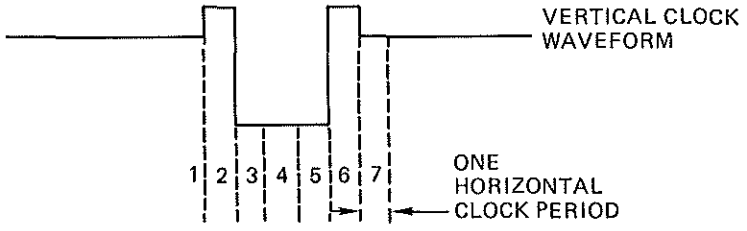

Figure 6. One Phase of Vertical Clock Waveform.

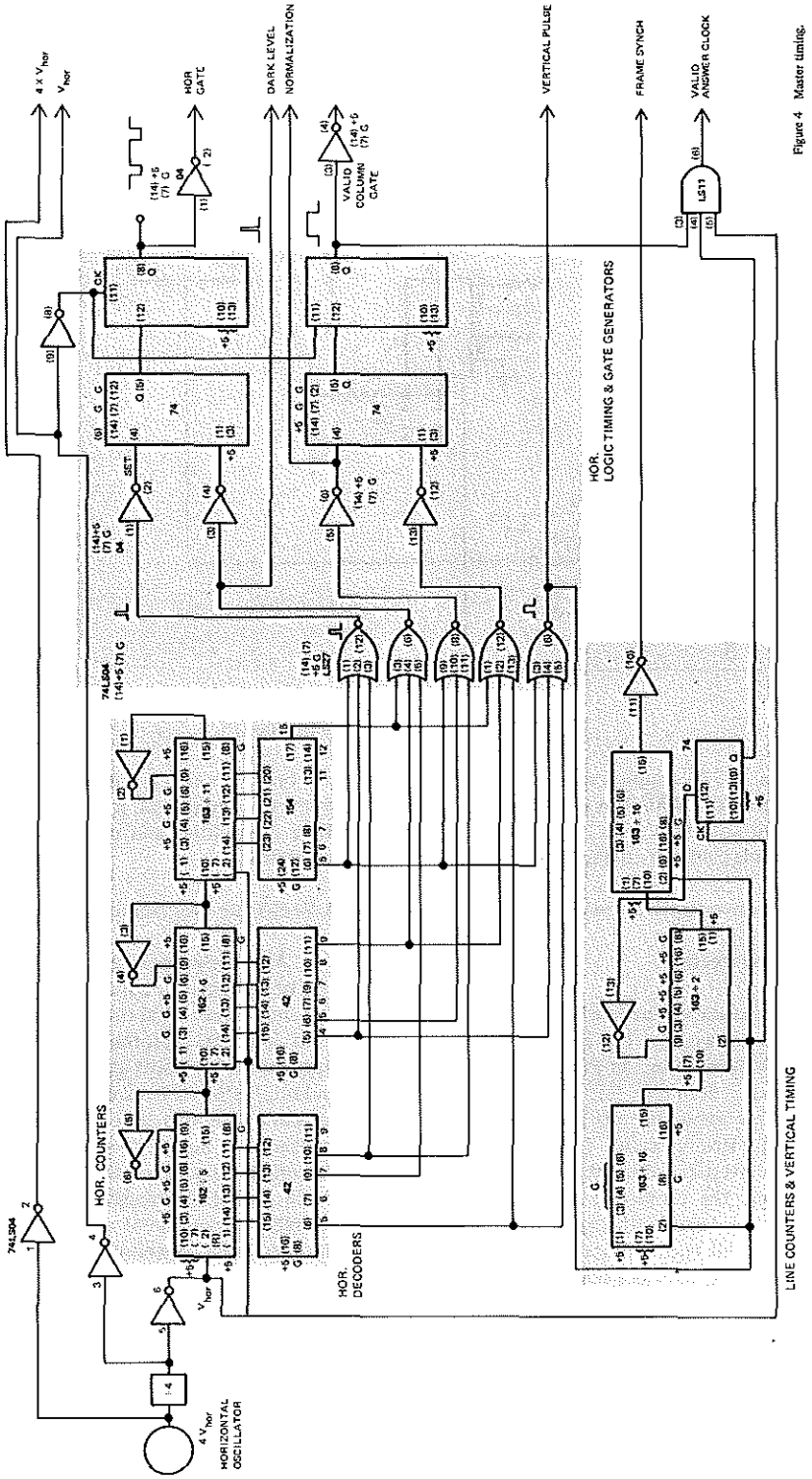

Figure 4 Master timing.

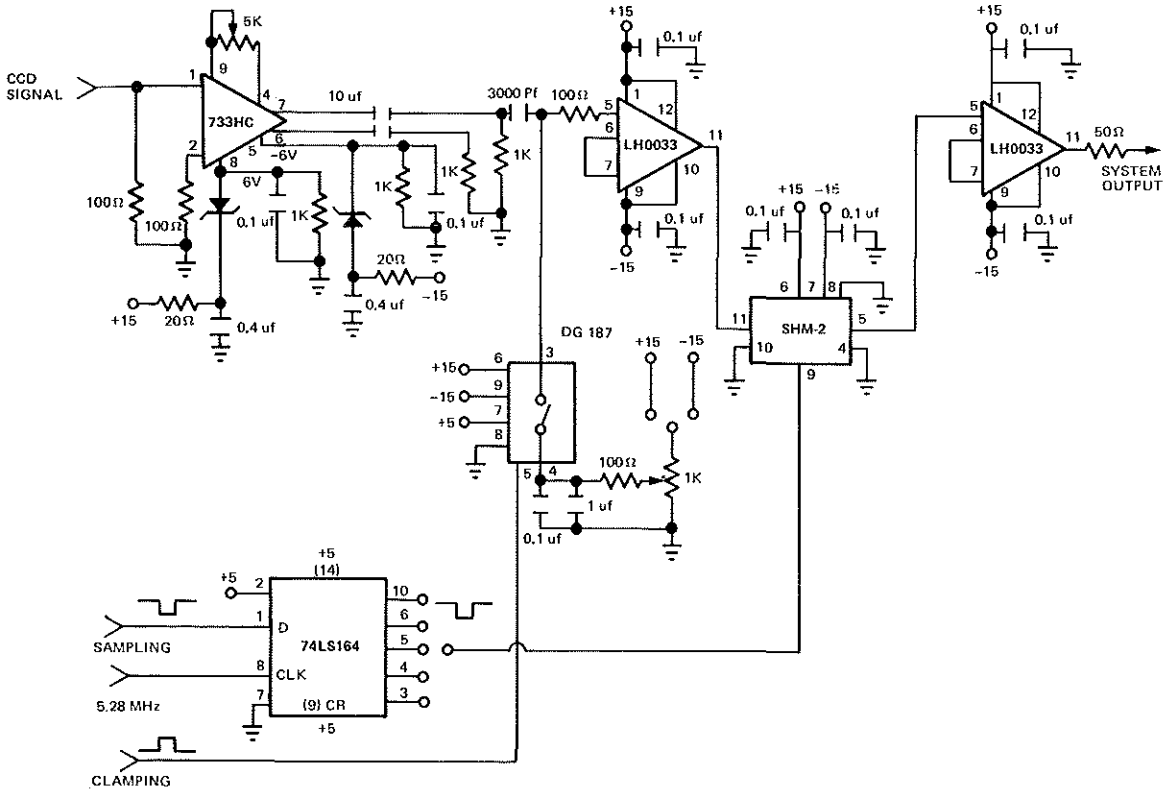

Figure 7. Signal Conditioner.

desired analog signal -- 320 sampled values per row. Again a buffer amplifier (LH0033) is used to interface the sample-and-hold unit with any external load for output display and/or further processing.

New Investigative Areas

A Modified CCD Architecture

During the discussion of the mathematical basis for the EOP, it was shown that the EOP performs *sliding-window* transformations. In those cases where large window overlap is desirable, for instance when an incoming signal has some arbitrary unknown starting point, this feature is very useful. In those cases where little window overlap is desired some mechanism for flushing out the unwanted coefficients (thereby increasing the bandwidth capability of the EOP) is desired. To this end, industry has been approached for solutions, such as a selectable gating function inserted between the area array and the output parallel to serial converter.[8] If successful, the vertical shift rate (and therefore the input sample rate) will become much less dependent on the horizontal shift rate, and in fact, limited only by CCD shift drive capabilities and electro-optical input signal generation.

A Real-Time Programmable Mask

Another promising investigative area is the mask. It is obvious that if a method of generating masks in real time or near real time existed, additional operations could be performed, such as non-linear transformations, recursive algorithms, adaptive solutions, and multi-stimulus correlations. Technologies being considered at this time include matrix-addressed transmissive liquid crystal devices. Laboratory demonstrations have been performed using a Hughes liquid crystal cell imaged onto the CCD, but considerable advancement must be made in expanding the grey scale capability (i.e., dynamic range), in reducing the resolution cell size to be compatible with that of CCD's, and ultimately in fabricating the transmissive matrix-addressed mask directly on the CCD surface.

Digital Capability

The last area to be discussed is that of digital operations with this unit. Historically, optical processing has been considered only applicable to analog problems with accuracies corresponding to about 8 bits, but work is proceeding with mask design and supporting algorithms to permit digital operations with any desired degree of accuracy.

Conclusion

The EOP is a compact, low-cost, low-power, high-speed signal processing module capable of performing a larger variety of useful linear operations with processing rates greater than 10^9 multiplications per second (depending on the array size and maximum vertical shift rate of the CCD used). General-purpose modules, each consisting of a two cubic inch EOP and three cards of external circuitry, have been fabricated and are now undergoing test and evaluation in a variety of application areas. Also, further development work is planned to increase the EOP's input rate from the present 32 kHz to the MHz range, to provide real-time programmability of the mask, and to allow the performance of digital operations with arbitrary accuracy.

Acknowledgements

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