A SILICON CCD/NMOS PROCESSOR FOR InSb CID ARRAYS

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ABSTRACT: Current infrared systems are limited in performance by the relatively small number of detectors which can economically be included on the focal plane. Several technology development programs have been initiated to improve the performance of IR systems by making feasible the fabrication of IR focal plane arrays (FPAs) including orders of magnitude more detectors than is practical with present technologies. In the case of imagers (FLIR) for tactical applications, FPA's with several thousands of detectors can be combined with time-delay-and-integration (TDI) signal processing in serial-parallel scanned systems to give dramatic improvements in sensitivity.

One technical approach to the realization of FPAs is the use of an intrinsic detector array of charge injection devices (CIDs) coupled to a silicon signal processor chip. This approach requires many fewer interconnects than the one per detector of most hybrid approaches and additionally can be implemented with a less mature detector MIS technology than is required for monolithic intrinsic approaches.

This paper describes the development of a silicon signal processor for an on-focal plane application with a 16 x 24 element InSb CID detector array. The processor chip includes preamplifier, correlated double sampling (CDS), 16-element TDI and AC couple/DC restore circuitry for each of 24 detector channels. The parallel signals are combined in a 24 channel CCD multiplexer.

I. INTRODUCTION

Current generation infrared systems are limited in performance by the relatively small numbers of detectors, typically less than 200, which can economically be included on the focal plane. Several technology development programs have been pursued to make feasible the fabrication of infrared focal plane arrays (FPAs) having many more detectors than are presently practical. In the case of infrared imagers, or FLIR, for tactical applications, FPAs with several thousand detectors would provide dramatic improvements in performance.

As a result of the low contrast available for tactical infrared imagers, the staring mode of imaging commonly used at visible wavelengths has difficulty in distinguishing between variations in detector responsivity and variations in scene irradiance. For example, since it is necessary to resolve apparent target temperature differences of less than 0.1°C, detector responsivity uniformity would have to be better than a few tenths of a per cent in the 3-5 μm wavelength band. Device uniformities of this order are simply not practical with available technologies. As a result, the mechanically scanned mode of operation - resulting in an effective AC coupling of the imager to the scene - is generally used for infrared imagers to avoid severe uniformity requirements for the detector responsivities. Two dimensional arrays operated in a serial-parallel scan mode can take advantage of time-delay-and-integration

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(TDI) signal processing to achieve enhanced signal-to-noise ratios and built-in redundancy protection against failure of a few detectors.

One approach to the realization of FPAs for serial-parallel scanned imagers is the combined use of an intrinsic IR detector array with an on-focal plane silicon IC designed to provide the desired signal processing functions for conditioning the raw detector information.[1] The development of charge injection device (CID) arrays fabricated on InSb has resulted in the potential for achieving background limited IR imager performance at detector sampling rates commensurate with tactical requirements.[2] The CID is an MIS structure in which IR-photon generated minority carriers are stored in potential wells which are created by means of external voltages applied to the gate electrodes. Readout of the signal charge is typically accomplished by injecting the stored charge into the substrate and sensing the resulting current with external circuitry. The function of the silicon signal processor IC is to sense the detector signal and perform the necessary preamplification and the desired TDI processing for signal-to-noise enhancement.

The InSb CID/Si processor approach offers several advantages. It requires many fewer interconnects than the one per detector needed for most hybrid photo-diode approaches, and it is expected to have fewer frequency response problems than the hybrid arrays. In addition, the CID approach can be implemented with a much less advanced MIS interface technology than would be required for infrared CCDs. The disadvantages of the CID approach result from the relatively high capacitance of the detector output node and from the need to read the entire array into the silicon processor within every sample time (at least once per dwell time, in other words). The high output capacitance results in a small output noise voltage for a given noise on the charge packet. This means that the preamplifier on the processor must have a very low input noise if the system is to be limited by the background shot noise on the charge packet. Read out of the entire array, which may contain many detectors, during each sample time means a relatively high output data rate for imager applications. This requires a wide bandwidth for the processor circuits (particularly the preamplifier), which makes low noise, low power performance even more difficult to achieve.

II. PROCESSOR REQUIREMENTS

This paper describes the development of a silicon signal processor designed to interface with a 16x24 element InSb CID detector array.[2] For the purpose of the signal processor technology development, a prototype system was assumed to be a horizontally scanned, 525-line TV-compatible FLIR. The focal plane was assumed to consist of ten 16x24 element CID arrays, with the 16 elements in the direction of scan for TDI, with an associated signal processor chip for each CID array. A complete list of the prototype system specifications appears in Table 1. This type of system was selected, in part, because it placed relatively stringent requirements on the signal processor circuits in terms of sampling rate and noise performance.

A processor implementation with silicon CCD/NMOS technology was based on the following considerations: 1) the operation of NMOS circuitry is enhanced at low temperatures[3], whereas that of bipolar circuitry is typically degraded[4], 2) the TDI function is easily implemented with CCD structures,[5] 3) CID control and signal sensing are facilitated using NMOS amplifier circuits which exhibit extremely high input impedances. Based on the prototype system specification the signal processor chip was configured to provide the necessary preamplification, TDI processing and multiplexing for 24 detector channels from each CID array. The block diagram in Figure 1 illustrates the components included in each channel and will be discussed in detail in the next section.

Scan	Horizontal Unidirectional (70% Efficiency)
Display Compatibility	525-Line TV (2:1 Interlace with 4/3 Aspect Ratio)
Detectors	10- 16x24 CID Arrays
Dwell Time	24 μs
Samples/Dwell	2 1/4
Background Rate (N_b)	3×10^9 Carriers/sec per Detector
Focal Plane Temperature	77°K
Power Dissipation on Focal Plane	1W

Table 1. Prototype FLIR System Specifications

The preamp is followed by a correlated double sampling (CDS) circuit[6] which suppresses kTC noise on the detector sense line and 1/f noise in the preamp. The signal from the CDS circuit is applied to the input of a CCD TDI consisting of a 16 stage charge transfer shift register which is connected to a 48 stage CCD TDI register through parallel transfer gates. Charge in the TDI register is advanced one stage each time the shift register is filled, thereby matching the oversampling rate of the detectors. The AC couple/DC restore operation is accomplished at the TDI output and the 24 channels are combined in a charge transfer output multiplexer. This configuration is a fully parallel implementation (necessitated by sampling rate considerations) of the focal plane processor concept discussed by Milton and Hess[1].

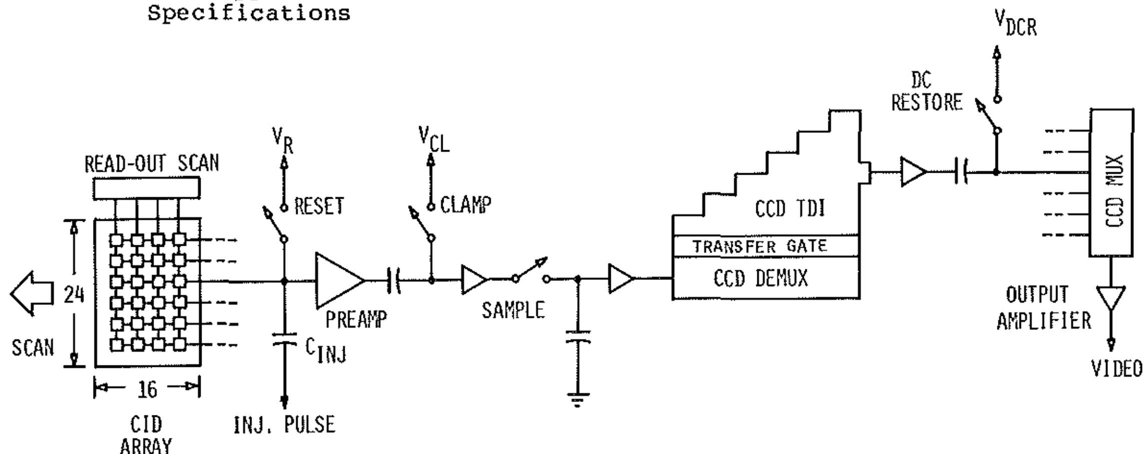

Figure 1. Block Diagram Showing the Components of the Silicon Processor Chip

The low noise preamplifier is an NMOS design with negative feedback employed for small signal gain and DC operating point stabilization. Significant aspects of the preamplifier design include: 1) low noise operation with the limited power budget required for on-focal-plane applications; 2) sufficient bandwidth and slew rate to allow settling of transients due to detector control pulses; 3) sufficient linear range to accommodate typical NMOS threshold voltage variations.

III. PROCESSOR DESIGN

The processor circuit is composed of six functional units, as can be seen in the block diagram of Figure 1: 1) detector signal line control, 2) preamplifier, 3) CDS, 4) TDI, 5) AC couple/DC restore, and 6) output multiplexer. In this section we discuss the details of the design considerations and resulting circuit configurations for each functional unit.

Detector Signal Line Control

Operation of the CID detector illustrating the detector control circuitry is shown in Figure 2. When a particular address line A_n is enabled by the read-out scan register, the integrated signal charge Q_s is transferred into the potential well beneath the CID electrode connected to the detector signal line. This causes a change in the signal line voltage proportional to Q_s, however the signal is not sensed at this time. Rather, the Reset Switch is closed briefly which sets the signal line voltage to the reference level V_R, and therefore the surface potential beneath the CID electrode to ϕ_R. Shortly thereafter, an injection pulse is applied through C_{inj} which collapses the potential well and causes Q_s to be injected into the substrate.

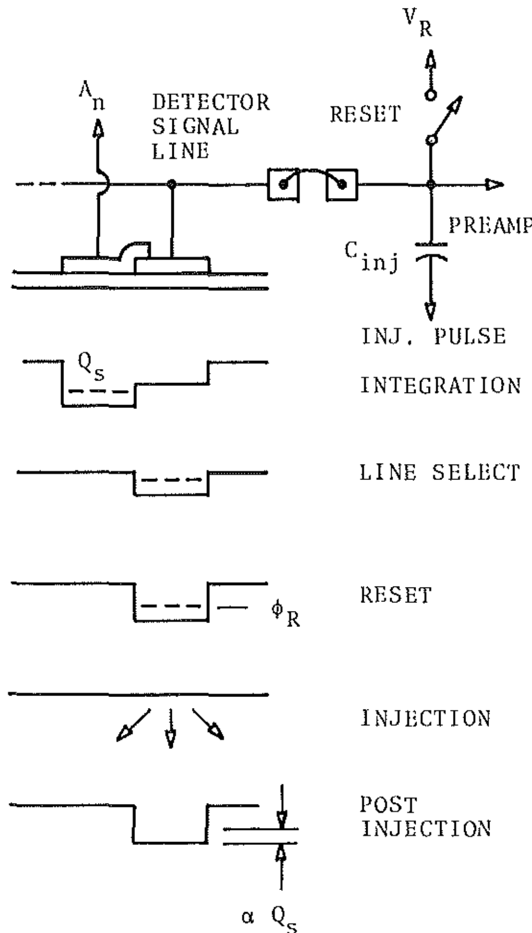

Figure 2. CID Operation by the Processor Chip Control Circuit.

When the switching transients due to the injection pulse have settled out, the surface potential beneath the CID electrode, and hence the signal line voltage, will have changed by an amount proportional to Q_s. At this point the preamplified signal is sampled. The operation described above occurs synchronously with the operation of the CDS circuit (to be described later) in order to suppress the well known kTC noise on the detector signal line due to the reset operation.

The value of C_{inj} must be sufficiently large to allow modest requirements for the injection pulse amplitude which is capacitively divided between C_{inj} and the total input node capacitance (the sum of the detector sense line capacitance and the preamplifier input capacitance). On the other hand, large values of C_{inj} cause increased loading of the input node with a corresponding decrease in signal voltage since the maximum charge in packet Q_s is limited by detector geometries and the signal voltage at the preamplifier input is:

$$V_{sig} = \frac{Q_s\ C_o}{C_D(C_0 + C_T) + C_o\ C_T}$$

where C_o is the detector electrode oxide capacitance, C_D is the depletion capacitance and C_T is the total signal line capacitance which includes the preamplifier input capacitance and C_{inj}. This signal attenuation results in a lower input referred noise requirement for the preamplifier in order to obtain background limited performance.

Choice of design parameters for the Reset Switch transistor involves similar considerations. The W/L ratio must be sufficiently large to allow completion of the reset operation in the time allotted (50 ns) with reasonable control pulse amplitudes. However, the gate-drain capacitance adds directly to the total signal line capacitance C_T and a minimum gate width is desirable.

Low Noise Preamplifier

The low noise NMOS preamplifier is the most critical component of the silicon processor and consequently presents the most challenging design problem. Of the several configurations considered, the one shown schematically in Figure 3 appeared the most immediately promising in terms of meeting the design goals.

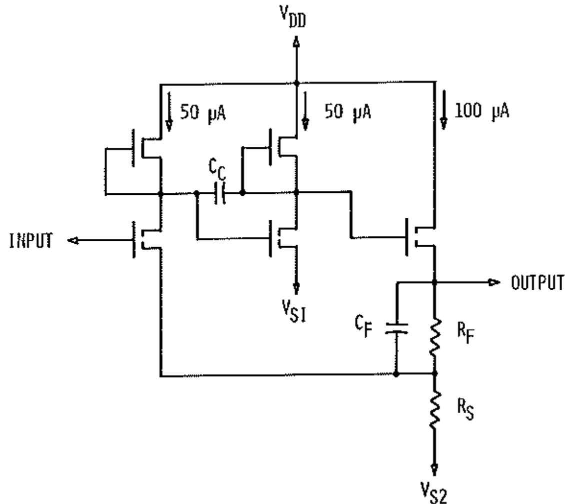

Figure 3. Schematic of the Preamplifier.

The circuit consists of a pair of cascaded inverters with a subsequent source follower stage which provides the low output impedance required for proper operation with the CDS circuit and negative feedback to the first stage for AC gain and DC operating point stabilization.

Although gain and bandwidth were important considerations in this design, the key trade-off is between noise performance and power dissipation, the latter being extremely limited due to the constraints imposed by on-focal plane operation. The dominant soures of Johnson noise are the input transistor and the feedback resistor, R_s. The input referred Johnson noise generated in the input transistor is given by:

$$e_n = (8kT/3g_m)^{1/2} \quad V/Hz^{1/2}$$

The improvement in MOS transistor parameters at low temperatures is primarily due to the increase in surface mobility which results in an increase in g_m. Thus, on-focal plane operation of the processor chip at 77°K results in a decrease in input referred noise by a factor of 4-6 relative to 300°K operation.

The Johnson noise generated in the input transistor when operated in the saturation region is approximately given by:

$$e_n = \left(\frac{8kT}{3}\right)^{1/2} \left(K' \, I_D \, \frac{W}{L}\right)^{-1/4}$$

where $K' = 2 \, \mu s \, \varepsilon_{ox}/t_{ox}$.

The drain current I_D is constrained by the limited power dissipation, and the W/L ratio by device area, photolithographic limitations, and short channel effects accompanying very small gate lengths. The value of R_s is limited by power dissipation and linear operating range considerations. The linear operating range must be sufficient to accommodate expected NMOS threshold variations, thus the amplifier output node must be capable of $\pm$ 4 volt swings about a nominal value. This results in a nominal 4 volt drop across $R_f + R_s$, thereby dictating the minimum drain current in the source follower stage. Since the ratio R_f/R_s determines the amplifier gain, a decrease in R_s requires the same percentage decrease in $R_f + R_s$ and results in an increase in the source follower drain current.

Assuming equal noise contributions from the input transistor and R_s, the design trade-offs can be accommodated (to first order) by the following:

1) Determine value of R_s based on

$$8kTBR_s = e_n^2$$

where e_n is the desired input referred noise in volts/$Hz^{1/2}$ and B is an estimate of the preamplifier bandwidth.

2) Determine source follower drain current from a nominal 4 volt drop across $R_f + R_s$, with R_f determined by R_s and the desired gain.

3) Apportion the remaining supply current equally between the inverter stages and determine the W/L of the input transistor such that the Johnson noise component is equal to that due to R_s.

4) Determine whether the resulting design meets gain, bandwidth and area requirements. If not, increase e_n and repeat the procedure from 1).

The amplifier circuit obtained from the cycle described above may differ from design goals in noise performance, but furnishes an initial set of device parameters which can be further massaged to provide optimum performance.

Table 2 summarizes the design goals and the predicted performance of the final preamplifier design based on computer simulation with device models appropriate for 77°K operation. The design goal for input referred noise performance is based on the background rate given in Table 1, an estimate of the total input capacitance (8 pF) and a 4 MHz preamplifier bandwidth. The predicted preamplifier noise performance is the best effort based on circuit area restrictions imposed by a conservative estimate of ultimate chip dimensions. The preamplifier bandwidth is primarily determined by its transient response to the injection pulse which occurs at a 1.48 MHz rate with an estimated duration of 85 ns. Proper operation of the CDS circuit requires that the preamp transients settle out within approximately 300 ns.[7] The preamplifier voltage gain is based on an estimate of the minimum value required to match the noise characteteistics of the following stages (CDS, TDI, and multiplexer).

Parameter	Goal	Predicted
Input Referred Johnson Noise	1.8nV/$Hz^{1/2}$	2.9nV/$Hz^{1/2}$
Power Dissipation	4 mW	4.1 mW
Bandwidth	Optimum	4.3 MHz
Gain	Optimum	40

Table 2. Preamplifier Design Goals and Predicted Performance.

Correlated Double Sampler (CDS)[6]

As shown in Figure 1, the CDS circuit is a straightforward implementation utilizing NMOS source follower stages to isolate and buffer the clamp and sample operations. Key design considerations include the selection of values for the clamp and sample capacitors which must be sufficiently large so as to maintain the kTC noise associated with the clamp and sample operations below the noise level at the amplifier output. In addition, the transistors utilized in the source followers are designed with as large a gate area as is practical in order to reduce the 1/f noise generated in these devices.[8] Power dissipation in the CDS circuit is predicted to be 0.2 mW.

Time Delay and Integration (TDI)

The function of TDI is to increase the signal-to-noise ratio of the detector output by integrating the response of each detector element over a number of samples. In the case of a scanned array, consecutive samples from each detector element must be delayed before integrating to account for movement of the scene relative to the detector array. CCD

structures have been designed to delay and add the parallel signals from a number of serially scanned detectors to produce a serial video output with enhanced signal-to-noise.[5,9] For these applications the detector signals are continually loaded in parallel into a CCD register as the CCD is clocked with the result that the signal from each detector is added in the CCD to delayed signals from each other detector. The CCD clocks must be synchronized with the mechanical scan of the array.

The CID array effectively multiplexes the detector signals. So the TDI structure must incorporate a demultiplexer in order to permit parallel entry of the detector signals into the summing register. Oversampling the detectors further complicates the design.

The TDI circuit for the processor chip is a CCD structure consisting of a 16 stage analog shift register coupled to a 48 stage TDI (summing) register through a set of parallel transfer gates. Although the detectors are sampled 2 1/4 times per dwell in the TDI (scan) direction, the detector spacing is adjusted to provide a 3:1 interleave for TDI. In other words, although the sampling rate is noninteger, the detector spacing and scan rate are such that every third sample occurs at the same "position" within each consecutive detector with respect to the image of a stationary point source.

Thus the analog shift register is filled with 16 samples at a 1.48 MHz rate (2 1/4 samples per 24 μs dwell time x 16 detectors in the TDI direction). These samples are transferred in parallel into the TDI register as the 17th sample enters the shift register. The charge in the TDI register is advanced one stage before the next 16 samples are loaded via the parallel transfer, etc. The operation is identical with that obtained from three individual 16 stage TDIs having inputs commutated every 16 samples and outputs 3:1 multiplexed. The resulting data rate at the TDI output is 92.5 kHz.

Primary considerations in the design of the TDI structure include kTC noise of the input and output circuits and 1/f noise of the source follower output buffer. The CCDs in the shift register and TDI register were designed as two phase devices with ion implanted wells. In addition, floating diffusions were used in the shift register in order to match the pitch of the TDI register. In order to maintain acceptable CTE in the shift register, transfer gate lengths must be carefully determined so as to minimize subthreshold leakage effects.[10] Figure 4 shows the channel stop and gate levels for the input circuit and first three stages of the CCD TDI structure.

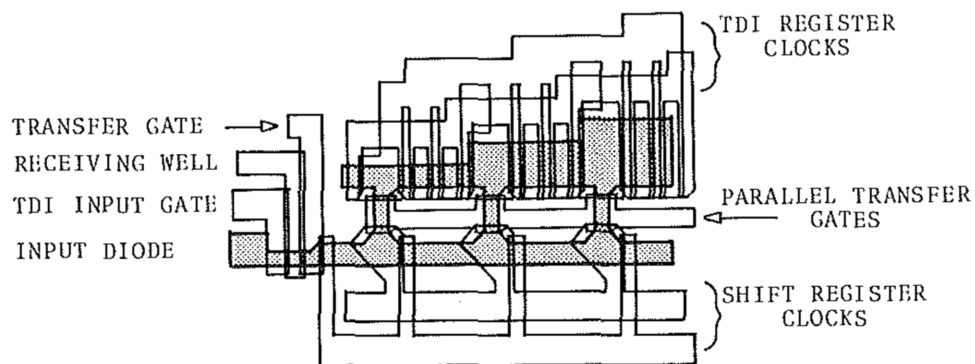

Figure 4. Channel Stop and Gate Levels For the Input Circuit and First Three Transfer Stages of the TDI Structure.

AC Couple/DC Restore and Output Multiplexer

DC restoration is accomplished by clamping the capacitively coupled multiplexer input via the DC restore switch shown in Figure 1. This operation removes all electronic offsets in the detector and processor circuits and, in addition, removes detector background response nonuniformities if a thermal reference is scanned by the detector array during the clamp.

The primary design consideration for the 24-channel output multiplexer is minimization of fixed pattern noise components commonly associated with CCD multiplexers due to MOS threshold voltage variations among the input circuits. A threshold-independent CCD input scheme has been described in the literature[11], however close examination revealed that it was not compatible with the AC couple/DC restore requirements. As a result, fixed pattern offsets introduced by the multiplexer will have to be "processed out" further down the signal processing chain.

A secondary design consideration involved matching the pitch of the multiplexer to the spacing of the processor channels. As in the TDI, this was accomplished with floating diffusions. The dominant noise sources include kTC noise in the multiplexer input and output circuits and 1/f noise in the output buffer amplifier.

Channel stop and gate levels for the AC couple/DC restore circuit and the multiplexer input circuit/transfer cell are illustrated in Figure 5. The multiplexer is a dual channel, two phase, phase multiplexed structure which reduces the clock rate in each channel. The AC coupling capacitors are the rectangular structures just above the restore switch transistors.

IV. PROCESSOR FABRICATON AND TESTS

The silicon processor chip has been fabricated using a double level, self-aligned polysilicon gate CCD/NMOS process. A photomicrograph of the completed chip appears in Figure 6. The output multiplexer is the vertical structure in the center of the chip. The interconnecting diffusions can be seen extending between the input circuit/transfer cells.

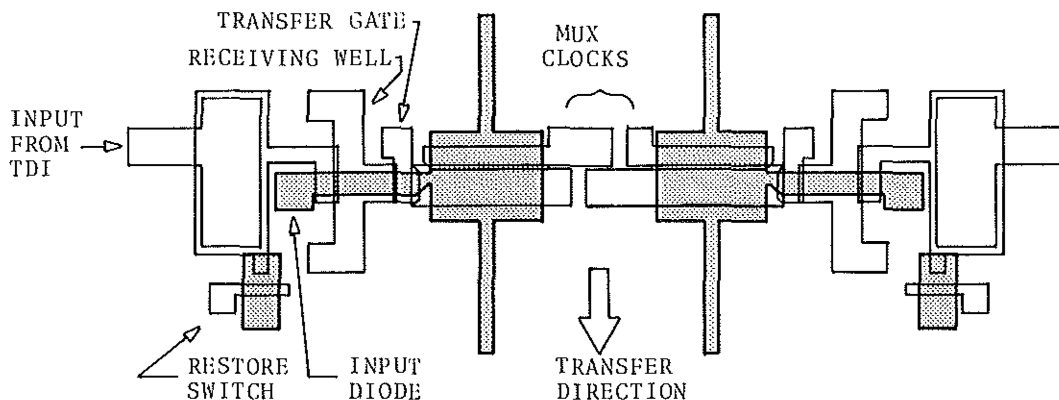

Figure 5. Channel Stop and Gate Levels for the AC Couple/DC Restore Circuit and Multiplexer Input Circuit/Transfer Cell.

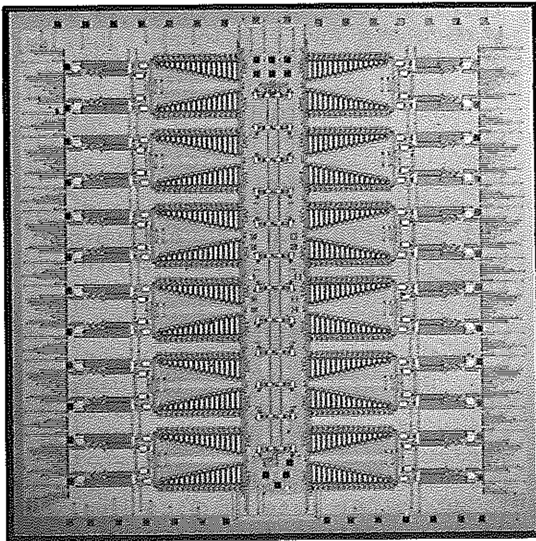

Figure 6. Photomicrograph of the Processor Chip.

As in any IC design incorporating moderately high circuit densities, a key design problem is interconnection of the various circuit components and routing of control and signal lines. Although this problem is somewhat alleviated by the highly parallel organization of the processor circuits, a considerable amount of effort was expended in laying out the interconnects, with special attention paid to avoiding control line - signal line crossovers.

An enlarged view of the chip showing more component detail appears in Figure 7. In addition to the processor chip, a test chip was designed and fabricated which includes each of the major components as separately bondable test structures. This allows full characterization of each of the individual components at 77°K with small laboratory liquid nitrogen dewars and considerably less equipment than is required to support operation of the full processor.

Preamplifier Test

The low noise preamplifier test structure includes an additional source follower stage as an output buffer in order to drive the large parasitic output capacitance associated with packaging and testing. The measured gain and noise performance of the test structure at 300°K and 77°K are presented in Figure 8. Preamplifier performance at 300°K agrees to within expected limits with predicted performance obtained from computer simulations. Performance at 77°K, however, is severely degraded. The 3 dB bandwidth is approximately 2 MHz and the input referred noise level is 5 $nV/Hz^{1/2}$ as compared with predicted values of 4.2 MHz and 2.9 $nV/Hz^{1/2}$ respectively.

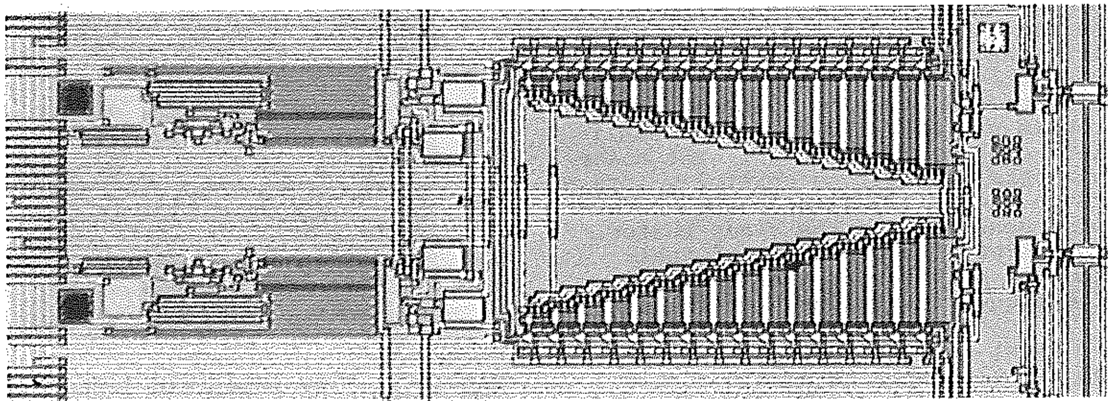

Figure 7. Enlarged View of the Processor Chip Showing Component Detail.

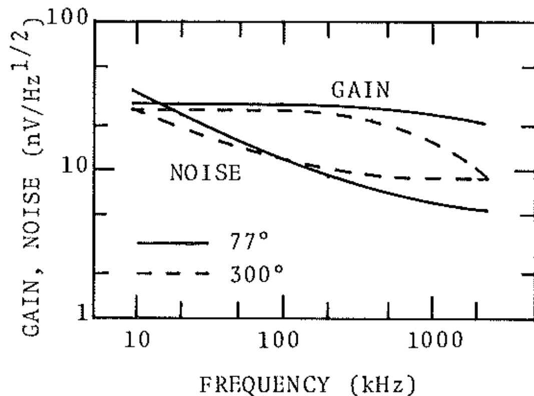

Figure 8. Voltage Gain and Input Referred Noise in the Preamplifier at 300°K and 77°K.

Further analysis indicates the source of the problem to be improper modeling of the temperature dependence of depletion load device parameters. This has resulted in a considerable decrease in DC drain currents in the first two stages, thereby causing an increase in noise and a decrease in small signal bandwidth and slew rate.

CDS Tests

The CDS test structure does not include an additional output buffer stage, and was tested at lower operating rates than required in the processor due to the large parasitic output capacitance. Proper operation of the circuit at 77°K has been observed. Since the depletion load devices in the source follower stages are externally biased, the low temperature problem (as observed in the preamplifier) can be circumvented. The noise data obtained must be carefully interpreted due to aliasing of the Johnson noise generated in the clamp buffer stage since the bandwidth of that stage is much larger than the operating frequency utilized for the tests.

Test results indicate that the CDS circuit exhibits a gain of 0.8 and operates satisfactorily with the required 50 ns clamp and sample pulse widths. The Johnson noise level referred to the CDS input is measured with clamp and sample switches closed and is less than 30 $nV/Hz^{1/2}$. The 1/f spot noise is 65 $nV/Hz^{1/2}$ at 10 kHz. The wideband (integrated over the Nyquist interval) kTC noise component was determined by subtracting the aliased Johnson noise component from the total input referred noise and was determined to be approximately 60 μV rms, well within processor requirements.

TDI Tests

Operation of the TDI device at 300°K is illustrated in Figure 9 which shows time delay and integration of a rectangular pulse. The shift register clock rate is 1.48 MHz resulting in an output rate of 92.5 kHz. Figures 9a and b correspond to pulse durations of less than 48 TDI register clock cycles while the input pulse in Figure 9c is greater than 48 cycles long. Voltage gain through the TDI is nearly unity, and measured wideband noise is approximately 260 μV rms at room temperature.

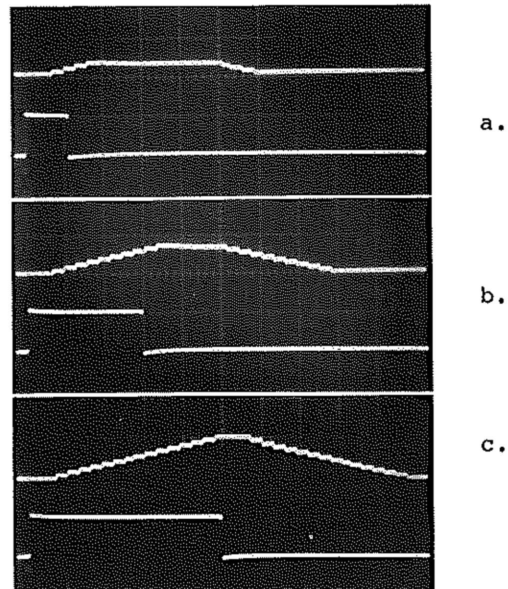

Figure 9. Time Delay and Integration of a Rectangular Pulse. (Top: TDI Output, .5V/div; Bottom: Input Waveform, .5V/div; Horiz: 0.1 ms/div).

Calculation of the predicted noise performance of the TDI indicates that it should be dominated by kTC noise resulting in a wideband output noise level of less than 100 μV rms. However, these calculations neglected the floating diffusion "bucket-brigade" type transfer as a potential noise source. An analysis of the bucket brigade transfer mechanism shows that the variance in the number of charges transferred at each transfer is [12]

$$\langle \zeta^2 \rangle = kTC_{FD}/q^2$$

where C_{FD} is the capacitance of the floating diffusion. The value of C_{FD} is calculated to be .069 pF from geometrical considerations, resulting in 106 noise electrons per transfer at room temperature. Since each consecutive charge packet contributing to a single TDI output charge packet experiences an additional transfer through a floating diffusion, the resulting variance on the output charge packet is

$$\langle \zeta^2_{out} \rangle = \langle \zeta^2 \rangle [1+2+3+\cdots 16] = 136 \langle \zeta^2 \rangle$$

Since adjacent charge packets in the shift register are separated by two interleaved packets in the TDI register, a strong correlation will exist between charge packets Q_n and Q_{n+3} resulting in peaks in the noise spectral density at odd multiples of $f_{clock}/6$.

The expression for the single sided noise spectral density as measured at the TDI output is [12]

$$S(f) = \frac{2}{f_c} \left(\frac{q}{C_{out}}\right)^2 \langle \zeta^2_{out} \rangle (1-\cos 6\pi f/f_c)$$

where f_c is the TDI register clock rate and C_{out} is the value of the output node capacitance. The sinx/x aperture function of the sample and hold output has been neglected. Inserting the appropriate numerical values (C_{out} = 0.7 pF, f_c = 92.5 kHz) yields

$$S(f) = 1.73 \times 10^{-12} (1-\cos 6\pi f/f_c).$$

Figure 10 compares the noise spectrum measured at the TDI output for normal operation with the expression above, and also shows the output circuit kTC noise level which was measured by disabling the TDI input circuit.

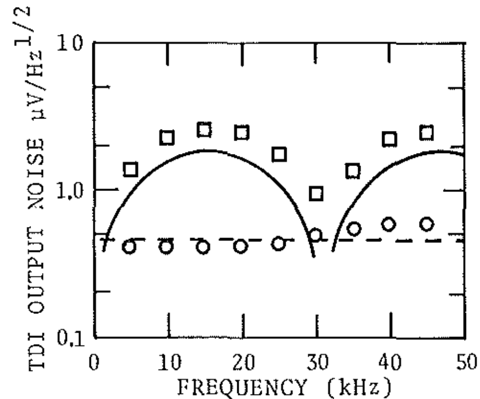

Figure 10. TDI Output Noise Spectrum. (Solid Line: Theoretical Transfer Noise, Dashed Line: Predicted kTC Noise, Measured values are indicated by squares and circles, respectively).

Figure 11 illustrates the "point source" response of the TDI. This is obtained by application of a properly synchronized 16-unit pulse train in order to integrate all 16 samples into a single charge packet. (Note that in actual operation, a point source would result in a TDI output signal which is 3 cycles in duration, due to oversampling of the detectors.) The second pulse seen trailing the main output in the oscillograph is due to CTE effects in the shift register caused by the floating diffusions which interconnect CCD transfer cells. Using only first order terms, the ratio of the charge in the signal packet to that in the trailing packet is

$$\frac{\text{signal}}{\text{error}} = \frac{\sum_{n=1}^{16} (\text{CTE})^n}{\sum_{n=1}^{16} (1-\text{CTE})^n}$$

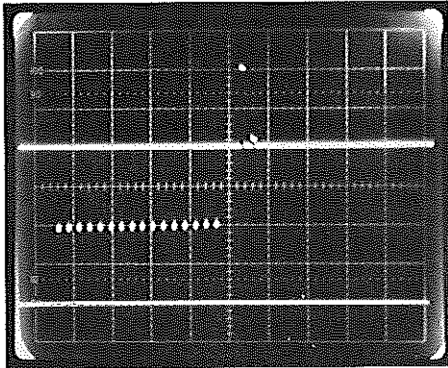

Figure 11. "Point Source" Response of the TDI from which CTE is Determined. (Top: TDI Output, 200 mV/div; Bottom: Input Pulse Train, 200 mV/div; Horiz: 0.1 ms/div).

The resulting calculation yields a value of approximately 0.99 for the CTE of the floating diffusion transfers.

Proper operation of the TDI device has been observed at 77°K, although a detailed analysis has not yet been performed due to excessive crosstalk among signal and control lines in the cables interconnecting the device and the test equipment.

Multiplexer Tests

Operation of the 24 channel output multiplexer at 300°K is demonstrated in the oscillograph in Figure 12 where a test signal has been applied to input number 13. Voltage gain through the device is approximately 0.14 due to a 5:1 mismatch between input and output capacitances (necessitated by the phase multiplexed design) and a voltage gain of 0.7 in the multiplexer output buffer amplifier. Figure 13 is an expanded view of the output waveform illustrating the fixed pattern noise component due to threshold voltage variations among the input circuits. Except for a large transient induced by the parallel transfer pulse (believed to be spurious coupling in the experimental set up), the fixed pattern variations are within an input referred range of ± 100 mV. This is at least a factor of two larger than the worst case expected, and further investigation is required to resolve the discrepancy.

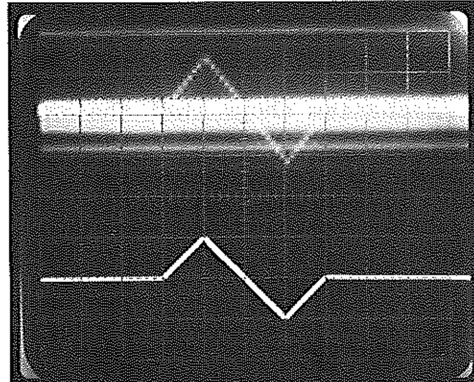

Figure 12. Multiplexer Response (Top: Multiplexer Output, 0.1V/div; Bottom: Signal Applied to Input Number 13, 1V/div; Horiz: 0.2 ms/div).

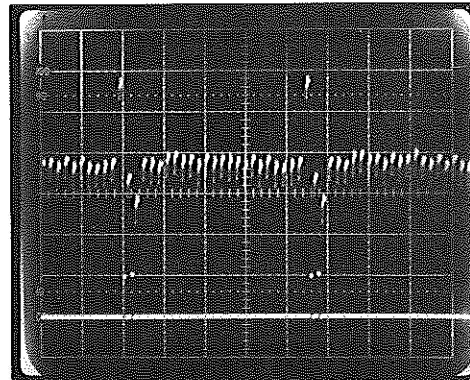

Figure 13. Detail of Multiplexer Response Showing Fixed Pattern Noise Component. (Top: Multiplexer Output, 0.1V/div; Bottom: Parallel Transfer Pulse, 10V/div; Horiz: 5 μs/div).

As in the TDI, the primary thermal noise source in the multiplexer is due to the bucket brigade transfers in the floating diffusions. CTE in the multiplexer is slightly better than in the TDI due to larger gate lengths which reduces the drain dependence of the subthreshold leakage.

The multiplexer has not been tested at 77°K, although operation of the output buffer amplifier is expected to be degraded due to the use of fixed bias depletion loads.

Processor Tests

Preliminary tests of the processor chip have been performed and have confirmed proper interconnection of the components. Although detailed tests to evaluate the performance of the processor have yet to be accomplished, preliminary evaluation of a single processor channel at 300°K has been accomplished by interconnecting the individual preamplifier, CDS and TDI test structures on the test chip.

The input waveform for these tests was generated with an external clamp/sample circuit in order to provide a reference level for the CDS clamp operation. Although the test structures utilized were on the same chip, they were interconnected externally, and the input sample rate was reduced to 148 kHz to accommodate parasitic capacitance. Figure 14 shows the input signal, CDS output and TDI output waveforms corresponding to the maximum signal amplitude for linear operation of the TDI. The voltage gain through the preamplifier and CDS circuits is approximately 10 due to the additional source follower in the preamplifier test structure and high bias levels in the CDS source followers required to obtain sufficient bandwidth.

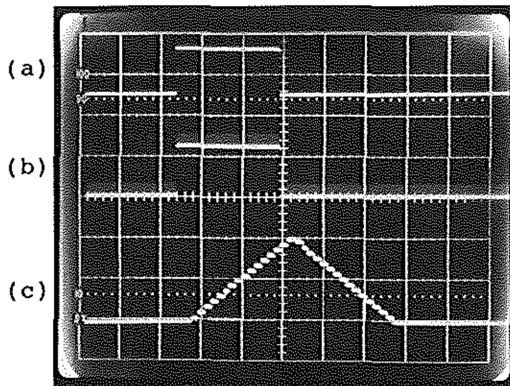

Figure 14. Response of the Processor Channel Test Circuit. (a) Input Signal, 50 mV/div. (b) CDS Output, 500 mV/div. (c) TDI Output, 500 mV/div. Horiz: 2 ms/div.

Figure 15 shows the CDS and TDI output waveforms when the test signal is reduced in amplitude by 40 dB. The smeared appearance of the TDI output waveform is due to droop in the sample and hold circuit connected to the TDI output in order to reduce clock feedthrough. This effect is shown in the expanded portion of the TDI output waveform. The wideband noise measured at the TDI output is approximately 520 μV rms and is generated within the TDI structure (confirmed by shortng the TDI input to ground). The primary noise component is due to the bucket brigade transfer discussed earlier, as was evidenced by observation of the characteristic noise spectral density function for that noise source. The resulting dynamic range observed in the TDI is 65 dB (peak signal to rms noise).

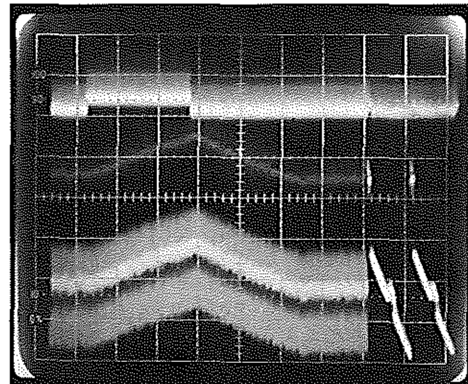

Figure 15. Response of the Processor Channel Test Circuit with Input Waveform Attenuated by 40 dB. (Top: CDS Output, 20 mV/div; Bottom: TDI Output 10 mV/div; Horiz: 2 ms/div, 100 μs/div)

The wideband noise measured at the CDS output is approximately 430 μV and is primarily due to aliasing of Johnson noise components in the preamplifier and CDS circuits.

V. DISCUSSION

The noise performance of the processor channel test circuit is dominated by transfer noise generated in the TDI input shift register. This will remain the dominant thermal noise source in operation of the processor chip. Although the gain of the preamplifier and CDS circuits is expected to increase by approximately a factor of 3, the noise in those circuits is expected to decrease by about the same amount due to a decrease in the noise aliased into the Nyquist interval. Input sample rates of from 500 kHz to 700 kHz should be possible at 77°K, with an input referred wideband noise level of approximately 14 μV - a factor of three higher than that required for background limited performance.

The transfer noise in the TDI can be improved by decreasing the capacitance (i.e, the area) of the floating diffusions. Although the geometry of the present design could be modified to reduce the area of the floating diffusions by a factor of 2 or 3, reduction by a factor of 20 to 30 is required to suppress the transfer noise level below the kTC noise generated in the TDI input and output circuit. The motivation for employing the floating diffusion interconnect was the reduced clock rate in the input shift register. This structure can be realized with a CCD shift register having the same cell pitch as in the TDI register and operating at a clock rate 48 times that in the TDI register, with the input circuit entering a charge packet every 3 clock cycles. The resulting clock rate in the input register is 4.5 MHz. Although this approach results in the potential for increased clock to signal crosstalk, it appears, in retrospect, to represent a lower overall risk in terms of processor noise performance.

Two key problem areas recognized in the early stages of this development program were related to preamplifier noise performance and multiplexer fixed pattern noise. Their status, in this regard, has not changed. The problem encountered with the depletion load devices in the preamplifier are quite disappointing, but hardly insurmountable. In addition, new amplifier configurations are currently under study which show much higher potential for low noise, low power operation than the circuit described here. Fixed pattern offsets in multichannel CCDs have been problematic to designers for years. The realities of tactical FLIR applications dictate an eventual analog-digital interface, and thus the possibility for "processing out" fixed pattern variations in the digital processor. The main requirement is that the fixed pattern offsets be sufficiently small - say, a few percent of the peak signal - so as not to degrade processor accuracy when the scene contrast is low.

In summary, although unexpected problem areas have been encountered, it is felt that low risk solutions are available. The result of this silicon processor development is a confirmation of the applicability of analog NMOS/CCD circuits to on-focal plane signal processors for intrinsic CID detector arrays. Further work in this area is unquestionably required, in order to more carefully analyze the performance of the present processor configurations and to define the optimum architecture for future processors.

ACKNOWLEDGEMENT

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