# A NEAR IR PIN/CCD DETECTOR ARRAY

G. H. Hershman, D. O. Massetti*
Hughes Aircraft Industrial Products Division, Carlsbad, Ca.

D. H. Alexander, G. Domingo, K. Williams
Hughes Aircraft Tactical System Division, Culver City, Ca.

ABSTRACT. A PIN diode array to detect near IR radiation has been designed, fabricated and tested. The array uses a charge transfer device signal readout mechanism and is optimized for the 0.7 to 1.0 μm band. The array consists of 160 detectors. Data is presented in this paper on the design considerations and test results. Quantum efficiencies of better than 80 percent have been measured with antireflection coated devices. Measured crosstalk between detector elements on 1.65 mil centers was 4 percent and detector response was uniform within 10 percent. The device operated nominally at a 20 kHz frame rate with detector integration times variable from 0.5 to 50 μs. All measurements in this paper were performed at a temperature of 300°K.

## I. INTRODUCTION

The need for high responsivity detectors in the near IR region of the spectrum has recently led to increased interest in intrinsic (ρ = 1000 to 20,000 ohm cm) silicon deep depletion devices. In particular, several 1.06 μm wavelength laser target designator systems are now utilizing silicon PIN detectors. Although the number of such applications have increased dramatically in the past two years, all the devices fabricated to date have been relatively simple structures, typically one to four PIN detectors per chip. The coupling of PIN detectors with a CCD type readout offers several advantages such as multiple detectors per chip, denser, higher resolution detector arrays, multiplexed readout structures and on chip signal processing. Our efforts have concentrated on developing a novel multi-detector staring array with CCD readout for application in the 0.7 to 1.0 μm wavelength region.

Table 1

| Multi-Element Detector Chip Design Goals | |
|---|---|
| Spectral Region | 0.7 to 1.0 μm |
| Responsivity | >0.4 amps/watt |
| Crosstalk | <10 percent |
| Cell Size | 1.65 mils at center |
| Dynamic Range | $\geq 10^5$ |
| BLOOM Protection | 100X maximum signal |
| Individual Cell Sample Rate | 20 kHz |
| Noise | $<1\ \mu V/\sqrt{Hz}$ |
| Total Array Diameter | 148 mils |

## II. DESIGN CONSIDERATIONS

For most imaging applications, high resolution is desirable over the entire field of view, however, this leads in many cases to high bandwidth requirements. In addition to the bandwidth considerations, for a staring detector array using charge integration devices the frame time also becomes important from a dynamic range standpoint. Higher frame rates (>30 Hz) are desired for higher dynamic range, but

*Now with NCR; Colorado Springs, Co.

this increases the bandwidth required. For many imaging and tracking applications, high resolution is important only in the center of the field of view, thus the array design utilized high density, high resolution detector elements in the center and increasing larger, lower resolution detectors in the periphery. To allow good dynamic range, a frame rate of 20 kHz was chosen, while the bandwidth was kept very low (160 kHz) by using few number of detectors (160) and multiple readout lines (20). These parameters were chosen to be conservative due to the higher risk believed to be involved in the center unit cell layout. From design rule considerations this center array of high resolution detectors had a unit cell size of 1.65 x 1.65 mil.

This square array is surrounded by 6 annular rings which increase in size from the center to the periphery where high resolution is not required. Each ring contains 16 cells. The total of 160 cells are multiplexed onto 20 output busses, each buss having a separate output amplifier. The output buffers are located around the periphery of the chip. The use of 20 output amplifiers allows parallel off chip signal processing and consequently reduces the data rate of each line by a factor of 20. The total chip size is 198 x 198 mils which includes a large number of test devices in the 4 corners of the die as well as the 148 mil diameter main array.

Meeting the goals of high responsivity and low crosstalk for small cell size detectors is particularly difficult for the spectral region of interest (0.7 to 1.0 μm). This fact can best be appreciated by referring to Figure 1 which plots the normalized photon intensity versus penetration depth into a silicon detector for several wavelengths in the visible and near IR regions of the spectrum. At $\lambda = 0.9$ μm the photons penetrate deep into the substrate before being absorbed; e.g., 10 percent of the incident photons remain unabsorbed at a depth of 35 μm, 6 percent are unabsorbed at 45 μm. In order to maximize responsivity and minimize crosstalk, it is desirable to have the majority of the photons absorbed in the depletion region. Hence, the photon generated electron-hole pairs are immediately separated by the electric field and the appropriate carrier is collected to the detector. Photons penetrating

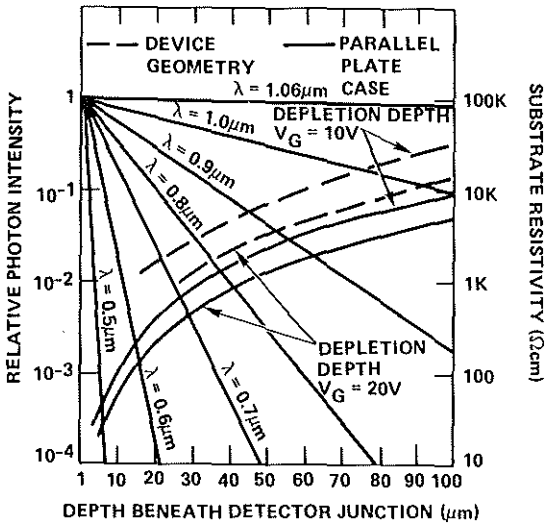



Figure 1. Decay at relative photon intensity for several wavelengths as a function of penetration depth into a silicon detector and depletion depth for voltages of 10 and 20 V as a function of substrate resistivity

deeper than the depletion volume create carriers in a field free region. Such carriers are free to migrate laterally which causes crosstalk. Furthermore, the recombination probability is much higher for carriers created in a nondepleted region which can result in a reduction in responsivity. Hence, meeting the crosstalk goal (10 percent) requires a depletion depth on the order of 30 to 50 μm. The depletion depths attainable for two MOS compatible voltages as a function of substrate resistivity are superimposed over the absorption curves in Figure 1. The solid lines in Figure 1 indicate the depletion depth versus bias of a one dimensional (parallel plate) detector geometry. For the actual geometries used in the device described in this paper, the depletion voltages are substantially higher as shown by the dashed lines in Figure 1, which represent the results of a two dimensional model of the device. Thus the geometry considerations further increase the demands on detector resistivity and for this device a goal of 8000 Ω-cm, which allows full depletion through a 50 μm material with a 10 volt bias, was chosen.

The design approach used to meet the goals of Table 1 utilizes a deep depletion, thinned, backside illuminated structure fabricated on a p-type high resistivity substrate. The backside illumination scheme allows 100 percent of the detector array's area to be optically active. The appearance of the completed array is shown in Figure 2.

The electrical equivalent circuit is shown in Figure 3. Each unit cell contains a PIN detector, a readout transfer gate and diffusion, and a bucket overload gate and drain. The Bucket Overload Protection (BOP) circuitry is required to prevent bloom at high illumination levels. Also the BOP can be used to vary the integration time of the detector pulsing the BOP gate. As illustrated in Figure 3, eight detectors are multiplexed onto a floating diffusion output buss which is connected to the input gate of a two stage N-MOS source follower amplifier.

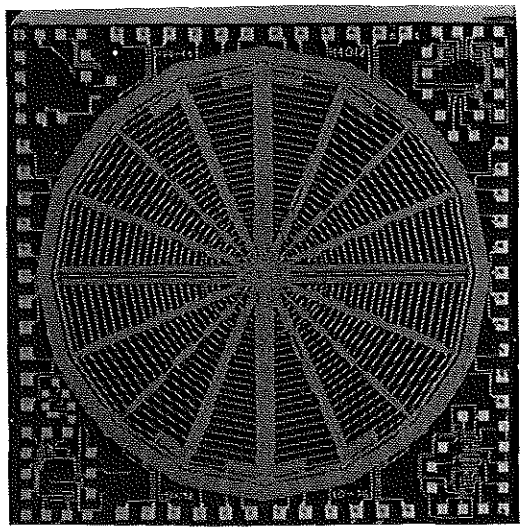


Figure 2. Photograph of a die containing the monolithic PIN/CCD array

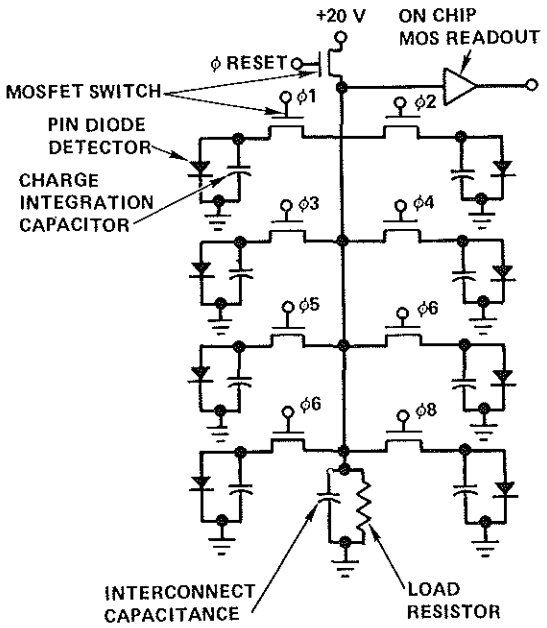



Figure 3. Electrical equivalent circuit of one line of 8 detector elements

## III. DEVICE OPERATION

The device operates as follows. The floating $n^+$ anode of the PIN detector is set to a potential of approximately 15 volts which is sufficient to deplete the entire substrate thickness. Photon generated hole electron pairs are separated by the depletion field and the electrons are collected to the diffusion and are stored in an inversion layer under the bias gate. As the storage "bucket" fills with charge the potential on the floating diffusion decreases. Thus it is important that the initial voltage be high enough such that the substrate remains depleted under full well condition. If this is not the case, crosstalk will result. The stored charge packet is transferred from the storage gate to the

output node by addressing the proper transfer gate. The transfer of the negative charge packet to the floating output node causes the potential of the node to fall and the output amplifier responds. After the transfer gate is turned off and the output settles, the output node is reset to 20 volts by the MOS switch. Since 8 detectors are multiplexed onto one output bus, eight transfer gate clocks are required along with a reset clock and a sample and hold clock. The sample and hold transistor in the output amplifier is used to give a cleaner and longer response. The bucket overload gates perform a dual function. In addition to bloom protection, the gates can be clocked to vary the cell integration period which increases the dynamic range under strong signal conditions.

## IV. EXPERIMENTAL SET UP

Characterization of array operation concentrated on the following parameters which were used to form a data base for analyzing the array operation:

1. Uniformity
2. Crosstalk
3. Responsivity
4. Frequency Response
5. Dynamic Range
6. Noise
7. Bucket Overload Protection
8. Detector Integration Time Variation
9. Array Transfer Properties

Testing of the detector array was performed on an optical bench. A modulated LED source was used that emitted in the wavelength range of 0.6 to 1 μm with a maximum at 0.9 μm. Modulation of the light was accomplished by means of a variable speed chopper which gave a modulation range of 50 Hz to 10 kHz. In front of the chopper a variable size aperture was used to vary the optical intensity and to decrease the spot size to less than 25 μm. To focus the source onto the detector array, a Nikor f/5, 63 mm lens was used. The chip was mounted on a motor controlled x-y translation table which permitted movement of the detector array relative to the optical spot. In front of the array, a Shott RG-5 spectral filter with 0.97 percent transmission between 0.7 and 1.2 μm, was used to screen out possible room light interference. All measurements were performed at room temperature.

Each detector could be individually monitored by choosing an output line with a 20 position output selector switch followed by an 8 channel sample and hold demultiplexer.

To obtain spot scans of the detectors, the array is moved across the focused spot of light and the output response of a single detector is monitored by a wave analyzer which drives the y axis on the x-y recorder. The x axis is the spot position given by a position encoder controlled by the x-y translation table. This is shown schematically in Figure 4. The resultant curve is a plot of a single detector response as a function of spot position on the detector. This scan is repeated for adjacent detectors to display detector response uniformity and crosstalk.

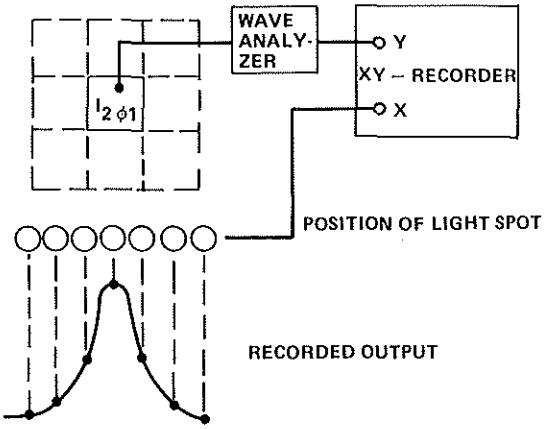



Figure 4. Schematic diagram of spot scan measurements of the PIN/CCD detector array

## V. EXPERIMENTAL RESULTS

### a. Output Devices

Each of the 20 video output lines had its own on chip output device as discussed previously. This output device was characterized using a separate test device of the exact same configuration. The results of this test are shown in Figure 5 for two values of gate bias on the MOS

source load resistors. Higher positive gate voltages increase the device conductance, reducing the source resistance which decreases gain and increases bandwidth. The gain bandwidth remained constant at about 300 kHz, more than sufficient for operation with 160 kHz video waveforms.

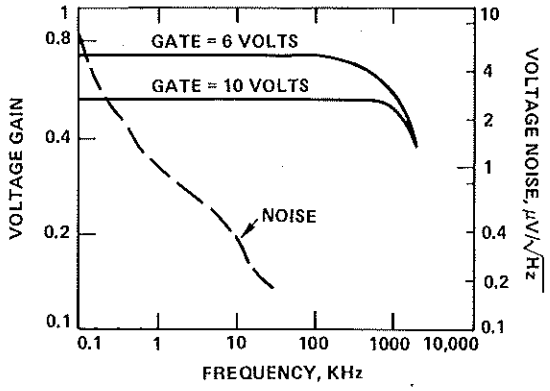



Figure 5. Gain and noise versus frequency of the dual source follower output

b. Detector Measurements

Measurements were made on response as a function of detector bias voltage using a 4 element linear test detector array of the same general configuration as the main array detectors. The test detector array consisted only of the n+ p detector, with no CCD readout. Measurements of these detectors was by means of a transimpedance amplifier. Figure 6 shows the measured detector response and cross talk (measured at the center of the adjacent detector) as a function of bias. Increasing the bias reduced the crosstalk from 8 percent to less than 2 percent for these test detectors, and increased responsivity as the detector base was further depleted. The response as a function of bias saturated above 10 volts at which bias the base was nearly fully depleted. This corresponds with the calculated value of 10V depletion for a 50 μm thick detector with a resistivity of 8000 Ω-cm as was shown in Figure 1.

c. Results of the Main Array

The output waveform of the array is shown in Figure 7. Figure 7a shows the output of one line with the focused spot (modulated at 1 kHz) centered on two adjacent detectors.

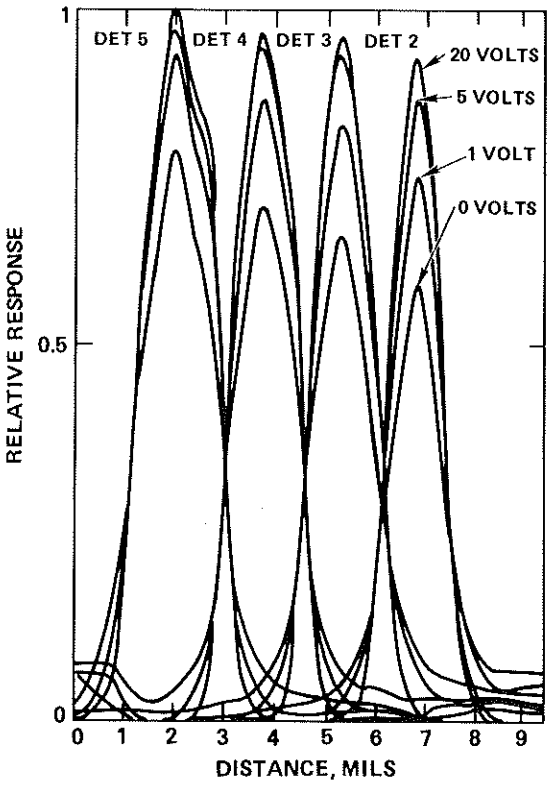
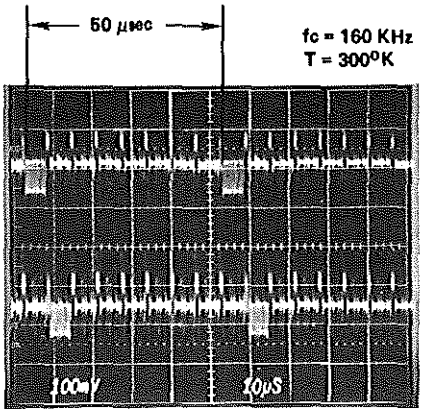


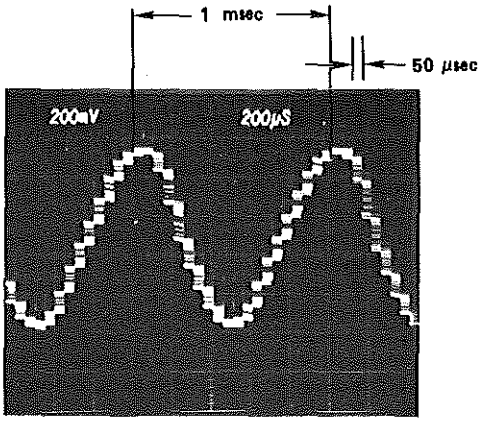

Figure 6. Relative response of test detectors as a function of bias

In each waveform the other 7 detectors are not illuminated. The output was kept valid for 85 percent of a full analog data bit period by a sample and hold circuit included in the on chip two stage source follower output device. Figure 7b shows the demultiplexed output waveform of one illuminated detector. The spread in amplitude of each sample interval is due to the aliasing of the 20 kHz sample rate with the unsynchronized 1 kHz signal.

A vertical spot scan of seven adjacent detectors in the center 8 x 8 portion of the chip is shown in Figure 8. As shown the uniformity is quite good with a standard deviation of 2.8 percent about the mean detector response. The spot scans shown have not been deconvolved to take out the optical blur of the focused signal, thus the spot scans show the total optical and electrical




a) WAVEFORM FROM ONE VIDEO OUTPUT (8 DETECTORS). THE TOP TRACE SHOWS THE RESPONSE OF A FOCUSED SPOT ON DETECTOR NO. 5, AND THE BOTTOM TRACE SHOWS THE OUTPUT WITH THE SPOT ON DETECTOR NO. 6.




b) DEMULTIPLEXED OUTPUT OF ONE DETECTOR SHOWING A SINGLE DETECTOR RESPONSE TO A SIGNAL MODULATED AT 1 KHz.

Figure 7. PIN/CCD array output waveforms

crosstalk to be less than 3 percent at the center of the adjacent detectors. Due to an open aluminum addressing line on this die, the eighth detector in the center array was not operational.

The scanned optical response of the ring detectors is shown in Figure 9. The

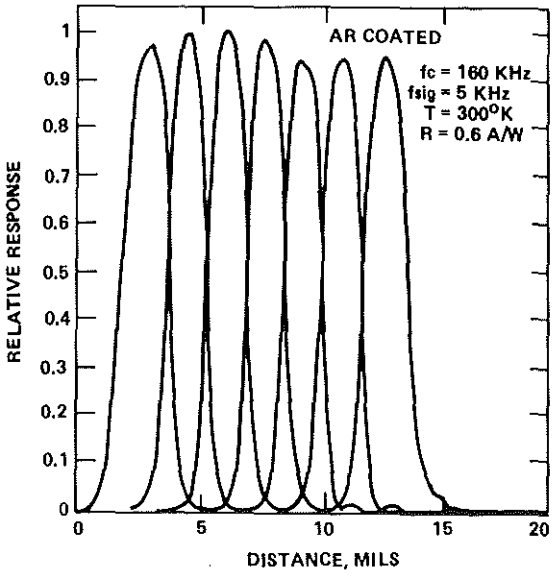



Figure 8. Vertical spot scan of detectors in the center 8 x 8 detector area

response of each successive ring decreases because the larger input capacitance of the dual source follower on the larger detectors of the outer rings decreased the transimpedance of the output devices. The structure in the responsivity within one detector area is due to the cross section of the ring array detectors. The second ring was not operational.

Figure 10 compares the response of the arrays with two different dopings. The array fabricated on a 8KΩ-cm substrate shows an increase in response by a factor of 4 and a decrease of crosstalk (from 15 to 4 percent) over the same array constructed on a 100 Ω-cm substrate. To fully deplete 50 μm of a 100 Ω-cm silicon a voltage of 200 volts is needed while only 10 volts is required to deplete the 8000 Ω-cm material. Since 15 volts were applied to both arrays the 100 Ω-cm was not fully depleted resulting in low quantum efficiency and higher crosstalk.

d. BOP Operation

As described in Figure 3, the BOP circuit can be used to vary the integration time of the detector element. The response as a function of integration time is shown in

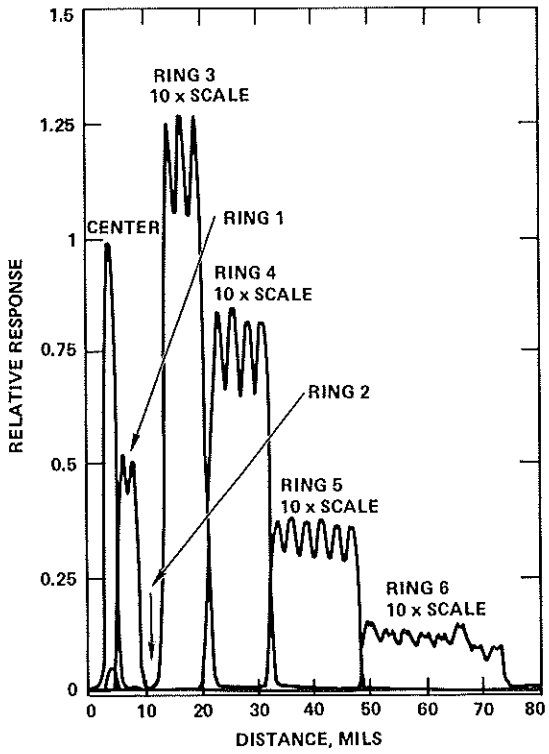



Figure 9. Spot scan response of the ring detectors

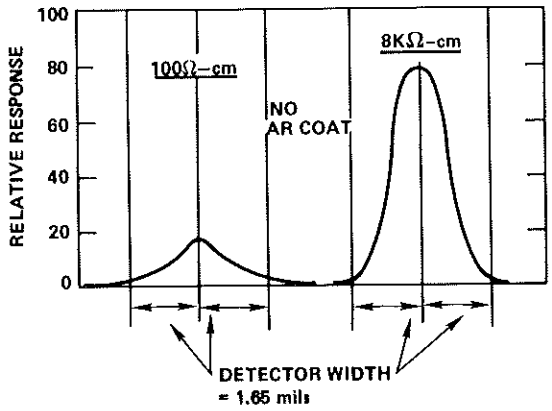



Figure 10. Spot scan of detectors with two different base dopings

Figure 11, the response is linear over two orders of magnitude integration time variation from 0.5 to 50 μs. This allows a

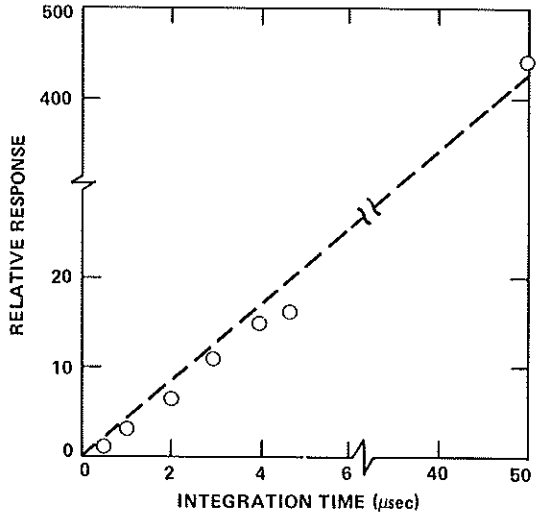



Figure 11. Relative response of detectors as a function of integration time (BOP)

dynamic range increase of a factor of 100 and provides the $10^5$ overall dynamic range required in the design goals.

## VI. CONCLUSIONS

A summary of the device operation is shown in Table 2 for a 8000 Ω-cm AR coated backside illuminated array and compared with design goals. Responsivity of 0.6 A/W was measured on the PIN/CCD detector elements with a variation of 10 percent. Crosstalk was 4 percent. The output voltage noise at 5 kHz was 600 nv/$\sqrt{\text{Hz}}$ which gave a noise equivalent intensity (NEI) of $1.62 \times 10^{-14}$ w/cm$^2$ measured on the 8 x 8 center portion of the array. Ring detectors yielded higher values of NEI due to the lower transimpedance as was shown in Figure 9 which caused the noise of the ring detectors to be limited by the on chip output device noise.

In summary, all the design goals of this device were met or exceeded during characterization of the completed PIN/CCD detector arrays. Processing problems initially encountered were solved. Processing with an EPI-MOS process on high resistivity silicon substrates was shown to give good device operation with no degradation in substrate characteristics. Some problem was encountered with aluminum step coverage and soft diode breakdown,

Table 2. Summary of PIN/CCD detector Array Performance

| | Design | Measured |
|---|---|---|
| Resistivity (KΩ-cm) | 8 | 8 |
| Responsitivity (amp/W) | >0.4 | 0.6 |
| Noise at 5 kHz ($\mu v/\sqrt{Hz}$) | <1 | 0.6 |
| NEI ($w/cm^2$) | $<3 \times 10^{-14}$ | $1.62 \times 10^{-14}$ |
| Crosstalk | <10% | 4% |
| Uniformity | <15% | 10% |
| Integration time (μsec) | 0.5 to 50 | 0.5 to 50 |
| Amplifier gain | 0.7 | 0.7 |

causing some devices to give only partial operation. Device thinning to 50 μm was successful and allowed full depletion of the array to give a quantum efficiency of better than 80 percent with AR coating in a unit cell size of 1.65 x 1.65 mil. Feasibility of a 20 kHz frame rate array detecting near IR light (0.7-1.0 μm) using high resistivity silicon detectors and a charge transfer readout device in a monolithic format has been fully demonstrated.

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