"MINIATURE CCD CAMERAS"

Jack M. Younse H. Dean Mercer Roland W. Gooch

Texas Instruments Incorporated, Dallas, Texas 75265

ABSTRACT

Texas Instruments has developed a series of miniature charge coupled device (CCD) cameras. The motivation behind and application of each camera has been different. Described here are two cameras from this series, which demonstrates the broad range of TI camera technology. Discussed first is a 327 x 490 pixel TV compatible camera which can be used for applications requiring a TV format. Described next is a 48 x 24 pixel time delay integration (TDI) camera which can be used for scanning applications. Although some of the cameras in this series have utilized 3-phase, backside illuminated CCDs, both cameras described here utilize 2-phase, buried channel, frontside illuminated CCDs which were designed and fabricated specifically for these cameras.

Special features of these cameras include:

- Two-phase, frontside illumination
- Buried channel technology
- High charge transfer efficiencies in excess of 0.9999
- Antiblooming control (TIC-5)
- High resolution
- Standard 525-line TV format (TIC-5)
- Time-delayed-integration operation (TIC-7)
- No residual imaging (image lag)
- No microphonics
- Single voltage and low power requirements
- Small size
- High resistance to image burn-in
- High uniformity
- No residual bias (fat zero) required

TIC-5: A TV Compatible CCD Camera

The TV compatible camera, which is called TIC-5, is shown in Figure 1. As shown, the camera can quickly be adapted for use in either of two configurations. Figure 1a shows the camera as it is used for standard TV applications; Figure 1b shows the camera configured with a remote sensor head for applications requiring an ultra-small sensor.

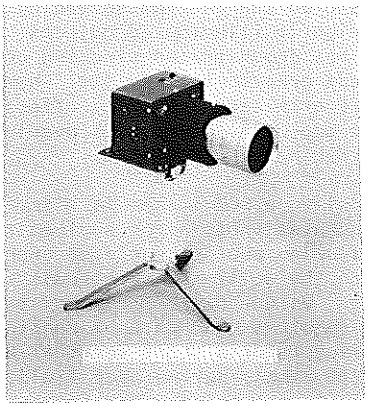


Figure 1a. Standard Configuration TIC-5 Camera

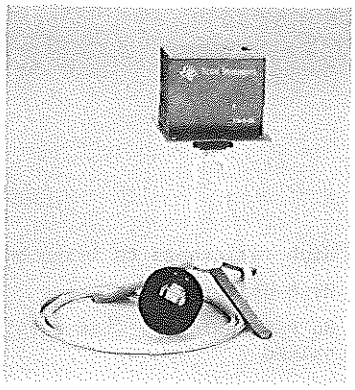


Figure 1b. Remote Head Configuration TIC-5 Camera

General Discussion

The TIC-5 camera utilizes a 327 x 490 (160,230 pixels) CCD as a 327 x 245 imager operating in the frame-store mode to generate standard 525-line TV pictures. The CCD employs two-phase, buried channel, front-side illuminated techniques to achieve very high charge transfer efficiencies. An anti-blooming structure is also included to prevent the stored charge from spreading while viewing brightly illuminated objects. This structure has demonstrated blooming control at overloads greater than 10,000. However, frame-store architecture limits effective control to approximately 1,000X overloads due to streaking.

Basically, a CCD imager is a device which integrates photons for a given time period, allowing photon generated charge to build up in the well, and then reads the charge out. On the other hand the standard TV format requires that data be continuously read out except for a short vertical blanking period (1250 μsec), during each field, when the monitor is retracing. The frame-store mode of operating a CCD is one way to overcome this incompatibility.

In the frame-store mode of operation, the CCD is divided into two equal areas (as shown in Figure 2): one, a 327 x 245 imaging area which is exposed to the incoming photon irradiation, and the other, an identical 327 x 245 memory area which is opaque to the incoming irradiation. During operation the image area integrates photons for one TV field (1/60 second). Then during vertical blanking of the TV monitor, the entire image area is quickly dumped into the memory area. While data for the next field is being collected in the image area, the data from the previous field is read out, line by line, by shifting down into the horizontal serial register and out through an on-chip output amplifier.

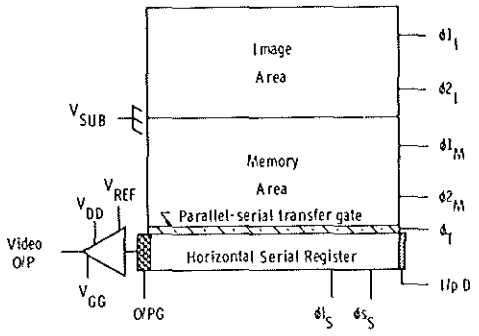


Figure 2. Frame-Store Mode CCD

Parallel Array Description

Both the image area and memory area consist of 80,115 MOS capacitors, each arranged into a matrix of 245 rows and 327 columns. The number of elements required in each area is determined as follows: a TV field consists of 262½ lines (242½ readout lines and 20 retrace lines). Therefore, a minimum of 242 lines are required, and the number 245 was chosen. Since this CCD has square 0.96 mil by 0.96 mil picture elements (pixels), it follows that the number of pixels per line to give a four to three aspect ratio (TV standard) is 327. Each individual pixel has boundaries consisting of built-in barriers in the horizontal direction and gate-controlled channel stops in the vertical direction as seen in Figure 3.

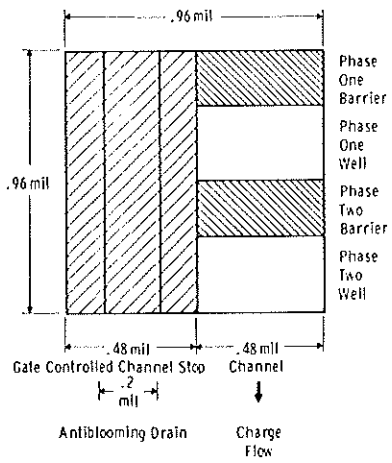


Figure 3. CCD Unit Cell

The method of interlacing used in this camera is accomplished by electronically shifting the centroid of integration for each well by half a cell dimension. This technique provides very little improvement in the vertical modulation transfer function (MTF), but does effectively double the vertical spatial sampling frequency. This tends to reduce the aliasing properties of the camera and improves the useful vertical resolution. Electronically, this method of interlacing is accomplished by biasing parallel phase electrode $\emptyset 1_1$ on during field A and then biasing parallel phase electrode $\emptyset 2_1$ on during field B. However, because in TIC-5 one electrode is polysilicon and the other is aluminum, there is a noticeable difference in the response between the two fields, and therefore the camera is most often operated in the non-interlace mode. By using a polysilicon version of the sensor, this problem is overcome.

Horizontal Serial Register

The horizontal serial register is used to shift the data, one line at a time, out of the CCD. This register sits idle for 10.9 µseconds during each horizontal blanking period while a new line of data is loaded into it and then clocks out serially at a 6.2 MHz data rate in order to be TV compatible. The data rate is determined as follows: a TV line readout is 63.5 µsec with a 10.9 µsec horizontal blanking period. Therefore the actual clocking time is:

$$t_{clocking} = 63.5\ \mu sec - 10.9\ \mu sec = 52.6\ \mu sec$$

and the time to read one pixel is:

$$t_{pix} = \frac{52.6\ \mu sec/line}{327\ pixels/line} = 0.1609\ \mu sec$$

The serial data rate then is:

$$f_{data\ rate} = \frac{1}{t_{pix}} = \frac{1}{0.1609 \mu sec} = 6.2\ MHz$$

Timing Diagram

A timing diagram for the TIC-5 camera is shown in Figure 4. As shown, both the imager and memory clocks, $\emptyset 1_1$, $\emptyset 2_1$, $\emptyset 1_M$, and $\emptyset 2_M$, are clocked together, during vertical blanking (dump), for 245 times in order to load a new frame of data into memory. Then one of the image area clocks ($\emptyset 1_1$ shown) is biased on to allow charge to accumulate during the integration period. The data stored in the memory section is read out by clocking the memory area clock $\emptyset 1_M$ and $\emptyset 2_M$, one cycle during each horizontal blanking period to reload the serial register. Then the serial register simply clocks 327 cycles to read the data out.

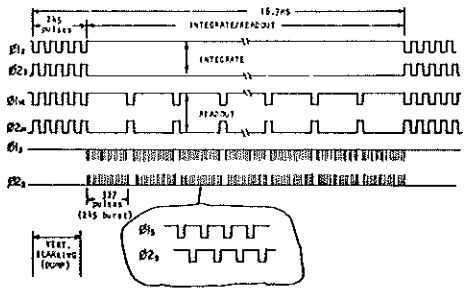


Figure 4. TIC-5 Camera Timing Diagram

An on-chip pre-charge, double-source follower amplifier is used to provide the

voltage waveform that is transmitted to the video processor circuitry. A diagram for this amplifier is shown in Figure 5. It functions as a resettable electrometer for detecting extremely small quantities of charge (down to fractions of femtocoulombs). The circuit consists of five MOSFETs, one (Q1) of which precharges the output diode of the CCD to a fixed reference voltage, V_{REF}, prior to the arrival of each charge packet. Two MOSFETs (Q2 and Q4) are used as source followers: the first to maximize the detection of charge, and the second to minimize output load impedances. MOSFETs Q3 and Q5 are on-chip loads for the corresponding source-followers.

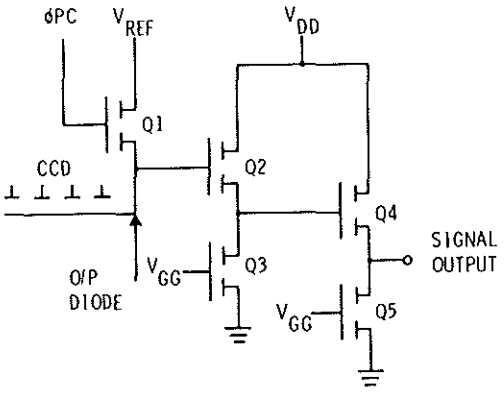


Figure 5. CCD On-Chip Precharge Amplifier

Video Processor

Within the video processor circuitry, the data are sampled and held at a time corresponding to approximately the center of the data well as shown in Figure 6. This sampled and held video output is stripped of the precharge pedestal and contains only desirable data.

Also, television sync signals are superimposed onto the sample and hold video to provide composite video, in accordance with the timing and synchronization portions of EIA RS-170 specifications, capable of operating into any standard TV monitor or commercial video tape recorder.

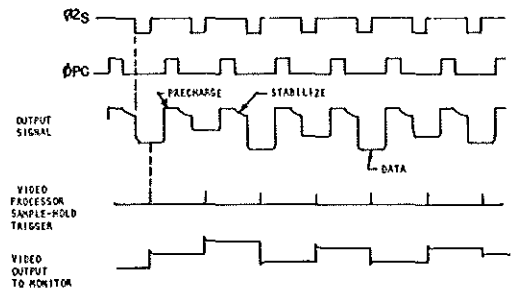


Figure 6
TIC-5 Output Sampling and Timing Diagram

Physical Parameters

The TIC-5 camera is small; for example, in the remote sensor head configuration the main camera body occupies 10.5 in^3, and the sensor head occupies only 1.6 in^3. Although the camera is very small, it is constructed using basically standard discrete components. The rather dense packaging is largely attributable to using flat-pack integrated circuits and a technique known as hot-electrode welding. As shown in Figure 7, this is a method of interconnecting electronic circuitry by point-to-point wiring. As shown, on the back side of the printed circuit board, nickel wire with polyurethane insulation is welded to pure nickel pins in a point-to-point fashion. One of the welder electrodes heats up and melts the polyurethane insulation away just prior to making the spot weld. The flat-pack integrated circuits are then soldered to the front side of the board.

The TIC-5 camera dissipates three watts of power and requires only a single +12V DC voltage input. Drawing only 250 mA of current, the camera can be operated from a relatively small battery pack for up to two hours per charge.

Typical imaging pictures taken from the operating camera are shown in Figure 8. The black vertical line near the lower left corner of the image is caused by a blocked channel in the CCD parallel array.

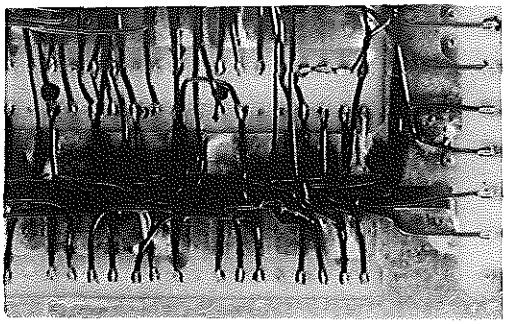
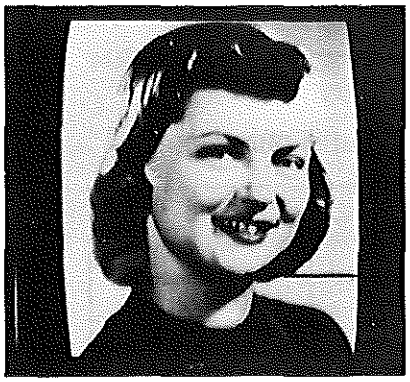


Figure 7
Hot Electrode Welding Packaging Technique



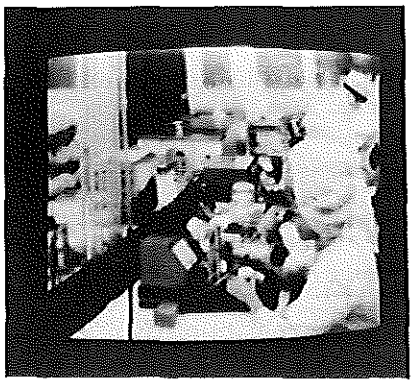


Figure 8
TIC-5 Typical Imaging Pictures

The camera specifications are listed below:

Electrical Parameters

Typical operating voltage	+12 ± 1V
Typical operating power	3 watts
Data rate	6.2 MHz
Horizontal video bandwidth	3.1 MHz
Integration time	16.7 ms
Output voltage - composite	1.0 V

Optical Parameters
(327 x 490 CCD)

Image cell size		0.96 mils x 0.96 mils
Aspect ratio		4 x 3
Image area size		0.314 in x 0.235 in
Spectral response		0.40 μm to 1.1 μm
Blooming control above saturation		>1000 times saturation level-test device
Charge transfer efficiency, CTE		>0.9999
Resolution:	Vertical	∿ 170 TVL/ph
	Horizontal	∿ 250 TVL/ph
Dynamic range		60

TIC-7: A Time-Delay-Integration Scanning Camera

Although the TIC-7 camera, shown in Figure 9, is primarily a time-delay-integration scanning camera, it can be operated in a secondary mode as a full-frame imager. The sensor for this camera is a 48 x 24 (1152 pixels) two-phase, frontside illuminated CCD. This device is similar to the 327 x 490 CCD discussed earlier except for its smaller size and the fact that no anti-blooming structure is included. Figure 10 illustrates the operation of a CCD in both the full-frame and time-delay-integration modes. When operating in the full-frame or stare mode, the imager sits idle for an integration period and then is clocked out

by shifting data down, one line at a time, into the serial register where it is then read out serially through an on-chip amplifier. In the primary time-delay-integration or scan mode, the imager is continuously read out in full-frame fashion as though the integration time is zero. However, the entire imager is scanned across the scene at the exact same rate at which the CCD is clocked out so that a pixel in the CCD field locks onto and tracks a point in the scene, until read out, to provide an effective integration period.

Camera Operation

The TIC-7 camera is designed to operate with a variable frequency with a master clock ranging from 384 kHz to 2.35 MHz. Table 1 shows the integration time range and required illumination level range for both the scanning and starring modes.

Mode	Master Clock	Integration Time	Minimum Illum. Level (2854°K Source)
Scan	384 kHz	6 msec	2.5 $\mu w/cm^2$
Scan	2.35 MHz	1 msec	15 $\mu w/cm^2$
Stare	384 kHz	31 msec	0.5 $\mu w/cm^2$
Stare	2.35 MHz	5.9 msec	2.5 $\mu w/cm^2$

A flow diagram illustrating the sequential operation of the camera is shown in Figure 11. In this diagram, X represents the number of counts in the pix/line counter, and Y represents the number of counts in the line counter. The X counter is 8 bits and therefore has a capacity of 256 counts while the Y counter is 5 bits and has a capacity of 32 counts. Initially, the X and Y counters are set to 208 and 8 counts, respectively. This represents the 48 pixels per line (256 - 208 = 48) and 24 lines (32 - 8 = 24) which ocrresponds to the TIC-7 sensor. In the scan mode only the pix/line counter loop is required. The circuit cycles around this loop, making a serial shift for each loop, 48 times until the serial register is read out. Then a parallel shift is made, loading a new line of data into the serial register. X and Y are reloaded and the cycle is repeated.

In the stare mode, the line counter loop is added so that after each line has been read out the line counter is increased by one count. After this counter indicates that one frame (24 lines) of data has been read out, the camera then enters the integration state. Here, additional loops are added to form an integration timer used to time out the integration period during which time the CCD sits idle. At the end of the integration period, the circuitry is reset, and the entire cycle repeated.

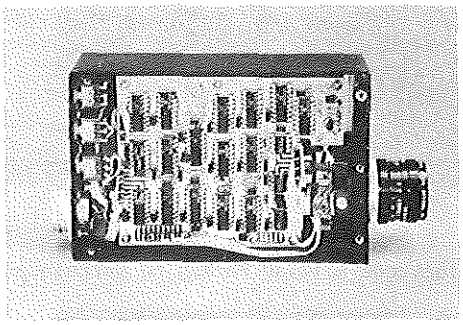


Figure 9. TIC-7 Camera

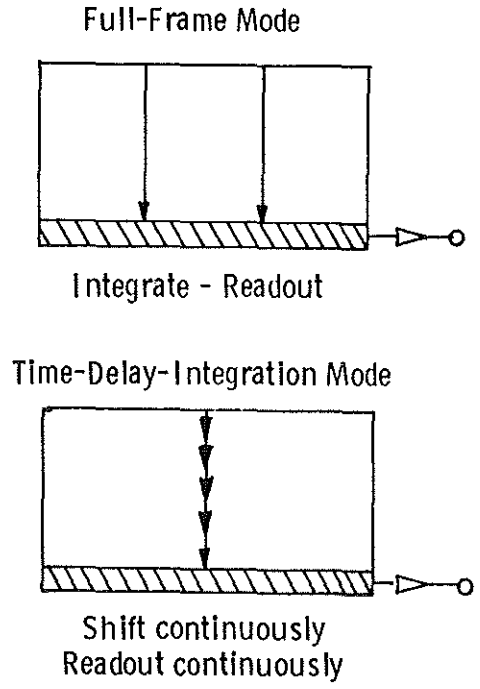


Figure 10. TIC-7 Modes of Operation

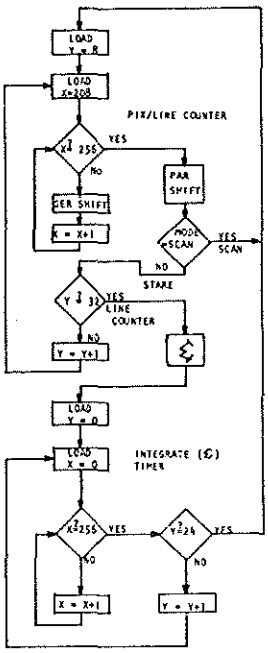


Figure 11. TIC-7 Flow Diagram

Figures 12 and 13 show an imaging picture and a uniform illumination picture, respectively, for the operating camera.

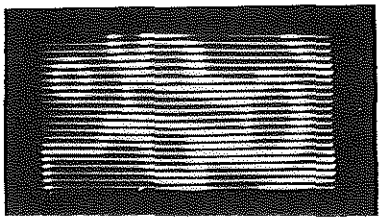


Figure 12. TIC-7 Imaging Picture

Physical Parameters

The TIC-7 camera measures 2"W x 4"H x 6"L and has a volume of 48 in^3. Although the camera is somewhat larger, it is built

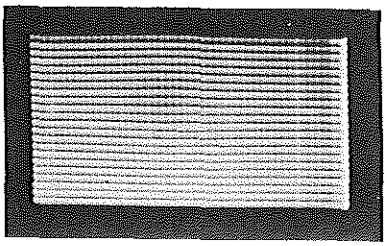


Figure 13
TIC-7 Signature-Uniform Illumination

in a modular fashion so that individual circuit cards can be quickly removed for repair and/or testing. The construction uses dual-in-line (DIP) packages interconnected using the hot-electrode welding technique discussed earlier. The TIC-7 camera, which includes an automatic gain control in its video circuitry, dissipates 4.3 watts of power and also requires only a single +12V DC voltage input.

A picture of the 48 x 24 CCD sensor is shown in Figure 14.

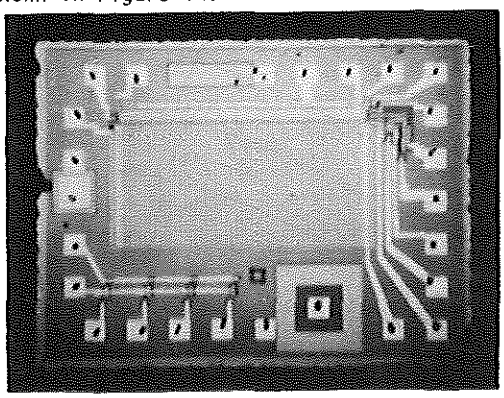


Figure 14. 48 x 24 CCD

Optical specifications for the TIC-7 camera are shown below:

Optical Parameters (48 x 24 CCD)	
Image cell size	0.96 mil x 0.96
Aspect ratio	2 x 1

Optical Parameters (con't)

Image area size	0.046 inch x 0.023
Spectral response	0.4 μm to 1.1 μm
Dynamic range	300
Modulation transfer function (MTF)	∿30% at Nyquist limit

Spectral Response

Finally, the spectral response is shown in Figure 15 for typical CCDs with a built-in antiblooming structure. The three curves shown represent polysilicon-aluminum electrodes, polysilicon-polysilicon electrodes, and thinned backside illuminated devices, respectively.

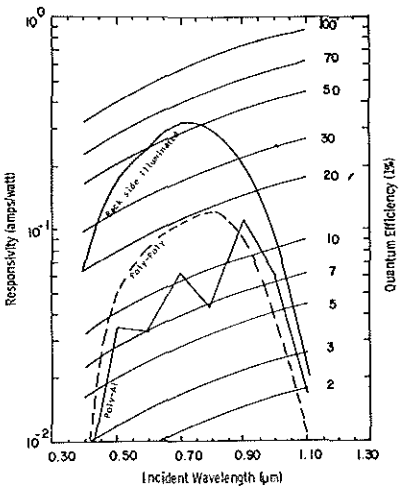


Figure 15. CCD Spectral Response

Summary

The two CCD cameras discussed here are representative of those which have been developed at TI. Although these cameras are only prototypes, built mostly from standard components, they demonstrate what is ahead on the CCD camera horizon. As large CCDs become available in quantity, very small and stable high resolution TV cameras will become more and more available. Special purpose cameras for military, commercial, and industrial applications built from modular units will lead this development. The variety of TI's prototype cameras will form the basis for such future CCD cameras.

Acknowledgements

The authors wish to thank Ms. M. Agnew, D. Awtrey, T. Dunavan, and T. Mercer for their contributions to camera development and fabrication. They also acknowledge W. Chan, R. Little, and R. Shields for their assistance in sensor design and testing, as well as Dr. D. R. Collins for his valuable assistance in editing this article. M. Tirone's assistance in editing and typing this manuscript is gratefully acknowledged.