A HIGH RESOLUTION BUTTABLE TIME DELAY AND INTEGRATE IMAGING CCD

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ABSTRACT. The design and fabrication of a CCD buttable 256 x 96 element TDI chip was undertaken by BNR and ITEK; as a vehicle to prove the development of a 2048 x 96 element buttable TDI. In both of these designs the time delay operation is in the 96 elements Y direction. The TDI imager was fabricated using BNR's two-level polysilicon buried channel CCD process. High resolution of 13 μm in the X and Y direction was achieved through the use of ripple clocking and a novel interlaced readout scheme. The TDI is also buttable with only 2 sensor elements gap between adjacent devices. The device offers some blooming control capability by electronic selection of 1, 8, or 96 rows of element. Device characterization results will be presented together with sample imagery taken with the imaging chip.

1.0 INTRODUCTION

Developments in reconnaissance area imaging systems over the last few years have emphasized the use of solid state imaging arrays. CCDs are natural candidates for this role. Various analysis have scoped the requirements for such CCD arrays (2,3).

Itek Corp., Lexington, Mass., U.S.A., and Bell-Northern Research Ltd., Ottawa, Ontario, Canada have been working since 1976 on the development of a family of CCD imaging devices intended for application in military reconnaissance systems (1). The purpose of this paper is to describe the design, operation and performance of the first TDI of this family. The TDI, designated Itek/BNR 719A, was designed to be buttable with less than two pixel spacings between chips. The resolution in both X and Y direction was 13 μm. The high resolution was achieved by using some novel design approaches. Test results reflect the high performance of these devices in the area of noise and dynamic range which are needed for military applications. This paper will describe the architecture and fabrication of the chip, and present test results including imagery of simulated moving scenery. Finally, we will briefly discuss the application of the chip to military reconnaissance systems.

2.0 DEVICE ARCHITECTURE AND FABRICATION

A block diagram of the buttable 719A TDI is shown in Fig. 1. The imaging area, parallel to serial interface, and serial shift register are the main functional blocks of the TDI. There are 3 basic operations in a TDI imager:

(i) The electronic imager formed on the TDI imaging areas is clocked from one row of sensors to adjacent row of sensors in synchronism with the optical image motion.

(ii) When a line of the electron image reaches the bottom row of sensors of the TDI, it is transferred into the serial shift register via the parallel to serial interface.

(iii) The data transferred into the serial shift register is read out serially by the output circuit located at the end of the shift register.

The option middle output tap is a destructive output which doubles both the TDI line rate and output data rate without increasing the serial shift register

clock frequency. When not required, it can be disabled by a transfer gate and all charge packets are transferred to the end output circuit. Electrical inputs are provided for the TDI array and serial shift register for convenience of testing and characterization.

The high resolution of the 719A in both X and Y directions is the result of the following two novel design approaches.

(i) Odd-even channel interlaced transfer into the serial shift register.
(ii) A 8-phase ripple clock scheme for the TDI array.

A detailed description of these two techniques will follow:

(i) In the X direction, the resolution of a conventional TDI is limited by the stage length ΔX of the serial shift register (see Figure 2). A novel way out of this limitation is to perform the charge transfer operation from the TDI to the serial shift register in two stages. This odd-even channel interlaced readout scheme runs as follows. In the first stage of the readout, charge from the odd channels is transferred to the serial shift register, and charge from the even channels is stored in a buffer register. Then data in the shift register is read out serially. In the second stage of the readout operation, charge from the even channel is transferred and clocked out. This is formally equivalent to multiplexing the serial shift register. Figure 3 shows that the CCD channels within the TDI array can be spaced to half the stage length of the CCD shift register, or $\Delta X/2$ (13 μm). Thus, at the expense of a slightly more complicated readout scheme, the resolution in the X direction is doubled.

(ii) In the Y direction, the normal 2 phase (or 3 phase or 4 phase) CCD structure is replaced with an 8-phase ripple clocking structure. The advantage of an n-phase ripple clocking system is that charge can be stored in n-1 consecutive pairs of CCD electrodes. Only 1-phase need to be reserved for charge transfer purposes. Figure 4 shows the clocking waveform for an eight phase ripple clock scheme. The resolution of a ripple clock TDI is not limited by the stage length $2\Delta Y$ (2 pairs of electrodes) of the CCD. Instead, it is exactly the same as the length of one pair of CCD electrodes, or ΔY. Actually, there is a certain amount of charge sharing involved during the charge transfer operation, which causes MTF degradation. The Y axis MTF degradation in a ripple clock TDI is given by:

$$(MTF)Y = \frac{\mathrm{Sin}\ \frac{n}{n-1}\ \P f \Delta Y}{\frac{n}{n-1}\ \P f \Delta Y}$$

where ΔY = stage length of CCD (2 pairs of electrodes)

f = spatial frequency in cycles/mm

n = # of ripple clocking phases

It can be seen that in order for the ripple clock to be effective (i.e., without suffering crippling MTF loss), it has to be significantly larger than 2.

The total MTF loss due to finite aperture size, discrete charge motion and charge sharing is then:

$$(MTF)Y = \underbrace{\frac{\mathrm{Sin}(\P \Delta y f)}{(\P \Delta y f)}}_{\text{aperature MTF}} \underbrace{\frac{\mathrm{Sin}\ \frac{n}{n-1}\ \Delta f \P y}{\frac{n}{n-1}\ \P f \Delta y}}_{\text{Ripple Clocking MTF}}$$

In a buttable TDI, the ripple clocking of the 96 pairs of electrodes poses some formidable problems. There are 3 basic system constraints:

(a) Since it was decided to adopt 8 phase ripple clocking, the 96 electrodes have to be connected in 12 blocks of 8 pairs of electrodes each.
(b) The buttability requirement precludes running the clock lines alongside the circuit and connected to the different set of electrodes in a matrix fashion.
(c) It was decided to make provisions allowing the selection of all 96 rows of sensors, the first eight rows of sensors or the first row of sensors only.

These 3 requirements are met by partitioning the imaging part of the B^2TDI into 8 segments (see Fig. 3) in the X direction. The use of two level metallization allows the implementation of these features.

The dimensional requirement for buttability was that the separation between two dies would be only 2 equivalent pixels as shown in Fig. 4. The edges were prepared by a chemical etching technique developed at BNR. Fig. 14 shows a picture of the prepared edges of the buttable 719A TDI.

In operation the photo-generated charge in the pixels is moved in the Y direction of the TDI by an 8-phase ripple clock scheme (Fig. 5) which is in synchronizism with the imagery scene motion. Once the charge reaches the bottom of the TDI, it is transferred in the serial shift register via the parallel to serial interface.

The clock timing for both interface scheme and shift register is shown in Fig. 6.

The output sensing circuitry of the serial shift register is shown in Fig. 8. It consists of a presettable floating diffusion connected to an on chip pre-amplifier (depletion type MOST source follower). The photocharge is sensed as a voltage change at the output of the source follower.

The imagers were fabricated using BNR's two levels polysilicon gate buried channel technology. The process allows the on-chip incorporation of enhancement and depletion (ion implanted) MOST structurers. This attractive feature contributed to the low noise performance of the output pre-amplifier. The process uses three ion implants steps plus n+ diffusion for source and drain. It also features isoplanar oxide isolation and two levels of aluminum interconnects.

3.0 TEST PROCEDURE AND EXPERIMENTAL RESULTS

3.1 General Information

The devices were evaluated on two levels; normal device characterization tests such as transfer efficiency, spectral response, pre-amplifier gain and noise measurements performed at BNR, and extensive testing at Itek to characterize the device as an image transducer in a situation comparable to a high quality reconnaissance system application.

3.2 Examination and Imaging Testing of the Itek/BNR 719 CCD Chip

High quality airborne military electronic reconnaissance camera systems are rather complicated, with the data stream from the CCD or other solid state array typically undergoing sophisticated signal processing in the aircraft, digital transmission or recording, and digital data processing on the ground before display. In order to fairly characterize a CCD array for this application, we must duplicate most of these functions with test gear such that the final displayed output is limited in its quality by the device under test, rather than be the test equipment. In the case of imaging CCD's, this is a difficult problem due to the low noise and high dynamic range of the Itek/BNR 719 chips.

Figure 9 is a block diagram of the Electro-Optical Imaging Laboratory used at Itek for the characterization testing of the Itek/BNR 719 CCD. It shows the image producing process from the input scene to the final output, which may be a hard-copy print of the image seen by the CCD or a computer printout representing the analysis of some properties of the image. At the left side, we show the various input possibilities for a CCD under test. We may choose among real scenes, model scenes, photographic reproductions of real scenes, or standard test charts. Most of the routine characterization testing that we perform is done using moving belts of film with reproductions of aerial photography and test charts. This test input is imaged on the TDI chip by a lens whose imaging performance is known. The image transducer in our situation is a CCD under test with its operating electronics. In order to simulate high quality data recording, we use a Data General Eclipse S-230 mini-computer with a customized set of peripheral equipment. The pixel stream from the CCD is digitized by a high quality A/D converter capable of 10^7 conversions per second with 13 bit resolution and fed into a

semiconductor memory which can store up to 10^7 bits. This is sufficient to reproduce frames of imagery large enough for display and characterization. The S-230 can then retrieve the data from the semiconductor memory, perform manipulations of the data, and write it onto tape for more detailed analysis in the Itek IBM 370-158 computer, which is a general purpose off-line machine. That computer can perform data manipulations of several types. It can perform image enhancement (such as calibrating out the element-to-element variations that exist in virtually all arrays) for the purpose of presenting hard-copy image display. It can perform a number of statistical analysis of the imagery such as signal-to-noise ratio calculations. It can also alter the recorded data to simulate the effect of other system components so that complete systems may be simulated for system design purposes. Finally, we have available as output peripherals, a choice among a laser writer (for hard-copy imagery), a line printer for tabular data, a plotter for graphical data, or a tape deck for tapes to be stored or transmitted to other organizations.

3.3 Test Results

The best demonstration of an imaging CCD is imagery produced by it. Fig. 10 shows two examples of imagery from the Itek/BNR 719 chip, recorded in the Itek EO Imaging Laboratory just discussed and printed out on the Laser Scanner. The images are of the USAF 1951 Resolving Power Test Target and the Itek 1975 MTF Test Target. The test conditions for these images are as follows:

Line rate	4 KHz
Pixel rate	1 MHz
Readout	End Tap
Exposure	50,000 e^-/pixel
	4,800 K Blackbody
Temperature	35°C

The imagery was reconstructed by properly interlacing the pixels with a software operation in the data gathering process.

For the MTF Test Target, the optical magnification was 0.1, so 40 lp/mm, the nominal Nyquist limit, is the 0 element of the 2 group. In a), the right portion of the printout is a 2X blowup of the last five groups in the left portion. In both cases, the Nyquist limit is resolved, and the uniformity and high quality of the imagery may be seen.

A summary of the measured properties of a typical sample is given in Table I. It is shown that an excellent imaging performance with high sensitivity and low noise was obtained. The dynamic range at 4 KHz line rate and 1 MHz pixel rate is 5,000, with the saturation level being limited by the small pixel size to about 125,000 e^-/pixel as an image sensor.

The MTF data are shown in details in Figure 11. Three curves shown in order to indicate the separate effects of CCD design and the charge diffusion in operation. Curve one is the calculated geometric MTF of the finite cell area and the motion error caused by continuous scene motion and discrete charge motion. For the eight phase ripple clock scheme used, that MTF component (for "short pulse clocking; that is, the phase clock pulses are shorter than the phase duration") is

$$MTF = \frac{\mathrm{Sin}(\P f \Delta y)}{\P f \Delta y} \qquad \frac{\mathrm{Sin}\,\frac{n}{n-1}\,\P f \Delta y}{\frac{n}{n-1}\,\P f \Delta y}$$

where n = 8 for the Itek/BNR 719 chip.

Curve 2 is a measured MTF with an incandescent source filter to remove light beyond 0.75 μm. Curve three is a measured MTF taken with light having approximately a 4800K blackbody spectrum. The previously discussed (4) effect of deep absorption of red and near infrared light and subsequent diffusion of charge to nearby pixels is evident. The effect was accentuated here, because the chip measured response peak at about 0.9 μm. This effect is a significant limiting factor to the performance of small CCDs in cases where both sensitivity and resolution are desired (3).

Signal and noise transfer are shown in Figure 12, as a function of exposure.

At a pixel rate of 5×10^6 per second, the dynamic range is from 0.4×10^{-6} j/m^2 to 0.9×10^{-3} j/m^2. Since the noise is predominantly flat, the extrapolated noise level with 10^6 pixels per second and a 2 MHz filter is 0.18×10^{-6} j/m^2.

Spectral response of this chip is shown in Figure 13. It shows the expected general form, with light at wavelengths less than about 0.5 μm absorbed in the overlying layers of polysilicon and also due to light at wavelengths longer than about 1.1 μm passing through the active region without being absorbed. The peak at 0.9 μm is a combination of high quantum continuation (photons per joule) at longer wavelengths and an optical feature. The peak quantum efficiency is 55%. The measurements were made with a monochrometer having $\Delta\lambda$ = 0.05 μm, and power measurement was made by substituting a radiometer in the CCD image plane.

3.4 Testing of Buttable (Edge Etched) CCD

In this section the operation of the Itek/BNR 719 chip is demonstrated. Figure 14 is a set of photomicrographs of the etched edges of a chip. By measurement, it may be seen that the two chips may be placed such that the center to center spacing of the two extreme TDI columns would be 37 μm. Since the goal was to have two chips buttable with two missing columns of data, the goal is satisfied if the extreme columns can be placed with a center-center spacing. Other work (4) has demonstrated the ability to place the CCD chips on a common substrate and register them to within about 5 μm of specified locations.

Figure 15 is a reproduced image of the USAF 1951 Resolving Power Test Target taken with the same chip appearing in Figure 14. In this picture, the display shows the pixels in the order they are read out of the chip, with the left half of the picture containing the even numbered pixels and the right half the odd numbered pixels. Since the optical magnification was 0.1, the Nyquist limit in the direction occurs at the 0 element of group 2. Because of the pixel interlace the Nyquist limit in the orthogonal direction is the 0 element of the 1 group.

As may be seen by examining the photo, the edge etching process has not introduced any artifacts into the imagery. The edge columns do not exhibit dark current or sensitivity noticeably different from the neighboring elements. The goal of a gap of two pixels was set based of a simulation using samples imagery. The imagery was processed to simulate a typical system MTF at the Nyquist limit. Gaps in the sensing array were then simulated by eliminating columns of video and replacing the pixel values with linear interpolations of the video on the closest remaining pixels. Gaps of from 1 to 10 pixels were simulated in this manner. A typical picture containing fairly busy imagery on which this procedure has been carried out is shown in Figure 16. Most observers can find the 10 pixel gap and the 5 pixel gap, but cannot find the 1 or two pixel gaps until they have found the wider ones for reference. (The gaps extend the vertical length of the pictures and all begin with the same horizontal pixel).

3.5 Demonstration of Operation of Intermediate Tap

One of the design features which is critical for successful operation at very high line rates is the tap at the 128th element. Operation of this tap is shown in Figure 17. There, a) shows the entire pixels read through the end tap with the center tap bypassed. In b) the output from the end tap is shown on the transfer gate adjusted at an intermediate value to demonstrate the partial extraction of signal charge by the middle tap. In c) and d), the outputs from the two taps are shown separately, having been recorded under identical conditions. There is no visible leak-through of data from the left half of the chip when the center tap operating voltages are set correctly.

The operating speed for these pictures was 20,000 lines per second. Operation up to 40,000 lines per second has been demonstrated.

The significance of successful tap operation becomes evident when considering the design of chips with 2,000 TDI columns to operate at 50,000 or more lines per second. This would require an output tap to operate at 100,000,000 pixels per second, unless intermediate taps are used. Such high operating rates, present problems in chip design, data handling design, and high output preamplifier noise due to the high bandwidth.

4.0 SUMMARY

To summarize, a prototype buttable TDI imaging chip was developed characterized and tested in a system context by BNR and Itek. The chip is capable of high dynamic range and low noise operation. It is buttable with less than two pixels spacing between chips. A middle output tap is provided for increased line rate readout. The chip has been tested thoroughly with sophisticated optical data processing set up and is shown to be useful for aerial reconnaisance application. A further 2048 x 96 TDI chip having the same features is being fabricated.

ACKNOWLEDGEMENT

The authors would like to thank W.G. Gilmour and J. Saeki for their contribution.

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(2) Wright, R.H., "Low Contrast Imaging", Vol. 301 Proceedings of SPIE (Airborne Reconnaissance), Washington, D.C., 1977.

(3) Bradley, W., "Small Geometry Charge Coupled Devices for Aerial Imagery", Vol. 137, Proceedings of SPIE, Washington, D.C., 1978.

(4) Goldfarb, S., and Coluin, D., "Precise Mounting of Semiconductor Chips for Electro-optical Arrays", Proceedings for ISHM78.

TABLE I: SUMMARY - PROPERTIES OF ITEK/BNR 719 CCD

Array Size	256 pixels x 96
Operation	TDI (96 element direction)
Spacing (ripple clocking) (2 Ø clocking)	13 μm x 12 μm 26 μm x 24 μm
Buttable	2 pixel gap
Tap (use optional)	128th element
Sensitivity	0.15 a/w
MTF (40 lp/mm; TDI direction)	0.2
Saturation Level	
Signal Exposure (5500K Blackbody)	125,000 e^-/pixel 0.9×10^{-3} j/m^2
Noise Level (dark) $\sim 5 \times 10^5$ pixels/sec	
Signal Equivalent Exposure	70 e^-/pixel rms 0.4×10^{-6} j/m^2
Noise Level (dark) $\sim 1 \times 10^6$ pixels/sec	
Signal Equivalent Exposure	30 e^-/pixel rms 0.18×10^{-6} j/m^2
Dark Current (20°C)	2 na/cm^2
Uniformity	
Sensitivity Dark Current	~1% p-p <1% of saturation

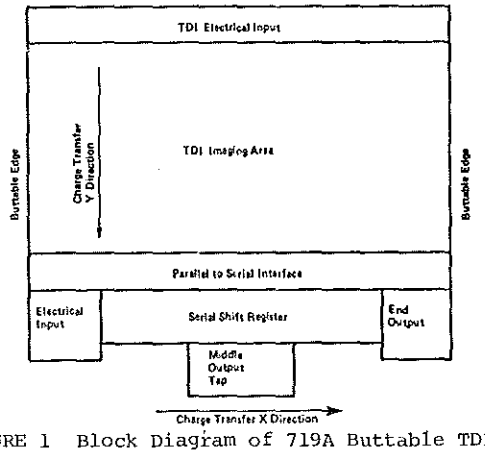


FIGURE 1 Block Diagram of 719A Buttable TDI

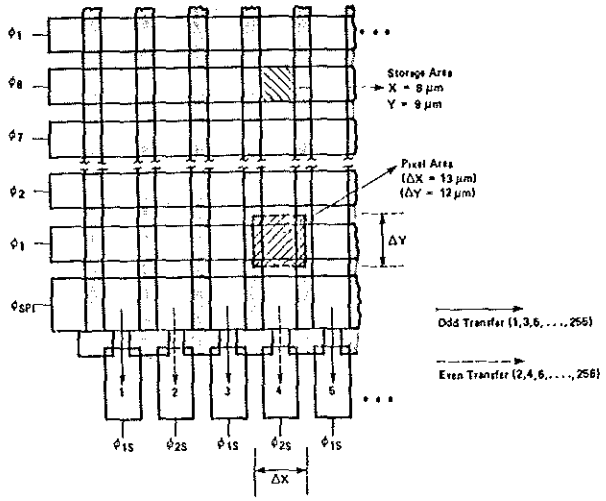


FIGURE 2 719A TDI High Resolution Cell Design

First Aluminum Level Lines

Second Aluminum Level Lines

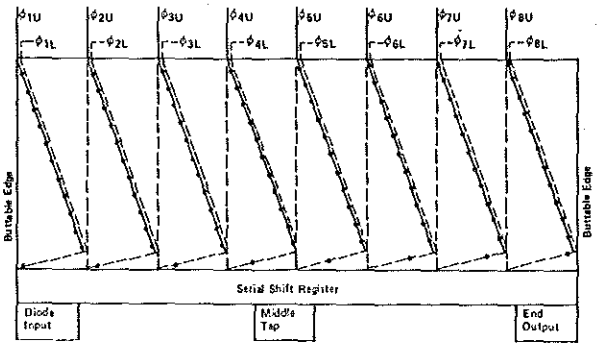
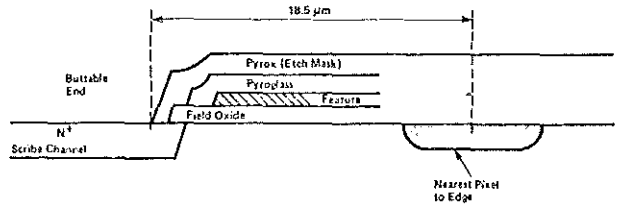


FIGURE 3 Electrode Contact Scheme on Buttable TDI



Scribe Channel Convention

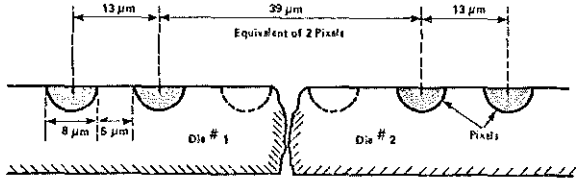


FIGURE 4 Butting Requirements of 719A TDI

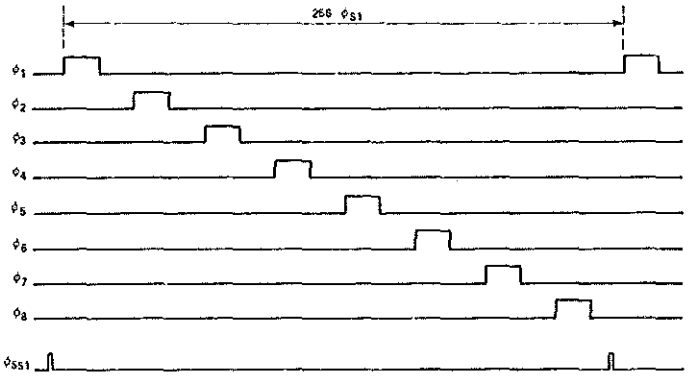


FIGURE 5 TDI 8-Phase Ripple Clocks

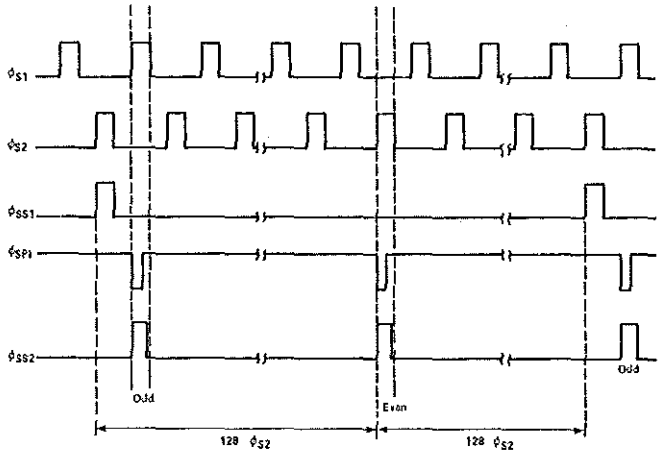


FIGURE 6 Serial Shift Register and Interface Electrodes Clocking

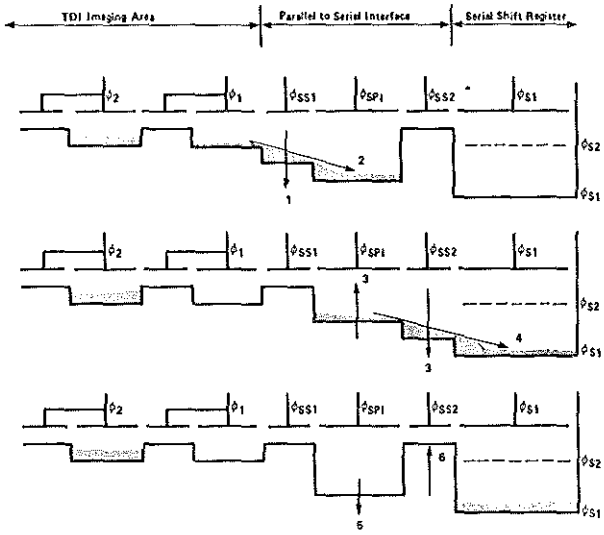


FIGURE 7 TDI Parallel to Serial Interface Operation (Odd Field)

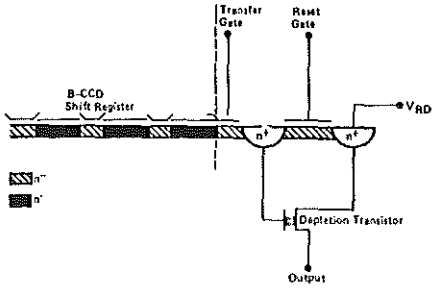


FIGURE 8 Output Charge Sensing Circuit

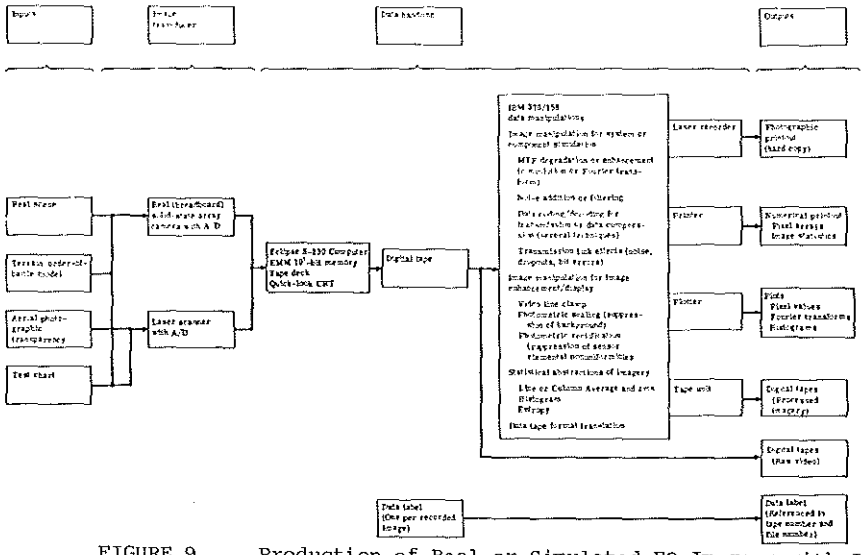
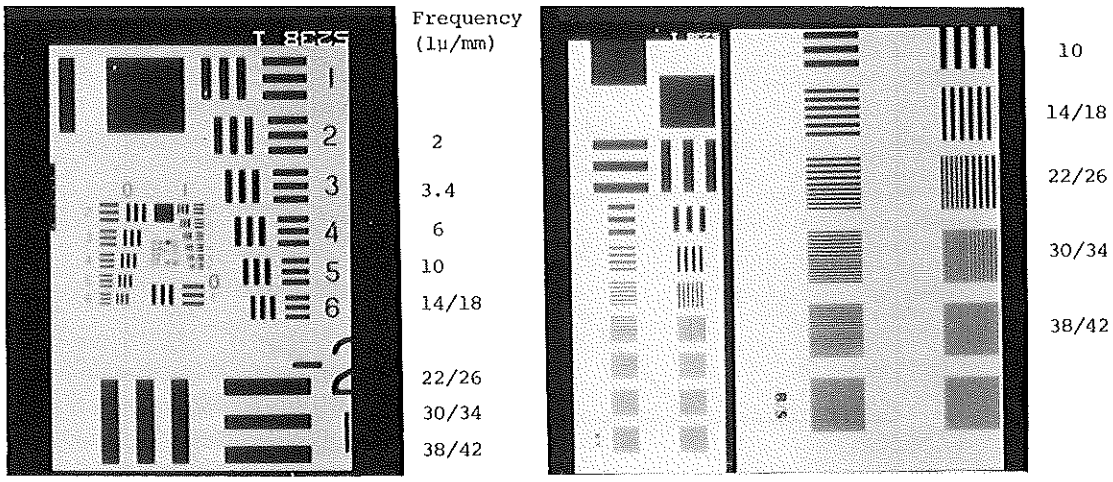


FIGURE 9 Production of Real or Simulated EO Imagery with Itek Electro-Optical Imaging Laboratory (block diagram)



a) USAF 1951 Resolving Power Test Target b) Itek 1975 MTF Test Target

FIGURE 10 Samples of Imagery from an Itek / BNR 719 CCD Chip

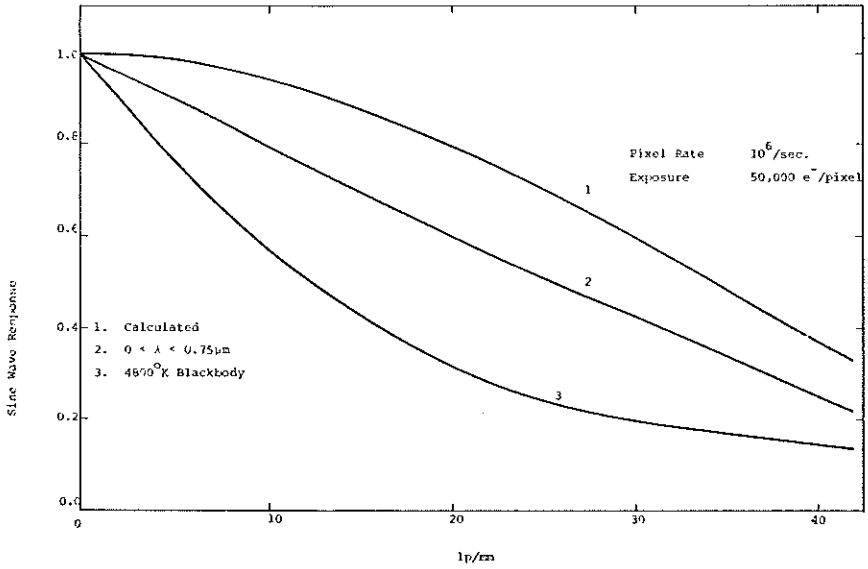


FIGURE 11 Modulation Transfer Function

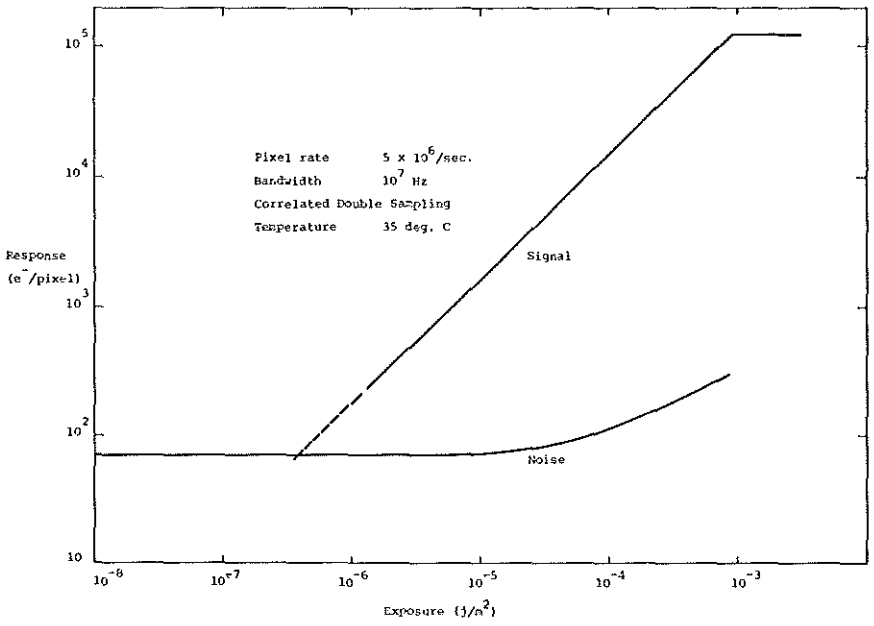


FIGURE 12 Signal and Noise vs. Exposure

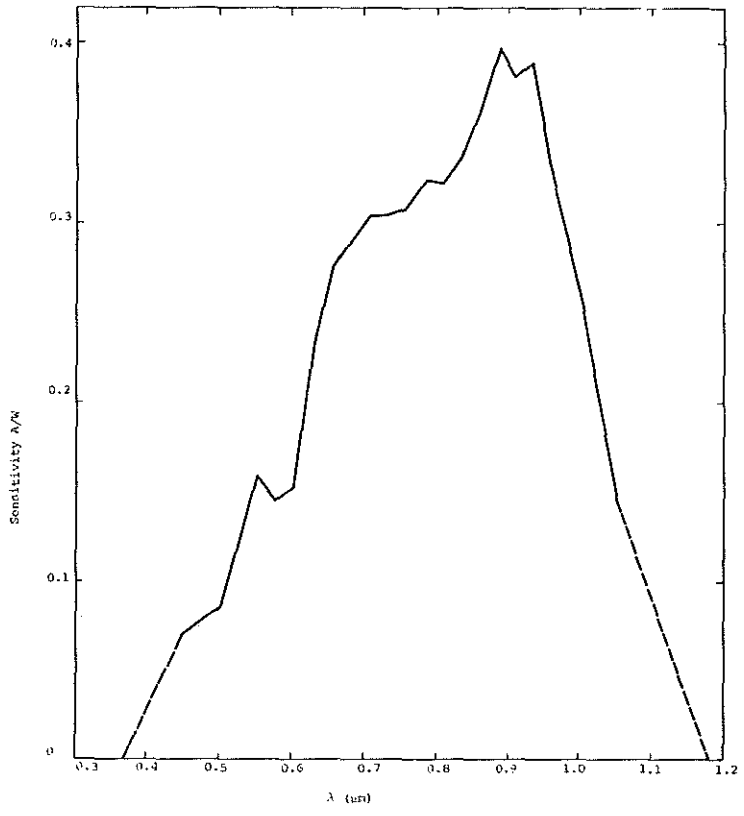
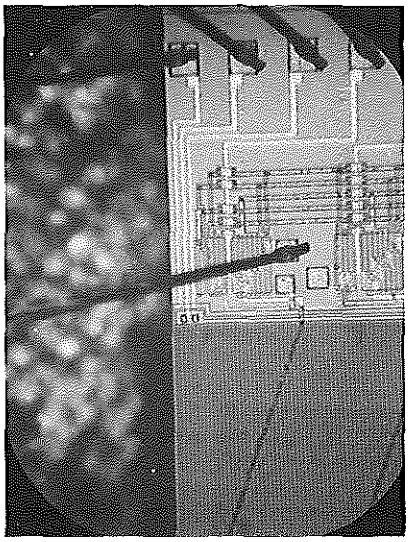
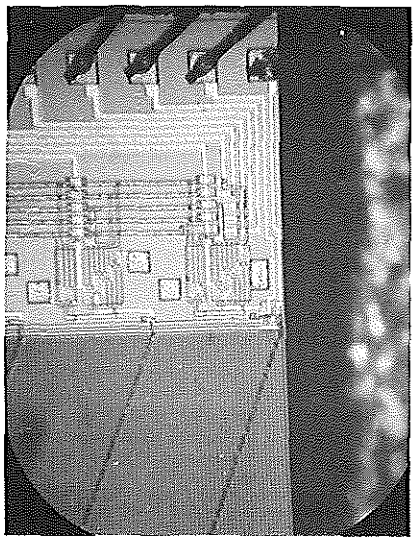


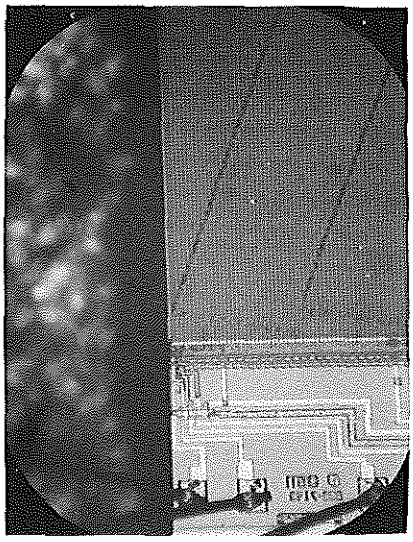
FIGURE 13 Spectral Response



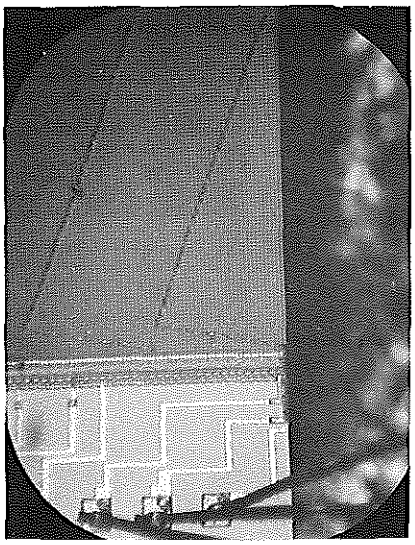
a) Top Left



b) Top Right



c) Bottom Left



d) Bottom Right

FIGURE 14 Photomicrographs of 719 CCD Buttable with 2 Pixel Gap

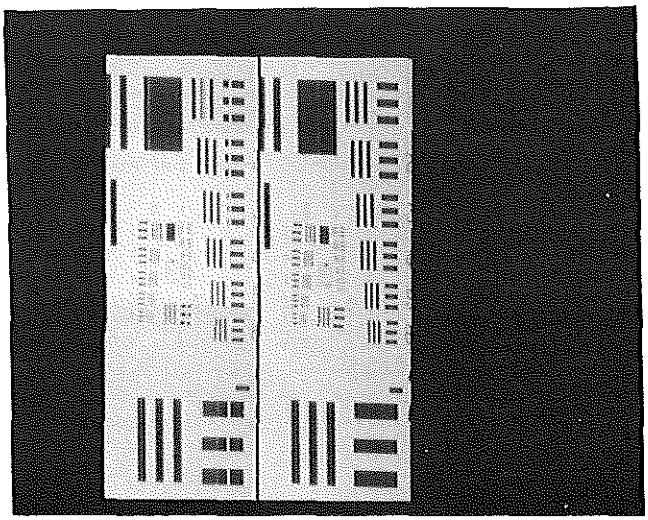
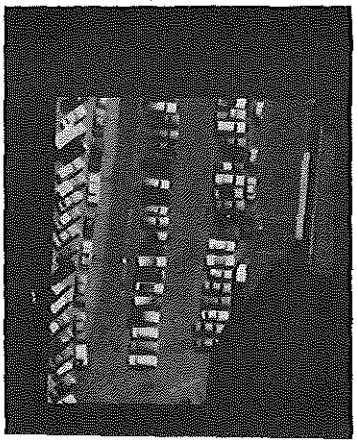


FIGURE 15 Imagery Recorded with Buttable Edge Etched 719 CCD

a) One Pixel Gap

b) Two Pixel Gap

c) Five Pixel Gap



d) Ten Pixel Gap

FIGURE 16 Simulation of Effect on Imagery of Gaps in CCD Focal Planes

a) Data from End Tap
Center Tap Bypassed

b) Data from End Tap
Center Tap Partially Activated

c) Data from Center Tap
Center Tap Activated

d) Data from End Tap
Center Tap Activated

FIGURE 17 Demonstration of Operation of Tap in Middle of CCD Register