FOURIER ANALYSIS COMPUTER-AIDED DESIGN OF CCD SIGNAL PROCESSING ANALOG MULTIPLIER ARRAYS

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ABSTRACT

When a CCD is used for signal processing, multipliers are required to multiply two signals or multiply the signal with a weight. The desired features of a multiplier are (a) low harmonic distortion, (b) wide dynamic range, (c) compatible signal levels, (d) small size, (e) low power dissipation, and (f) compatible with the CCD processing. From the design standpoint, many of these requirements are conflicting. This paper is a study of the design of MOS multipliers with CAD. In particular we use the Fourier analysis capability of the CAD program to analyze the harmonic distortion rejection, DR, of the multiplier.

I. INTRODUCTION

The multiplication function can be performed with MOS transistors operating in the triode region. The drain current I_D of an MOS transistor can be approximated as

$$I_D = \alpha\ (V_{GS} - V_T)\ V_{DS} + \beta V_{DS}^2 \qquad (1)$$

where V_{GS} is the gate to source voltage, V_T is the threshold voltage, V_{DS} is the drain to source voltage and (α, β) are physical parameters proportional to the width to length ratio and mobility of the channel. When the drain to source voltage is low, i.e. near the origin of the output characteristics, the square term in Eq. (1) is small and

$$I_D \approx \alpha\ (V_{GS} - V_T)\ V_{DS} \qquad (2)$$

If V_{GS} and V_{DS} represent two signals, then the drain current has a term ($\alpha\ V_{GS}\ V_{DS}$), which is proportional to the product of the two signals. If the two signals represented by V_{GS} and V_{DS} are substituted in Eq. (1) or Eq. (2), there are terms other than the desired multiplied outputs such as $\alpha\ V_{DS}\ V_T$ or $\beta\ V_{DS}^2/2$. These extraneous components of the drain current can be reduced in a balanced multiplier[1] as shown in Figure 1. But the signals may contain dc bias which must eventually be eliminated. One signal is given as $V_x \sin\theta$ with a dc offset V_X. The other signal is $V_y \sin\phi$ with a dc offset V_Y. The signal $V_X + V_x \sin\theta$ is applied to the common drain of Q_3 and Q_4. The signal $V_Y + V_y \sin\phi$ is applied to the gate of Q3, but only the offset voltage V_Y is applied to the gate of Q4. The currents of Q_3 and Q_4 can be obtained by substituting in Eq. (1) $V_X + V_x \sin\theta$ as V_{DS} and $V_Y + V_y \sin\phi$ as V_{GS} for Q_3 and V_Y as V_{GS} for Q_4.

$$I_{D3} = \alpha_3 \left[(V_Y + V_y \sin\phi - V_{T_3})\ (V_X + V_x \sin\theta)\right] + \beta_3 \left[(V_X + V_x \sin\theta)^2\right] \qquad (3)$$

$$I_{D4} = \alpha_4 \left[(V_Y - V_{T4})\ (V_X + V_x \sin\phi)\right] + \beta_4 \left[(V_X + V_x \sin\theta)^2\right] \qquad (4)$$

The differential output current I_{D0} is obtained by subtracting Eq. (4) from Eq. (3), assuming identical thresholds ($V_{T3} = V_{T4}$) and physical parameters ($\alpha_3 = \alpha_4$, $\beta_3 = \beta_4$):

$$I_{D0} = I_{D3} - I_{D4} = \alpha V_x V_y \sin\theta \sin\phi + \alpha V_X V_y \sin\phi \qquad (5)$$

But in a typical MOS array needed for a CCD correlator the assumptions used to give Eq. (5) are invalid, so that a four-quadrant sequential multiplication operation [2] is needed to eliminate terms due to array non-uniformities which degrade rejection of the two input frequencies. CAD Fourier analysis, however, facilitates evaluation of the susceptibility of various candidate circuits to degradation of distortion rejection due to MOS array nonuniformities.

II. EFFECTS OF DRIVING IMPEDANCES ON THE MULTIPLIER

For the proper operation of the multiplier, the driving point impedance should be low. Otherwise, the product current will develop a voltage across this impedance which would multiply with the voltage at the gate and cause distortion.

Since the impedance of a floating gate, from which the signal is derived is high compared with the channel resistance of the multiplier, a buffer must be placed between the floating gate and the

drain of the multiplier. A balanced multiplier can be used in conjunction with a source follower buffer as shown in figure 2.

Let R_{OB} be the output impedance of the buffer, then a voltage $I_{xy} R_{OB}$ would appear at the drain.

$$I_{xy} R_{ob} = \alpha V_x V_y R_{ob} \tag{6}$$

When multiplied by the gate signal V_y, an undesired product current I' is produced

$$I' = \alpha V_y (\alpha V_x V_y R_{OB}) \tag{7}$$

This current should be much less than the desired product current $\alpha V_x V_y$. Let the rejection ratio be DR. Then,

$$DR = \frac{\alpha V_x V_y}{\alpha V_y (\alpha V_x V_y R_{OB})} = \frac{1}{R_{OB} \alpha V_y} \tag{8}$$

where $\alpha = \mu C_{ox} W_x/L_x$ μ = mobility, W_x/L_x is the width to length ratio of the channel of the multiplier transistor. For the buffer

$$R_{ob} = \frac{L_B}{\mu C_{ox} W_B (V_{GS_B} - V_{T_B})} \tag{9}$$

where L_B, W_B are the length and width of the buffer.

Combining these three equations, we have this limitation from the drain buffer

$$\frac{(W_B/L_B)(V_{GS_B} - V_{T_B})}{W_x/L_x \quad V_y} = DR\Big]_{DB} \tag{10}$$

In a similar fashion, any impedance in series with the gate of the multiplier can develop a voltage by virtue of the feed-through capacitance from the drain of the multiplier transistor.[3] If the multiplier gate signal is directly derived from the floating gate of a CCD with sensing capacitance, C_{FG}, the impedance of the driver is the impedance of the capacitance C_{FG}. The voltage feedthrough is equal to $V_x C_{gdy}/C_{FG}$. If the desired signal is V_y, the rejection ratio limited by gate interaction is simply

$$\frac{V_y C_{FG}}{V_x C_{gdy}} = DR\Big]_G \tag{11}$$

One way to reduce the adverse effect of the feedthrough from the drain to the gate of the multiplier transistor is to place a buffer between the floating gate of the CCD and the gate of the multiplier. Because the gate of the multiplier should be more negative than the drain for p-channel transistors, it is easier to derive the proper d-c voltage with an inverter than a source follower. The schematic diagram for an inverter buffer at the gate is shown in Figure 3, complete with "dummy" sensing circuits for automatic multiplier biasing and clock feed-through cancellation (using small resistors in lieu of a differential current meter to facilitate CAD modeling).

Besides a lower impedance, it is also possible to increase the voltage gain. The output impedance is the source impedance of the load device, Q2:

$$\frac{1}{g_m} = \frac{1}{\alpha_2 (V_{GS2} - V_{T2})} \tag{12}$$

where V_{GS2} is the gate to source voltage of Q_2. The feedthrough signal from the drain now becomes

$$\frac{V_x}{\frac{1}{j\omega C_{gdy}} + \frac{1}{g_m}} \times \frac{1}{g_m} = \frac{V_x}{1 + \frac{\alpha_2 (V_{GS2} - V_T)}{j\omega C_{gdy}}} \tag{13}$$

The rejection ratio now becomes

$$DR\Big]_G = \frac{V_y}{V_x} \left[1 + \frac{\alpha_2 (V_{GS2} - V_T)}{j\omega C_{gdy}}\right] \tag{14}$$

III. ANALYSIS OF THE MULTIPLIER WITH A DRAIN BUFFER ONLY

For the proper operation of the multiplier in Figure2 the drain of the multiplier transistor Q_3 should be driven from a voltage source; i.e., the output conductance of the source follower (Q_1, Q_2), should be larger than the conductance of the multiplier Q_3. If the current source Q_2, is operating in the pentode region, the output conductance, Q_1 should be operating as a pentode. The output conductance is then equal to

$$\frac{dI_{D1}}{dV_{GS1}} = \alpha_1 (V_{GS1} - V_{T1}) = g_{m1} \tag{15}$$

where α_1 is a geometry constant, V_{GS1} is the gate to source voltage, V_{T1} is the threshold voltage, and g_{m1} is the transconductance. If V_X is the d-c voltage of the first signal appearing at the gate of Q_1 and V_3 is the d-c source voltage then source-follower operation gives:

$$V_{GS1} = V_X - V_3 \tag{16}$$

The drain voltage of Q_2 is also V_3 and the gate voltage should be chosen to operate in the pentode region. One convenient way is to make the gate

voltage of Q_2 equal to V_3. For equal geometry of Q_1 and Q_2,

$$V_X - V_3 - V_{T1} = V_3 - V_{T2} \tag{17}$$

If the self-biasing effect is small, $V_{T1} \cong V_{T2}$

$$V_3 = V_X/2 \tag{18}$$

Combining (15), (16), (18)

$$g_{m1} = \alpha_1 (V_X/2 - V_{T1}) \tag{19}$$

This conductance should be larger than the conductance of the multiplier:

$$g_3 = \frac{dI_{D3}}{dV_{DS}} = \alpha_3 (V_{GS} - V_{T3}) \tag{20}$$

or

$$g_{m1} \geq g_3 \tag{21}$$

If the two signals are at the same d-c level then

$$V_{GS1} = V_{GS3} = V_X/2 \tag{22}$$

Equation (21) can be satisfied if

$$\alpha_1 (V_X/2 - V_{T1}) \geq \alpha_3 (V_X/2 - V_{T3}) \tag{23}$$

If all the transistors have the same threshold voltage, then

$$\alpha_1 \geq \alpha_3 \tag{24}$$

Since α_1 and α_3 are proportional to the width to length ratios, it is desirable to have

$$\frac{W_1}{L_1} \geq \frac{W_3}{L_3} \tag{25}$$

Meanwhile, the multiplier transistor must not be cut off, i.e. (from eqn. 22)

$$V_X > 2V_{T3}. \tag{26}$$

From the standpoint of linearity, it is desirable to use a large amplitude V_X; because the linear triode region, where the linear multiplication function is performed, should be large compared to the signal. Thus, the larger the dc signal level V_X, the closer the multiplier approximates operation near the origin of eqn 1 and the better is the harmonic distortion rejection. On the other hand, a large value of V_X gives rise to large dissipation, and the choice of V_X is a compromise between distortion and dissipation.

The dissipation of the drain-buffered multiplier is essentially due to the buffer and is equal to

$$P_d \cong \alpha_2 (V_X/2 - V_{T2})^2 V_X \tag{27}$$

If, to satisfy Eqn (26), one chooses

$$V_X = 2 (V_{T2} + V^*) \tag{28}$$

Then from Eq. (27),

$$P_d \cong 2 \alpha_2 (V^*)^2 (V_{T2} + V^*) \tag{29}$$

From Eq. (29), we can see that a lower V_T reduces the power dissipation. Therefore, a <100> crystal orientation with a low threshold voltage should give reduced power consumption. A depletion mode transistor should help similarly.

Another consideration in designing a multiplier is the output current,

$$I = \alpha_3 \left[(V_X + V_x \sin\theta) \left(\frac{g_{m1}}{g_{m1}+g_{m2}+g_3} \right) (V_Y + V_y \sin\phi - V_{T3}) \right] \tag{30}$$

The desired output is the product term,

$$\frac{\alpha_3 g_{m1}}{g_{m1}+g_{m2}+g_3} (V_x V_y \sin\theta \sin\phi)$$

From (19) and (20)

$$\frac{\alpha_3 g_{m1}}{g_{m1}+g_{m2}+g_3} = \frac{\alpha_1 \alpha_3 \left(\frac{V_X}{2} - V_{T1} \right)}{\alpha_1 \left(\frac{V_X}{2} - V_{T1} \right) + \alpha_2 \left(\frac{V_X}{2} - V_{T2} \right) + \alpha_3 \left(\frac{V_X}{2} - V_{T3} \right)} \tag{31}$$

Here we see that larger geometry multipliers increase the desired output signal current but only up to the point where buffer loading occurs. This is in concert with equation (10), which shows that distortion rejection performance requires very limited loading by the multiplier on the drain buffer.

IV. THE FULLY BUFFERED MULTIPLIER

With a single (source-follower) buffer to drive the multiplier drain, the signal for the gate of the multiplier is assumed to be directly derived from the floating clock of a CCD. There are some advantages if an inverter is placed between the floating clock and the gate of the multiplier. a) Voltage

gain achieved for the signal. b) Reduced capacitive feed through from the signal at the drain of the multiplier to the gate of the multiplier. While the inverter lowers the driving point impedance, gain may reduce the d-c voltage developed at the multiplier gate and simultaneously increase the ac signal voltage there.

In Figure 3, if the amplifying transistor Q_1 and the load device Q_2 are of the same minimum geometry and both transistors are operating in the pentode region; then the voltage gain is unity, and the output conductance is the transconductance of the load device. To operate Q_1 in the pentode region, the following condition should be satisfied:

$$V_{DS1} = V_3 \geq V_Y - V_{T1} \tag{32}$$

Since the same current must flow in both Q_1 and Q_2, for pentode operation we must have

$$I_1 \cong \frac{\alpha_1}{2} (V_{GS1} - V_{T1})^2 = I_2 \cong \frac{\alpha_2}{2} (V_{GS2} - V_{T2})^2$$

or

$$V_{DD} - V_3 - V_{T2} = (V_Y - V_{T1}) \cdot \left(\frac{\alpha_1}{\alpha_2}\right)^{1/2} \tag{33}$$

But the unloaded voltage gain, A_v, of such an inverter may be approximated by:

$$A_v = g_m Z_L = \frac{g_{m1}}{g_{m2}} = \frac{\alpha_1 (V_{GS1} - V_{T1})}{\alpha_2 (V_{GS2} - V_{T_2})} = \left(\frac{\alpha_1}{\alpha_2}\right)^{1/2} \cdot \left(\frac{I_1}{I_2}\right)^{1/2} = \left(\frac{\alpha_1}{\alpha_2}\right)^{1/2} \tag{34}$$

Combing (32), (33), and (34) gives: $V_{DD} \geq (1 + A_v)(V_Y - V_{T1}) + V_{T2}$ (35)

For the case of unity gain and comparable threshold voltages, the minimum V_{DD} becomes $(2 V_Y - V_T)$. Also equation (35) indicates that the power dissipation of the multiplier gate buffer, P_g, increases directly with the voltage gain:

$$P_g \cong \alpha_1 (V_Y - V_{T1})^2 (1 + A_V) (V_Y) \tag{36}$$

Application of eqn (27) to Figure 3 gives

$$P_d \cong \alpha_{16} (V_X/2 - V_{T16})^2 V_X \tag{37}$$

Again invoking the requirement that the multiplier not be cut-off for the dual buffered circuit of Figure 3, we find

$$V_{GS4} = (V_Y - V_X/2) > V_{T4} \tag{38}$$

To simplify the operation of the two CCD's, it is desireable to use common clock and bias levels, so that one may again want to apply

$$V_X \simeq V_Y \simeq 2(V_T + V^*) , \tag{39}$$

yielding a combined power per multiplier stage of

$$P = P_d + P_g = 2(V_T + V^*) \left[\alpha_{16} (V^*)^2 + \alpha_1 (1 + A_V) (2V^* + V_T)^2\right] \tag{40}$$

The benefits of low threshold and operating voltages are certainly apparent to minimize on-chip heat generation.

V. THE FOURIER ANALYSIS BY CAD

The distortion error of a multiplier can best be determined by Fourier analysis as shown in Eq. (5), the desired term is the product term. If the two input signals are harmonically related say $\phi = N\theta$, where N is an integer, then the desired output is $^{\alpha} V_x V_y \sin\theta \sin N\theta$. From trigonometry, this product term can be resolved as a sum and difference frequency terms.

$$\sin\theta \sin N\theta = 1/2 \left[\text{Cos } (N-1)\theta - \text{Cos } (N+1)\theta\right] \tag{41}$$

All other frequency components are undesirable. The distortion rejection ratio can be defined as

$$DR = \frac{V^2 (f_G - f_D) + V^2 (f_G + f_D)}{(NYQUIST)}$$

$$\sum_{(m,\ p)} = \sum_2 \left[V^2 (mf_D - f_G) + V^2 (pf_G - f_D) + V^2 (f_D) + V^2 (f_G) + V^2 (pf_G \pm mf_D)\right] \tag{42}$$

The different frequency components of a Fourier Analysis can readily be obtained with a CAD program.

VI. RESULTS OF CAD FOURIER ANALYSIS

Many circuit configurations were considered and evaluated by means of CAD Fourier analysis, including (i) MOSFET circuits consisting of all the same type devices requiring no extra fabrication steps beyond those needed to make CCD's, (ii) circuits incorporating depletion mode devices, (iii) complementary MOSFET circuits, (iv) combined MOS and bipolar circuits, and (v) permutations of all the preceeding. The MSINC CAD program developed by Standord University was used for all non-bipolar circuits. To best illustrate important aspects of the CAD Fourier analysis technique, we have selected one of the many circuit configurations studied: in particular, a fully buffered MOSFET circuit fabricated completely

within a typical CCD manufacturing sequence, featuring complementary operation as shown in Figure 3. Most of the significant data from four different computer runs for the selected circuit (PCWCO = PMOS correlator with complimentary operation) are presented in Tables 1 through 4, where the bottom-most harmonic listing describes the single multiplier current (I_4 =(V8, 17)÷ 10 ohms) while the harmonics above that give the differential output current. A summary of the CAD data is then listed in Table 5, to facilitate comparison with the preceeding general analysis. For the purpose of the CAD Fourier analysis, all other CCD clocks and switches (like the floating clock switch) are assumed to be in the state they would occupy at the time of anlalog readout. Furthermore, although the a-c-signal surface potential variations in a CCD typically exceed one volt amplitude, considerable attenuation of that amplitude due to parasitic capacitive loading has been incorporated into the model by setting the applied sine-wave signals at one-quarter volt peak-to-peak. (Tabulated amplitudes are from center to peak.) Both the ac and dc conditions used in the model closely approximate those observed in our own non-destructive parallel read-out CCD[4].

Run PCWCO-4-3, shown in Table 1, describes a PERFECTLY UNIFORM array with the CCD operated to give an ac "Fat Zero" level of about ten volts on the floating clock. In Table 2 (Run PCWCO-4-5) a nonuniform multiplier threshold offset of 0.25 V. is introduced, and the effects are comparable to such an offset in the floating clock/gate buffer circuit. A 0.25V. threshold offset nonuniformity in a floating clock/drain buffer is contained in Table 3 (PCWCO-4-6). The final run (PCWCO-4-2) shown in Table 4 is again a perfectly uniform array but with higher voltage operation. The summary of results (Table 5) accentuates the following conclusions:

(1) The theory of the SEQUENTIAL four-quadrant multiplier nominally requires only a single transistor, not a differential matched pair. Table 5, however, shows that rejection of the input drain signal would be substantially more difficult by around 80 dB. (i.e., the sequential cancellation of two extremely large quantities is required.)

(2) The differential circuit enhances the rejection of the drain signal second harmonic by at least 20 dB over the single FET multiplier.

(3) An increase from 10V. to 12V. for the ac Fat Zero level nearly doubled the power consumption per multiplier but did not proportionately improve the distortion rejection, due to the resultant loading (see #7 below).

(4) Two identical minimum-geometry devices as biased in the inverter give a gain around half; while two identical larger devices give a slightly larger gain as source followers. The inverter was just barely into the pentode region, which may be cured by a larger V_{DD} bias, that increases power consumption.

(5) Array nonuniformities which introduce multiplier source-drain offsets will degrade rejection of the input gate frequency and the intermodulation of the gate frequency with the second harmonic of the drain signal as well as the drain signal and its second harmonic to a smaller extent.

(6) Array nonuniformities which introduce multiplier differential gate offsets degrade rejection of the input drain signal and its second harmonic.

(7) The limited range tabulated for loading (λ) by the multiplier on the drain buffer falls totally within the region that the source-follower buffer gain (A_D) is being degraded by the multiplier load:

$$A_D = \frac{g_m R_s}{1 + g_m R_s} = \frac{1}{1 + g_{ds}/g_m} = \frac{1}{1 + \lambda^{-1}} \quad (43)$$

This equation describes the tabulated correlation between A_D, λ, and, consequently, the desired output signal via eqn (31). Since this group of runs does not involve greatly reduced loading, there is no apparent relationship between distortion rejection and λ; and eqn (10) is not truly applicable.

Some of the more promising configurations are now undergoing experimental hybrid-device laboratory evaluation. The observed characteristics closely match the CAD Fourier Analysis predictions like those exhibited in Tables 1 through 5. Figure 4 illustrates the typical output of a minimum geometry PMOSFET pair with

V_{DS} = 51 mV. DC and 0.2 V_{pp} at 1 KHz

V_{GS} = 3.962 V. DC and 0.2 V_{pp} at 5 KHz

V_{SB} = 11.78 V. DC and ΔV_G = 142 mV.

VII. SUMMARY/CONCLUSIONS

CAD Fourier analysis of analog multiplier arrays for CCD signal processing facilitates comprehensive study of most practical device configurations before commitment to mask layout is required. The CAD Fourier analysis technique helps evaluate many trade-off options and

interactions between the following: (1) Device technology such as simple MOS, MOS with depletion mode FET's, CMOS, and MOS with bipolar. (2) Area and complexity of each buffered multiplier circuit. (3) Circuit performance to include drive and signal compatibility with the associated CCD's, power consumption, output signal amplitude and distortion rejection, and susceptibility of circuit performance to array nonuniformities.

Computer predictions and laboratory multichip hybrid models agree reasonably when such comparisons are possible.

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Table 1. Perfect Uniform Array, No Offsets (PCWCO-4-3)

```
TIME 1U 200U
RA 8 17 10
RB 9 17 10
C8 8 0 5P
C9 9 0 5P
C16 16 0 .5P
C17 17 0 5800U
C10 10 0 .5P
Q1 BP1 3 2 6 0 .7M .7M 0 0 .07P .07P
Q2 BP1 4 4 3 0 .7M .7M 0 0 .07P .07P
Q4 BP1 16 3 8 0 2.8M .7M 0 0 .28P .28P
Q5 BP1 16 10 9 0 2.8M .7M 0 0 .28P .28P
Q3 BP1 10 7 0 0 .7M .7M 0 0 .07P .07P
Q6 BP1 4 4 10 0 .7M .7M 0 0 .07P .07P
Q14 BP1 16 17 0 0 14M .7M 0 0 .07P .07P
Q15 BP1 17 17 0 0 14M .7M 0 0 .07P .07P
Q16 BP1 7 6 16 0 14M .7M 0 0 .07P .07P
Q17 BP1 7 7 17 0 14M .7M 0 0 .07P .07P
BP1 PMO VTO=-2 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
BP2 PMO VTO=-2.25 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
V4 4 0 -20
V7 7 0 -10
VSIN 6 0 .125V 6KHZ 0 -10
VSIN 2 0 .125V 30KHZ 0 -10
PLOT VOUT 8 9
PLOT V5 16 0
PLOT V3 3 0
PLOT V8 8 17
PLOT V6 3 10
PLOT V17 17 0
FOR 30U 196.667U 20
END
```

NODE VOLTAGES --

(0)	.0000	(2)	-10.0000	(3)	-8.7846	(4)	-20.0000
(6)	-10.0000	(7)	-10.0000	(8)	-4.4624	(9)	-4.4624
(10)	-8.7846	(16)	-4.4624	(17)	-4.4624		

TRANSISTOR OP. PT. --

NAME	TP	VGS	VDS	VSB	IDS(MA)
Q1	P	-10.0000	-8.7846	.0000	-.1291
Q2	P	-11.2154	-11.2154	-8.7846	-.1291
Q4	P	-4.3221	-.0000	-4.4624	-.0000
Q5	P	-4.3221	-.0000	-4.4624	-.0000
Q3	P	-10.0000	-8.7846	.0000	-.1291
Q6	P	-11.2154	-11.2154	-8.7846	-.1291
Q14	P	-4.4624	-4.4624	.0000	-.3026
Q15	P	-4.4624	-4.4624	.0000	-.3026
Q16	P	-5.5376	-5.5376	-4.4624	-.3026
Q17	P	-5.5376	-5.5376	-4.4624	-.3026

	ORDER	HARM	DSINE	COOSINE	MAGNITUDE	REL MAG	PHASE
V89:		0	.0000	-.1267-10	.1267-10	5.3795	180.0000
		1	.2022-09	.1209-09	.2356-09	100.0000	-59.1188
		2	.3119-09	.6844-11	.3120-09	132.4361	-88.7430
		3	-.2942-08	-.1109-08	.3145-08	1334.8697	110.6585
		4	.4757-06	-.8919-07	.4840-06	205439.9595	-100.6191
		5	-.7262-08	.1737-08	.7467-08	3169.5422	76.5503
		6	.2264-06	-.4069-06	.4656-06	197655.0427	-150.9082
		7	-.1645-09	.2663-08	.2668-08	1132.3948	3.5362
		8	-.2496-09	-.7649-09	.8046-09	341.5345	161.9263
		9	-.1008-09	-.4966-09	.5067-09	215.0972	168.5307
		10	-.1678-09	-.3498-09	.3879-09	164.6712	154.3725
		11	-.2007-09	-.3724-09	.4230-09	179.5752	151.6817
		12	-.7872-10	-.3059-09	.3158-09	134.0631	165.5675
		13	-.5805-10	-.3812-09	.3856-09	163.6592	171.3406
		14	-.2275-10	-.3482-09	.3489-09	148.1193	176.2024
		15	-.6252-10	-.3593-09	.3647-09	154.8230	170.1300
		16	-.2663-10	-.3775-09	.3784-09	160.6288	175.9649
		17	-.4544-10	-.3532-09	.3561-09	151.1591	172.6681
		18	-.2519-10	-.3951-09	.3959-09	168.0653	176.3528
		19	-.2114-10	-.3737-09	.3743-09	158.8854	176.7619
		20	-.3655-10	-.4156-09	.4172-09	177.0943	174.9741
V817:		0	.0000	.2722-06	.2722-06	1.5494	.0000
		1	.7466-05	.1590-04	.1757-04	100.0000	-25.1475
		2	.2073-06	.1723-06	.2695-06	1.5341	-50.2653
		3	-.6232-08	-.1670-08	.6451-08	.0367	105.0009
		4	.4447-06	-.8296-07	.4524-06	2.5747	-100.5674
		5	-.8786-08	.2834-08	.9232-08	.0525	72.1259
		6	.2117-06	-.3800-06	.4350-06	2.4758	-150.8732
		7	-.1684-09	.3758-08	.3762-08	.0214	2.5658
		8	-.1496-09	-.4339-09	.4590-09	.0026	160.9762
		9	-.7467-10	-.1873-09	.2017-09	.0011	158.2671
		10	-.1028-09	-.5846-10	.1183-09	.0007	119.6193
		11	-.1747-09	-.5412-10	.1829-09	.0010	107.2119
		12	-.6024-10	-.2233-10	.6425-10	.0004	110.3359
		13	-.4383-10	-.6039-10	.7462-10	.0004	144.0733
		14	-.3691-10	-.4635-10	.5926-10	.0003	141.4682
		15	-.5933-10	-.4428-10	.7403-10	.0004	126.7346
		16	-.5602-10	-.5300-10	.7712-10	.0004	133.4104
		17	-.6512-10	-.3799-10	.7539-10	.0004	120.2568
		18	-.6212-10	-.5262-10	.8141-10	.0005	130.2676
		19	-.6883-10	-.4481-10	.8213-10	.0005	123.0863
		20	-.8110-10	-.6068-10	.1013-09	.0006	126.8057

Table 2. An Offset (0.25V) Multiplier Threshold (or Floating Clock/Gate Buffer) (PCWCO-4-5)

```
TIME 1U 200U
RA 8 17 10
RB 9 17 10
C8 8 0 5P
C9 9 0 5P
C16 16 0 .5P
C17 17 0 5800U
C10 10 0 .5P
Q1 BP1 3 2 0 0 .7M .7M 0 0 .07P .07P
Q2 BP1 4 4 3 0 .7M .7M 0 0 .07P .07P
Q4 BP2 16 3 8 0 2.8M .7M 0 0 .28P .28P
Q5 BP1 16 10 9 0 2.8M .7M 0 0 .28P .28P
Q3 BP1 10 7 0 0 .7M .7M 0 0 .07P .07P
Q6 BP1 4 4 10 0 .7M .7M 0 0 .07P .07P
Q14 BP1 16 17 0 0 14M .7M 0 0 .07P .07P
Q15 BP1 17 17 0 0 14M .7M 0 0 .07P .07P
Q16 BP1 7 6 16 0 14M .7M 0 0 .07P .07P
Q17 BP1 7 7 17 0 14M .7M 0 0 .07P .07P
BP1 PMO VTO=-2 UB=250,6E4,.15 COX=23N ONB=1E15 XJD=.3M GDS=2 CSS=.5P
BP2 PMO VTO=-2.25 UB=250,6E4,.15 COX=23N ONB=1E15 XJD=.3M GDS=2 CSS=.5P
V4 4 0 -20
V7 7 0 -10
VSIN 6 0 .125V 6KHZ 0 -10
VSIN 2 0 .125V 30KHZ 0 -10
PLOT VOUT 8 9
PLOT V0 16 0
PLOT V3 3 0
PLOT V8 8 17
PLOT V8 3 10
PLOT V17 17 0
FOR 30U 196.667U 20
END
```

NODE VOLTAGES --

(0)	.0000	(2)	-10.0000	(3)	-8.7846	(4)	-20.0000
(6)	-10.0000	(7)	-10.0000	(8)	-4.4624	(9)	-4.4624
(10)	-8.7846	(16)	-4.4624	(17)	-4.4624		

TRANSISTOR OP. PT. --

NAME	TP	VGS	VDS	VSB	IDS(MA)
Q1	P	-10.0000	-8.7846	.0000	-.1291
Q2	P	-11.2154	-11.2154	-8.7846	-.1291
Q4	P	-4.3221	-.0000	-4.4624	-.0000
Q5	P	-4.3221	-.0000	-4.4624	-.0000
Q3	P	-10.0000	-8.7846	.0000	-.1291
Q6	P	-11.2154	-11.2154	-8.7846	-.1291
Q14	P	-4.4624	-4.4624	.0000	-.3026
Q15	P	-4.4624	-4.4624	.0000	-.3026
Q16	P	-5.5376	-5.5376	-4.4624	-.3026
Q17	P	-5.5376	-5.5376	-4.4624	-.3026

ORDER	HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
V89:	0	.0000	.2281-07	.2281-07	.6164	.0000
	1	-.1572-05	-.3350-05	.3701-05	100.0000	154.8549
	2	.1780-07	.1443-07	.2292-07	.6192	-50.9759
	3	-.3536-08	-.1335-08	.3779-08	.1021	110.6825
	4	.5000-06	-.9383-07	.5088-06	13.7477	-100.6284
	5	-.7884-08	.2166-08	.8176-08	.2209	74.6347
	6	.2380-06	-.4278-06	.4895-06	13.2278	-150.9148
	7	-.2014-09	.2978-08	.2985-08	.0807	3.8695
	8	-.2840-09	-.8711-09	.9163-09	.0248	161.9435
	9	-.2433-10	-.4964-09	.4970-09	.0134	177.1941
	10	-.1950-09	-.4233-09	.4661-09	.0126	155.2638
	11	-.1069-09	-.4618-09	.4740-09	.0128	166.9616
	12	-.8853-10	-.3708-09	.3812-09	.0103	166.5725
	13	-.6343-10	-.4597-09	.4641-09	.0125	172.1436
	14	-.2068-10	-.4199-09	.4204-09	.0114	177.1797
	15	-.6626-10	-.4362-09	.4402-09	.0119	171.3428
	16	-.2146-10	-.4554-09	.4559-09	.0123	177.3024
	17	-.4405-10	-.4282-09	.4305-09	.0116	174.1266
	18	-.1930-10	-.4779-09	.4783-09	.0129	177.6874
	19	-.1302-10	-.4523-09	.4525-09	.0122	178.3511
	20	-.3011-10	-.5015-09	.5024-09	.0136	176.5637
V817:	0	.0000	.3020-06	.3020-06	2.1403	.0000
	1	.5996-05	.1277-04	.1411-04	100.0000	-25.1477
	2	.2301-06	.1911-06	.2991-06	2.1198	-50.2623
	3	-.6963-08	-.1926-08	.7224-08	.0512	105.4586
	4	.4674-06	-.8730-07	.4755-06	3.3701	-100.5792
	5	-.9471-08	.3310-08	.1003-07	.0711	70.7340
	6	.2225-06	-.3995-06	.4573-06	3.2409	-150.8814
	7	-.2068-09	.4114-08	.4119-08	.0292	2.8781
	8	-.1825-09	-.5348-09	.5650-09	.0040	161.1563
	9	-.2982-11	-.1866-09	.1867-09	.0013	179.0847
	10	-.1268-09	-.1269-09	.1808-09	.0013	134.5672
	11	-.8699-10	-.1373-09	.1625-09	.0012	147.6362
	12	-.6962-10	-.8242-10	.1079-09	.0008	139.8150
	13	-.4887-10	-.1334-09	.1421-09	.0010	159.8811
	14	-.3497-10	-.1129-09	.1182-09	.0008	162.7867
	15	-.6288-10	-.1147-09	.1308-09	.0009	151.2673
	16	-.5121-10	-.1254-09	.1355-09	.0010	157.7884
	17	-.6389-10	-.1076-09	.1252-09	.0009	149.3039
	18	-.5669-10	-.1295-09	.1414-09	.0010	156.3643
	19	-.6132-10	-.1177-09	.1327-09	.0009	152.4877
	20	-.7521-10	-.1405-09	.1593-09	.0011	151.8328

Table 3. An Offset (0.25V) Floating Clock/Drain Buffer (PWCO-4-6)

```
TIME 1U 200U
RA 8 17 10
RB 9 17 10
C8 8 0 5P
C9 9 0 5P
C16 16 0 .5P
C17 17 0 5800U
C10 10 0 .5P
Q1 BP1 3 2 0 0 .7M .7M 0 0 .07P .07P
Q2 BP1 4 4 3 0 .7M .7M 0 0 .07P .07P
Q4 BP1 16 3 8 0 2.8M .7M 0 0 .28P .28P
Q5 BP1 16 10 9 0 2.8M .7M 0 0 .28P .28P
Q3 BP1 10 7 0 0 .7M .7M 0 0 .07P .07P
Q6 BP1 4 4 10 0 .7M .7M 0 0 .07P .07P
Q14 BP1 16 17 0 0 14M .7M 0 0 .07P .07P
Q15 BP1 17 17 0 0 14M .7M 0 0 .07P .07P
Q16 BP2 7 6 16 0 14M .7M 0 0 .07P .07P
Q17 BP1 7 7 17 0 14M .7M 0 0 .07P .07P
BP1 PMO VTO=-2 UB=250.6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
BP2 PMO VTO=-2.25 UB=250.6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
V4 4 0 -20
V7 7 0 -10
VSIN 6 0 .125V 6KHZ 0 -10
VSIN 2 0 .125V 30KHZ 0 -10
PLOT VOUT 8 9
PLOT VO 16 0
PLOT V3 3 0
PLOT V8 8 17
PLOT VG 3 10
PLOT V17 17 0
FOR 30U 196.667U 20
END
```

NODE VOLTAGES --

(0)	.0000	(2)	-10.0000	(3)	-8.7846	(4)	-20.0000
(6)	-10.0000	(7)	-10.0000	(8)	-4.4501	(9)	-4.4501
(10)	-8.7846	(16)	-4.3125	(17)	-4.4501		

TRANSISTOR OP. PT. --

NAME	TP	VGS	VDS	VSB	IDS(MA)
Q1	P	-10.0000	-8.7846	.0000	-.1291
Q2	P	-11.2154	-11.2154	-8.7846	-.1291
Q4	P	-4.3345	.1376	-4.4501	.0033
Q5	P	-4.3345	.1376	-4.4501	.0033
33	P	-10.0000	-8.7846	.0000	-.1291
Q6	P	-11.2154	-11.2154	-8.7846	-.1291
Q14	P	-4.4501	-4.3125	.0000	-.2980
Q15	P	-4.4501	-4.4501	.0000	-.2995
Q16	P	-5.6875	-5.6875	-4.3125	-.2914
Q17	P	-5.5499	-5.5499	-4.4501	-.3061

ORDER	HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
V89:	0	.0000	.1541-08	.1541-08	111.0164	.0000
	1	.8261-09	.1116-08	.1388-08	100.0000	-36.5218
	2	-.8756-09	-.1401-08	.1652-08	119.0382	148.0041
	3	-.7616-08	-.2560-08	.8035-08	578.8249	108.5779
	4	.4426-06	-.8350-07	.4504-06	32447.1410	-100.6830
	5	.1303-05	-.9419-06	.1608-05	115845.2490	-125.8525
	6	.2106-06	-.3787-06	.4333-06	31216.7599	-150.9253
	7	-.6241-09	.6808-08	.6837-08	492.5152	5.2372
	8	.1999-09	-.2778-09	.3423-09	24.6562	-144.2590
	9	-.1114-08	-.1837-08	.2149-08	154.7760	148.7535
	10	-.1492-08	-.1344-08	.2008-08	144.6763	132.0099
	11	-.2541-09	-.8337-09	.8715-09	62.7846	163.0474
	12	.8675-10	-.1011-08	.1014-08	73.0756	-175.0943
	13	-.1505-09	-.7970-09	.8111-09	58.4295	169.3083
	14	-.1652-09	-.7133-09	.7322-09	52.7488	166.9593
	15	-.1252-09	-.8848-09	.8936-09	64.3726	171.9439
	16	-.1996-09	-.9289-09	.9501-09	68.4407	167.8712
	17	-.1335-09	-.8999-09	.9098-09	65.5381	171.5591
	18	-.7761-10	-.8960-09	.8994-09	64.7899	175.0498
	19	-.1057-09	-.9522-09	.9580-09	69.0151	173.6658
	20	-.1225-09	-.9425-09	.9504-09	68.4649	172.5936
V817:	0	.0000	.3273-04	.3273-04	172.4026	.0000
	1	.8068-05	.1719-04	.1899-04	100.0000	-25.1478
	2	-.3012-07	-.2512-07	.3922-07	.2066	129.8229
	3	-.6221-07	-.1640-07	.6433-07	.3388	104.7673
	4	.4480-06	-.8402-07	.4558-06	2.4009	-100.6222
	5	.1231-05	-.8898-06	.1519-05	8.0013	-125.8571
	6	.1912-06	-.3432-06	.3929-06	2.0693	-150.8843
	7	-.1558-08	.2161-07	.2167-07	.1141	4.1238
	8	.5230-09	.6807-09	.8584-09	.0045	-37.5368
	9	-.6739-08	-.6865-08	.9620-08	.0507	135.5319
	10	-.3902-08	-.1825-08	.4307-08	.0227	115.0646
	11	.3743-08	-.9270-09	.3856-08	.0203	-103.9097
	12	.2486-08	-.2149-08	.3286-08	.0173	-130.8447
	13	-.1084-08	.1038-08	.1501-08	.0079	46.2547
	14	-.4834-09	.1880-08	.1941-08	.0102	14.4183
	15	-.2866-09	-.1064-08	.1102-08	.0058	164.9214
	16	-.1321-08	-.1752-08	.2194-08	.0116	142.9857
	17	-.1055-09	-.5098-09	.5206-09	.0027	168.3108
	18	.1013-08	-.5513-09	.1153-08	.0061	-118.5581
	19	-.2817-10	-.6324-09	.6330-09	.0033	177.4494
	20	-.6564-09	.1200-09	.6672-09	.0035	79.6417

Table 4. No Offsets; Higher Voltage Operation (PCWCO-4-2)

```
TIME 1U 200U
RA 8 17 10
RB 9 17 10
C8 8 0 5P
C9 9 0 5P
C16 16 0 .5P
C17 17 0 5800U
C10 10 0 .5P
Q1 BP1 3 2 0 0 .7M .7M 0 0 .07P .07P
Q2 BP1 4 4 3 0 .7M .7M 0 0 .07P .07P
Q4 BP1 16 3 8 0 2.8M .7M 0 0 .28P .28P
Q5 BP1 16 10 9 0 2.8M .7M 0 0 .28P .28P
Q3 BP1 10 7 0 0 .7M .7M 0 0 .07P .07P
Q6 BP1 4 4 10 0 .7M .7M 0 0 .07P .07P
Q14 BP1 16 17 0 0 14M .7M 0 0 .07P .07P
Q15 BP1 17 17 0 0 14M .7M 0 0 .07P .07P
Q16 BP1 7 6 16 0 14M .7M 0 0 .07P .07P
Q17 BP1 7 7 17 0 14M .7M 0 0 .07P .07P
BP1 PMO VTO=-2 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
BP2 PMO VTO=-2.25 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
V4 4 0 -24
V7 7 0 -12
VSIN 6 0 .125V 6KHZ 0 -12
VSIN 2 0 .125V 30KHZ 0 -12
PLOT VOUT 8 9
PLOT VD 16 0
PLOT V3 3 0
PLOT V8 8 17
PLOT VG 3 10
PLOT V17 17 0
FOR 30U 196.667U 20
END
```

NODE VOLTAGES --

(0)	.0000	(2)	-12.0000	(3)	-10.6794	(4)	-24.0000
(6)	-12.0000	(7)	-12.0000	(8)	-5.4035	(9)	-5.4035
(10)	-10.6794	(16)	-5.4035	(17)	-5.4035		

TRANSISTOR OP. PT. --

NAME	TP	VGS	VDS	VSB	IDS(MA)
Q1	P	-12.0000	-10.6794	.0000	-.1975
Q2	P	-13.3206	-13.3206	-10.6794	-.1975
Q4	P	-5.2758	-.0000	-5.4035	-.0000
Q5	P	-5.2758	-.0000	-5.4035	-.0000
Q3	P	-12.0000	-10.6794	.0000	-.1975
Q6	P	-13.3206	-13.3206	-10.6794	-.1975
Q14	P	-5.4035	-5.4035	.0000	-.5546
Q15	P	-5.4035	-5.4035	.0000	-.5546
Q16	P	-6.5965	-6.5965	-5.4035	-.5546
Q17	P	-6.5965	-6.5965	-5.4035	-.5546

ORDER	HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
V89:	0	.0000	-.2959-10	.2959-10	2.2089	180.0000
	1	.6670-09	.1162-08	.1340-08	100.0000	-29.8581
	2	.2327-09	-.1611-10	.2333-09	17.4102	-93.9598
	3	-.1350-08	-.6318-09	.1490-08	111.2334	115.0853
	4	.3898-06	-.7306-07	.3966-06	29600.9913	-100.6156
	5	-.4553-08	-.2802-10	.4553-08	339.8208	90.3526
	6	.1856-06	-.3334-06	.3816-06	28479.3551	-150.9007
	7	-.6174-10	.1165-08	.1167-08	87.0957	3.0332
	8	-.1975-09	-.6103-09	.6414-09	47.8777	162.0628
	9	-.4497-09	-.7588-09	.8820-09	65.8339	149.3453
	10	-.1196-09	-.2814-09	.3058-09	22.8235	156.9661
	11	-.6260-09	-.2536-09	.6772-09	50.5501	111.9908
	12	-.5751-10	-.2571-09	.2634-09	19.6639	167.3899
	13	-.4784-10	-.3124-09	.3161-09	23.5924	171.2942
	14	-.1880-10	-.2855-09	.2861-09	21.3575	176.2324
	15	-.5048-10	-.2958-09	.3001-09	22.3994	170.3161
	16	-.2025-10	-.3098-09	.3104-09	23.1711	176.2607
	17	-.3612-10	-.2914-09	.2936-09	21.9145	172.9341
	18	-.1962-10	-.3254-09	.3260-09	24.3308	176.5494
	19	-.1607-10	-.3082-09	.3086-09	23.0332	177.0152
	20	-.2834-10	-.3423-09	.3434-09	25.6344	175.2675
V817:	0	.0000	.2087-06	.2087-06	.8116	.0000
	1	.1093-04	.2328-04	.2572-04	100.0000	-25.1454
	2	.1585-06	.1320-06	.2063-06	.8021	-50.2035
	3	-.2497-08	-.5290-09	.2552-08	.0099	101.9603
	4	.3615-06	-.6716-07	.3677-06	1.4297	-100.5246
	5	-.5324-08	.6422-09	.5362-08	.0209	83.1217
	6	.1722-06	-.3086-06	.3534-06	1.3743	-150.8398
	7	-.1632-10	.1953-08	.1953-08	.0076	.4786
	8	-.5398-10	-.1452-09	.1549-09	.0006	159.6017
	9	-.3929-09	-.3082-09	.4994-09	.0019	128.1132
	10	-.3032-10	.1219-09	.1256-09	.0005	13.9656
	11	-.5647-09	.1872-09	.5950-09	.0023	71.6535
	12	-.3330-10	.1367-09	.1407-09	.0005	13.6935
	13	-.2837-10	.1345-09	.1375-09	.0005	11.9097
	14	-.4053-10	.1338-09	.1398-09	.0005	16.8484
	15	-.4687-10	.1425-09	.1500-09	.0006	18.2052
	16	-.6385-10	.1420-09	.1557-09	.0006	24.2057
	17	-.6526-10	.1470-09	.1609-09	.0006	23.9321
	18	-.7307-10	.1522-09	.1688-09	.0007	25.6485
	19	-.8490-10	.1493-09	.1717-09	.0007	29.6283
	20	-.9223-10	.1521-09	.1778-09	.0007	31.2367

Table 5. Summary of MSINC Run Data:
PMOS Correlator with Complementary Operation (PCWCO)

"PCWCO" Run No.	Differential Output				Single-Ended Output			
Item	4–3	4–5	4–6	4–2	4–3	4–5	4–6	4–2
Absolute Currents (na.) Drain Freq.	.0236	370.1	.1388	.1340	1757	1411	1899	2572
Gate Freq.	.7467	.8176	160.8	.4553	.9232	1.003	151.9	.5362
(Gate - Drain) Freq.(Desired Signal)	48.40	50.88	45.04	39.66	45.24	47.55	45.58	36.77
(Twice Drain) Freq.	.0312	2.292	.1652	.0233	26.95	29.91	3.922	20.63
(Gate - Twice Drain) Freq.	.3145	.3779	.8035	.1490	.6451	.7224	6.433	.2552
Distortion Rejection (dB): Drain Freq.*	66.3	-17.2	50.2	49.4	-31.8	-29.4	-32.4	-36.9
Gate Freq. * †	36.2	35.9	-11.1	38.8	33.8	33.5	-10.4	36.7
(Twice Drain) Freq.	63.8	26.9	48.7	64.6	4.5	4.0	21.3	5.0
(Gate - Twice Drain) Freq.	43.7	42.6	35.0	48.5	36.2	36.4	17.0	43.2
Power (mW): Drain Buffer	3.026	3.026	2.914	6.655				
Gate Buffer	2.582	2.582	2.582	4.740				
Total	5.608	5.608	5.496	11.395				
Loading: g_{m14} (micromhos)	245.8	245.8	243.3	325.9				
g_{DS4}(micromhos)	22.8	17.5	25.3	35.9				
Ratio: $(g_{m14} \div g_{DS4}) = \lambda$	11.1	14.1	9.6	9.1				
g_{m1} (micromhos)	32.3	32.3	32.3	39.5				
Multiplier Drives: V_{DS4} (mV)	0	0	137.6	0				
V_{GS4} (V)	4.322	4.322	4.335	5.276				
V_{SB4} (V)	4.462	4.462	4.450	5.404				
AC Signals: V_{ds4} (mV.)	79.59	80.69	75.16	71.74				
V_{gs4} (mV.)	65.69	65.69	65.69	63.43				
Buffer Gain: Drain (%) = A_D	63.7	64.6	60.1	57.4				
Gate (%) = A_G	52.6	52.6	52.6	50.7				
Multiplier Efficiency: $\frac{\mu a}{V^2}$								
$v\ (f_g - f_D) \div (V_{ds4} \times V_{gs4})$	9.26	9.60	9.12	8.72				

Run No. Key:
PCWCO–4–3: Perfect Uniform Array, No Offsets.
PCWCO–4–5: An Offset (0.25 V) Multiplier Threshold (or Floating Clock/Gate Buffer)
PCWCO–4–6: An Offset (0.25 V) Floating Clock/Drain Buffer
PCWCO–4–2: No Offsets; Higher Voltage Operation

* Distortion Rejection Values Prior to Four-Quadrant Sequential Multiplication Operation.

† This Model Circuit Makes no Provision for Gate-Frequency Cancellation.

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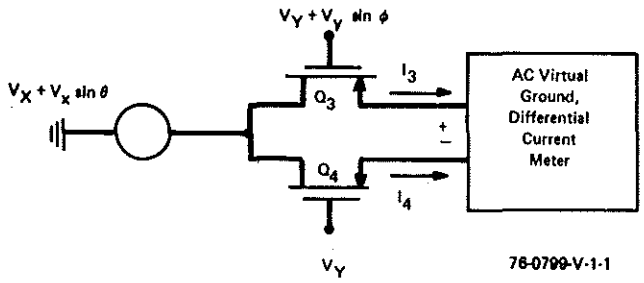

Figure 1. Conceptual Multiplier Circuit

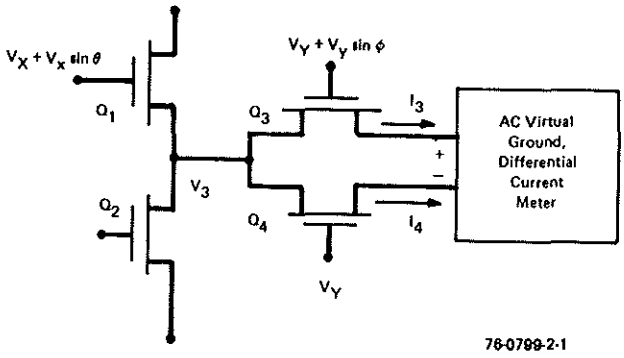

Figure 2. Drain-Buffer Multiplier Circuit

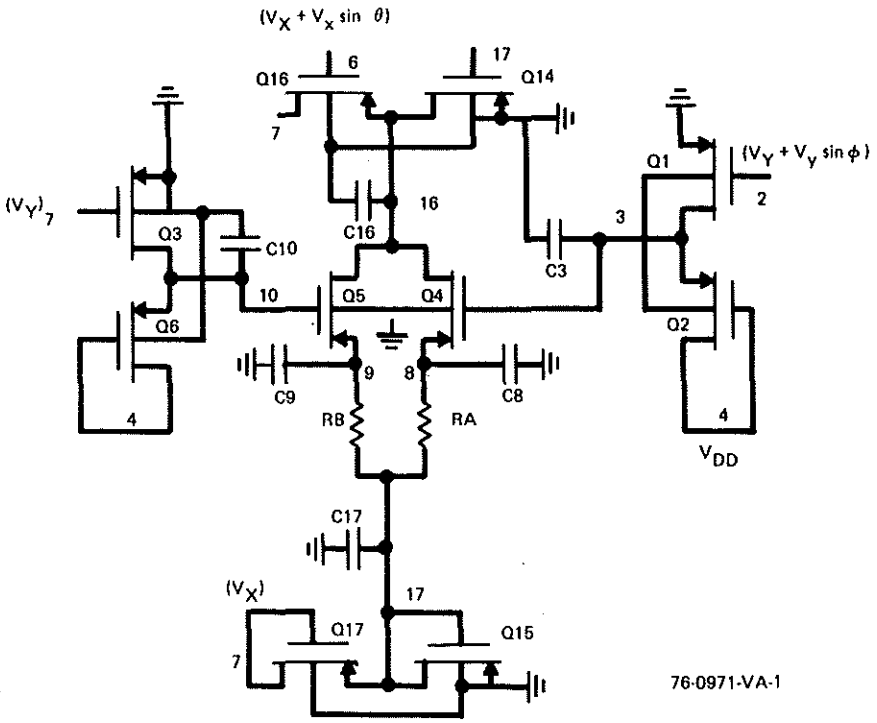

Figure 3. CAD Modeling Circuit for Fully Buffered Multiplier

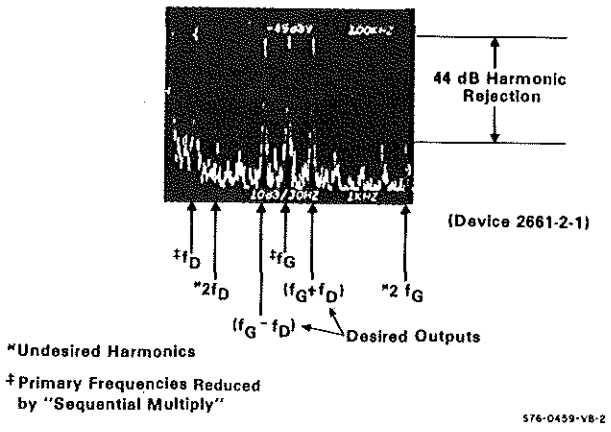

Figure 4. MOS Analog Multiplier Output