A CCD MEMORY FOR RADAR SIGNAL PROCESSING

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ABSTRACT

The results of an Air Force Avionics Laboratory program to develop a CCD digital memory device are discussed. Chip design and performance characteristics are given and compared with other known CCD devices. The use of the 16K bit CCD memory for radar signal processing is discussed and a specific system example is shown. CCD memory cost is projected and compared with other leading semiconductor memory approaches.

INTRODUCTION

The Air Force has a significant number of applications for 10^6 to 10^8 bit memories which do not require non-volatile operation. Among these are synthetic aperture radar processors, scan converters, radar change detectors, high speed swapping discs in communications systems, and buffer memories for video sensor bandwidth compression. In 1972 the Air Force Avionics Laboratory initiated a program with Fairchild Camera and Instrument Co. (Ref 1.) to develop a low-cost general purpose digital CCD memory chip that would offer significant cost and performance advantages for such systems. That program has now concluded with the demonstration of a 16K bit device and the partial development of a 32K bit device, both of which have potential application in military and commercial systems.

DISCUSSION OF CHIP DESIGNS

The Fairchild devices employ a novel memory organization to achieve fast access time along with low power dissipation. This organization is known as the Line-Addressable Random Access Memory (LARAM) approach. (Fig. 1) As implemented with a 1-1/2 phase CCD structure, this organization achieves bit densities comparable to either the serpentine or SPS types while reducing chip access time and clock load capacitance by an order of magnitude. The principle of operation involves clocking a string of bits into a selected register via a common input bus. The clocks are then halted and the information stored in a static fashion as in an MOS RAM type device. As long as the memory returns to this register before the leakage charge exceeds the unity threshold, any other register may be selected at random and undergo a READ, WRITE, or RESTORE operation. When the original register is again selected, the information is clocked out, sensed, and either recirculated or replaced with new data as appropriate. The key to obtaining a compact chip layout is the 1-1/2 phase CCD structure, which permits the single selectable clock line to run the entire length of each register.

16K BIT CHIP DESIGN

A block diagram of the 16K chip is shown in Fig. 2. The chip is organized as four parallel sections of 4K bits each. Each section has its own data input and output pin. A decoder for each section selects one of the thirty-two registers in that section, resulting in only four registers being clocked on the chip at any one time. The active power dissipation is thus reduced, allowing clock drivers on the chip itself, resulting in a simpler device to the memory user. On-chip control logic can switch the chip into either a WRITE mode,

an NDRO READ mode, a R/M/W mode, or a data REFRESH mode. In the REFRESH mode the data is recirculated on-chip with the I/O circuits powered down.

Data rate is variable from 400 KHz to 5 MHz except in the R/M/W mode where the maximum data rate is 3 MHz. Data can be read successively into the same register or into adjacent registers with no loss of speed, although power dissipation will be higher in the latter mode due to the higher duty cycle of the address circuits. Data rate is continuous in all chip modes and all addressing patterns. Access time to a random register is 200 nanoseconds. The average access time is 12.8 microseconds, and the maximum access time to a random bit is 25.6 microseconds.

A picture of the chip is shown in Fig. 3. The chip is 201 by 219 mils, and is packaged in a standard 22 pin dual-in-line package. The chip dissipates 200 mW at a 5 MHz data rate, and less than 50 mW in the REFRESH mode. Only one 12V clock is required, which has a 200 pF capacitance load. All pins except the 12V clock are fully TTL compatible with no pull-up resistors required. The device has tristate outputs to facilitate paralleling the chips in a memory system.

32K BIT CHIP DESIGN

A block diagram of the 32K bit device is shown in Fig.4. The device is identical in design and operation to the 16K bit device, except that it has only one input pin and one output pin for the entire chip. This is achieved by means of an additional on-chip decoding circuit which selects one of the eight simultaneously clocked registers for routing to the output buffer. The other seven registers are automatically recirculated on-chip. A picture of the device is shown in Fig. 5. The entire chip is 240 X 240 mils, and is packaged in an 18 pin ceramic DIP with 0.4 mil pin spacing. Clock capacitance is only 200 pF for a single clock line.

CHIP CONSTRUCTION FEATURES

Both devices share the same CCD structure , sub-circuit designs, and fabrication sequence as the Fairchild 9K CCD memory already on the market (CCD450). The CCD registers are two-phase n-channel buried channel structures with overlapping polysilicon gates. A dual nitride-oxide gate dielectric is used, which places all gate electrodes on the same level of gate dielectric. Ion implantation through the first level polysilicon CCD electrodes generates the required asymmetry for two-phase operation. Dielectric isolation is used in the MOS support circuits to obtain higher packing density. The fabrication sequence requires nine photomasks, of which only two involve critical mask alignments.

Sub-circuits common to both devices include level shifters, decoders, line drivers, sense amplifiers, control logic, and I/O circuits. A dual differential sense amplifier is used as in the TI 4K RAM, with slight modification for sensing charge rather than current. Amplifier sensitivity is further increased by a novel capacitance decoupling circuit, which reduces the loading of the CCD outputs on the amplifier input node. The sense amplifier compares the charge levels in the selected register with a reference level in a dummy register located in each memory subsection. Since the reference level can be adjusted by geometric factors, threshold voltage tracking is achieved without the need for dedicated circuits. This feature, plus conservative design rules, permits wide operating margins and a higher device yield.

The present status of 16K chip development is characterized by the capability to produce small numbers (>100) of fully working prototypes at occasionally excellent yields (>30%). A large number of additional devices are fully functional except for one line or one section, indicating that further yield improvement is possible. Dark current is still a problem and, if not corrected, could restrict the temperature range to less than 50°C. Experiments with variations in process steps show promise for reducing the number of dark current spikes as well as the residual level of leakage charge, indicating that a temperature range of 0°C to 50°C may still be possible. Device modification and yield improvement is continuing under an AFML contract (Ref.2) as well as under company produce development funds. Sample quantities should become available to users by the early fall of 1975, with limited production quantities available approximately six months later. The device is expected to be competitive in a sizeable commercial market.

The development of the 32K bit device lags the 16K device by approximately six months. This is attributable to the greater complexity of the device, the tighter design rules, and larger chip size involved. It is possible that this device will be made available commercially also, although market volume maybe higher for the 16K device.

COMPETING 16K BIT DEVICES

Two other 16K bit CCD memory devices have been announced to date, the Intel 2416 device and the Bell Northern CC16M1 device. The Intel device is available commercially whereas the BNR device is basically a developmental prototype. However, both devices have characteristic features which can be contrasted with the 16K LARAM device.

INTEL 2416

A block diagram of the Intel CCD is shown in Fig. 6. The chip is organized into blocks of 256 bits which communicate with a single set of I/O pins through a 1 of 64 decoder, giving the chip a one bit swath. The decoder operates like a 64 bit RAM which transfers one bit at a time from each of the 256 bit registers. On-chip control logic determines whether the chip is in a NDRO READ, WRITE, R/M/W, or standby SHIFT cycle. Cycle time for the RAM decoder is 460 ns. for a READ or WRITE cycle and 620 ns. for a R/M/W cycle. Random access time for the READ cycle is 250 ns. to the first bit of a block. The minimum shift cycle period is 750 ns. This gives a maximum chip access time of less than 200 microseconds to any random bit, and a maximum internal shift rate of 1.33 MHz in the search mode.

The decoder can be used to read consecutive bits out of the same 256 bit block or consecutive bits out of successive adjacent registers. The first alternative requires one RAM cycle and one SHIFT cycle for each bit transferred, limiting the maximum data rate to 800 KHz for the READ and WRITE modes or 730 KHz for the R/M/W mode. The second alternative permits a higher 2 MHz data rate for the READ and WRITE mode and a 1.33 MHz rate for the R/M/W cycle; however, in this case the data rate is not continuous because each time the RAM is completely loaded, a SHIFT operation must take place to transfer the data to the CCD registers. Minimum refresh considerations require further that a SHIFT operation occur at least every 16 RAM cycles at 70°C.

A picture of the chip is shown in Fig. 7. It is 143 X 237 mils long and is packaged in a standard 18 pin plastic DIP. The device has four 12 to 14V clock inputs, two with a 500 pF load capacitance and two with a 700 pF load capacitance. Total power dissipation is 600 mW at 1 MHz, which decreases to 150 mW in the 125 KHz standby SHIFT mode. Chip I/O lines are TTL compatible, although pull-up resistors are required. The chip inverts data from input to output.

BELL NORTHERN CC16M1

The BNR device (Fig. 8) is organized as four parallel registers of 4K bits each, with separate data input and output pins for each 4K block. Each block consists of two parallel SPS registers of 2K bits each which operate in a push-pull fashion. The SPS registers have a 16 bit input register and 32 parallel 64 bit registers half of which are loaded on alternate clock phases. The data rate at each I/O pin is 1 to 10 MHz, which implies an average access time of 0.2 to 2.0 milliseconds for each 4K block. The chip dissipates only 325 mW at a 10 MHz data rate and only 85 mW at a 1 MHz rate.

The chip generates all its own internal clocks and timing from a single 2-phase clock input. Clock swing is 0-12V and capacitive loading is only 60 pF on each clock line. On-chip control logic switches the chip to either a WRITE, R/M/W, NDRO READ, or an on-chip RECIRCULATE mode. Data and control lines are fully TTL compatible, with no pull-up resistors required. Chip size is only 137 by 170 mils. The device is packaged in a standard 16 pin DIP.

COMPARISON OF 16K DEVICES

A comparison of the three 16K devices is shown in Table 1. The widely ranging characteristics reflect the fact that the devices are directed at different market objectives. The Intel device is directed primarily at the head-per-track disk and drum market, where its faster access time should yield significant system advantages. The Bell Northern device is directed mainly at the MOS shift register market, where it can be used in CRT refresh, terminal storage and communications buffering type

applications. The Fairchild device is intended to be a general-purpose shift register type of device which will compete in both of the memory areas cited, but whose unique accessing capabilities might allow the exploitation of new memory system architectures.

Selection of the appropriate device depends strongly on the type of system contemplated. In a computer-type memory system, only a single bit, word, or block of information is accessed at any given time. The primary measure of memory performance is how fast the data can be made available to the CPU. Since only a small fraction of the system is active at any given time, standby power is the dominant feature. The larger the memory becomes, the more standby power must be emphasized.

For a serial buffer or signal processing type of system the primary measure of memory performance is the data transfer rate. Random accessability is not a major advantage since the data sequence is rarely re-ordered. Most importantly, the fraction of devices active at any time is usually quite high, making the active device power the dominant factor. This is especially true in serial signal processing systems, where all devices might be active at any given time.

Fig. 9 plots the total power dissipation versus serial data rate for some candidate serial devices. The standby power is seen to be quite similar for all the devices, reflecting the fact that leakage mechanisms are similar for these NMOS type devices. At clock frequencies near one megahertz, however, the power dissipation differs greatly, reflecting differences in chip organization and in the ratio of capacitive loading to DC loading per bit. Clearly, the power savings can be substantial for large serial data systems if the new CCD memories are used.

Keeping these comparisons in mind the BNR device would likely be preferred for shift-register memory applications due to its high data rate, low power dissipation, small package size, wide temperature range, ability to string registers, and potential for low chip cost (ie. small chip size and standardized process). The Fairchild device would rank a close second with its more complicated overhead requirements, smaller temperature range, larger package size, and more complex fabrication process. The Intel device would rank a distant third, with a heavy penalty attached to its discontinuous data rate, single bit swath, data inversion, and increased overhead requirements. Cost considerations based on volume sales capability could influence the preference somewhat if low system cost is a primary objective.

A different order of ranking results if a disk-type memory system is considered. Here, the Intel device is most highly preferred for its fast access time, single bit swath, short time to refresh, small package size, higher temperature range, and lower cost potential. The Fairchild device compares favorably, but is penalized somewhat for its four bit swath, lower temperature range, more complicated fabrication process, and either a long or an unconventional refresh cycle. The BNR device ranks third for its slow access time and long time to refresh. All three devices can be improved somewhat for a disk-type memory application through simple design modifications. Such modifications might include the sharing of a common I/O pin, decoding on-chip for a single bit swath, and in general, simplifying the chip interface requirements.

APPLICATION OF CCD's TO RADAR SIGNAL PROCESSING

Synthetic aperture radar systems are notorious for the digital memory capacities they require. A block diagram of a typical system is shown in Fig. 10. Essentially, the system collects high frequency radar returns at a low duty cycle, stretches them to achieve a lower bandwidth at a continuous duty cycle, filters the data to extract the imaging information, and presents the information to a display or recorder. Two memories are generally required, one in the processor and one with the display. With high resolution systems, these memories can reach capacities of 10^6 to 10^8 bits or more.

Figs. 11 and 12 show the detailed memory organization for a particular SAR processor known as Synthetic Aperture Precision Processor High Reliability (SAPPHIRE). This processor is currently being developed by Goodyear Aerospace Corporation under ASD/AFAL

sponsorship. (Ref 3.) The small rectangles in Fig. 12 represent 1 Kbit blocks of data. Each block stores data from consecutive radar returns and presents it to the complex multipliers sixteen returns at a time. In the accessible memory, each block receives new data every sixteenth return in an interleaved pattern. The entire memory is 23.6 megabits in size and dissipates 2350 watts.

Fig. 13 shows how the Fairchild 16K CCD can be used to replace the Intel 2401 2K bit shift register in the accessible portion of the SAPPHIRE memory. Since the non-accessible portion is purely serial storage, direct CCD substitution is a straightforward matter. The entire memory is therefore replaceable with CCD storage with no re-organization required. It is expected that the CCD version will dissipate one tenth the power, occupy 1/3 to 1/4 the volume, and weigh 1/2 to 1/3 as much as the present MOS shift register version. In production, it should cost 1/3 to 1/4 as much as the MOS unit.

COST POTENTIAL OF CCD MEMORY

The cost of CCD memory is bounded by the cost of MOS RAM's to less than 0.1 cents per bit. It is expected that CCD's can achieve even lower costs because roughly four times as many bits can be placed on the same size chip using the same process and design rules.

The projected cost of CCD memory is shown in Fig. 14. This projection by an independent consulting firm agrees closely with estimates from potential CCD manufacturers and large volume memory users. Table II presents a second independent assessment of CCD memory market size. It is still too early to tell whether CCD's will fulfill these optimistic predictions, but the potential is definitely there. Actual system experience will provide the answer over the next two to three years.

The following individuals and companies are acknowledged for their discussions of the status of CCD technology and for furnishing detailed descriptions of device operation: Gordon Moore and Sun-lin Chow of Intel Corp.; Mark Guidry, Gil Amelio, Henry Pao, and Kamil Gunsagar of Fairchild; and Doug Colton, Bill Coderre, and Neil Waterhouse of Bell Northern. Thanks also go to J. Decaire for a critical reading of the manuscript and to Mrs. Penny Carpenter for typing the final version.

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2. Contract F33615-74-C-5088, entitled "Manufacturing Method on Charge-Coupled Device (CCD) Memory Arrays", May 1974 to May 1976.

3. Contract F33657-74-C-0604, entitled "Synthetic Aperture Precision Processor High Reliability (SAPPHIRE), July 1974 to December 1975.

4. Quantum Science Corp., in Electronic Design 22, October 25, 1974, p. 43.

5. H.C. Wainright & Co., in Electronic News, February 5, 1975.

TABLE 1. COMPARISON OF 16K CCD MEMORY CHIPS

CHARACTERISTICS	FAIRCHILD CD460	INTEL 2416	BNR CC16M1
Organization (Swath/select/block size)	4/random/128	1/random/256	4/serial/4K
Operating modes	R,W,R/M/W,RECIRC	R,W,R/M/W,SHIFT	R,W,R/M/W,RECIRC
On-Chip recirculate	YES	YES	YES
Off-Chip recirculate	R/M/W (latch Req'd)	NO	YES
Required power supplies	+125V, +5V, -5V	+12V, -5V	+12V. +5V, -5V
Clock voltages	12V	12V	12V
Clock phases	2	4	2
Clock capacitance	120pF, 15pF	2 @ 500pF 2 @ 700pF	2 @ 60pF
Clock rep rate	0.5 to 5.0 MHz	0.1 to 1.3 MHz	0.5 to 5.0 MHz
Data transfer rate (per pin)	0.5 to 5.0 MHz	0.2 to 2.0 MHz*	1.0 to 10 MHz
Worst case access time	25.6µs	192µs	0.4ms
Average access time	12.8µs	96µs	0.2ms
Time to refresh	0.8ms	49µs	0.4ms
No. refresh clock cycles	4096	64**	2048
Temperature range	0°C to 55°C	0°C to 70°C	0°C to 70°C
Chip power (max)	200mW @ 5 MHz	300mW @ 2 MHz	325mW @ 10 MHz
Standby power	50mW	24mW	85mW @ 1 MHz
Output structure	Tri-state TTL Compatible	Open drain Pull-up resistor req'd	Tri-state TTL Compatible
Chip size	219 X 201	237 X 144	137 X 170
Package size	22 pin ceramic	18 pin plastic	16 pin ceramic
Process	ISO-NMOS(BC)	NMOS(SC)	NMOS(SC)
Start-up clear req'ts	8192 cycles	4096 cycles	43 cycles
Unique features	--	inverts data	--

* The data rate is interrupted every 16 cycles for a SHIFT operation.

** 128 cycles are required to restore the addresses to their initial state.

TABLE 2. MEMORY MARKET *

	1973		1978	
	Qnty. (Bill. Bits)	Value (Millions)	Qnty. (Bill. Bits)	Value (Millions)
Semiconductor				
Bipolar	16	$250	80	$ 500
MOS	45	208	280	565
SOS	--	2	15	65
CCD	--	--	60	45
TOTAL	61	460	435	1,175
Magnetic				
Core	62	280	50	135
Plated Wire	8	135	15	155
Buble	--	--	10	20
TOTAL	70	415	75	310
Other	5	95	5	65
TOTAL	136	$970	515	$1,550

Note: Total market, including captive production

*Source: Ref. 5

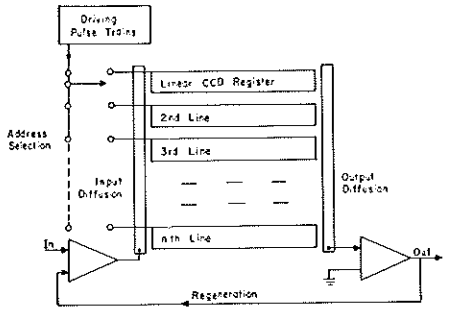

Fig.1. LARAM principle.

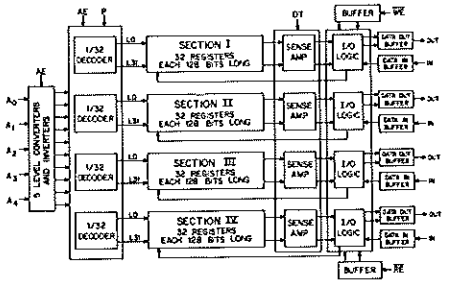

Fig.2. CCD460 block diagram.

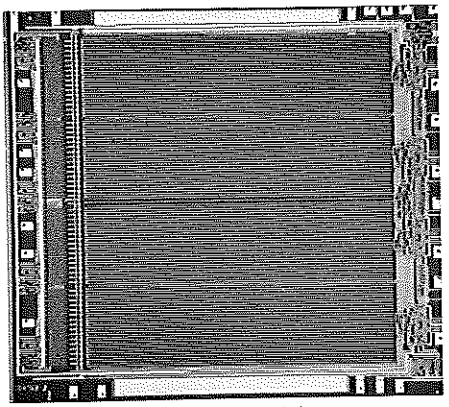

Fig.3. CCD460 chip.

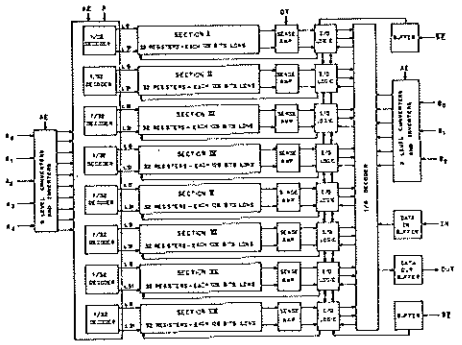

Fig.4. 32K block diagram.

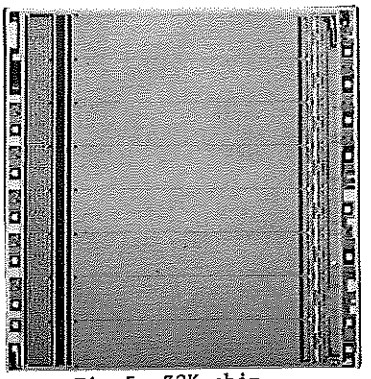

Fig.5. 32K chip.

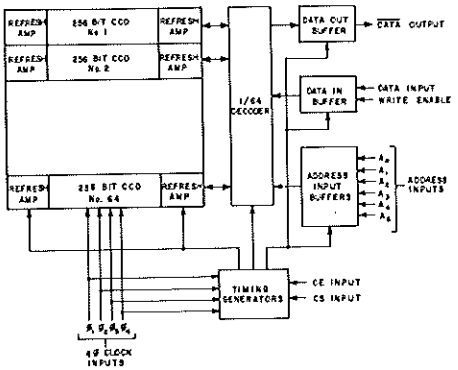

Fig.6. Intel 2416 block diagram.

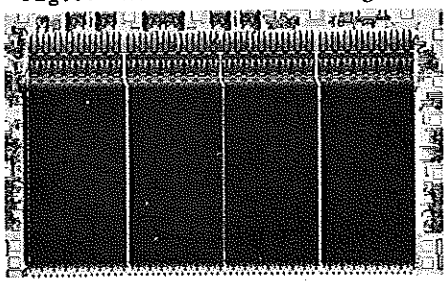

Fig.7. Intel 2416 chip.

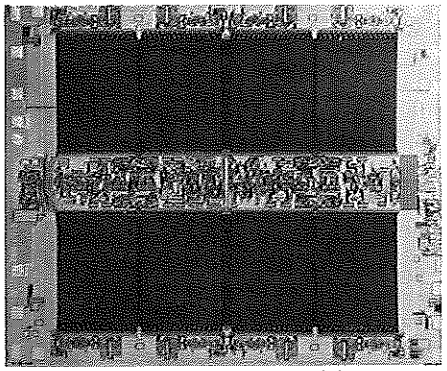

Fig.8. BNR CC16M1 chip.

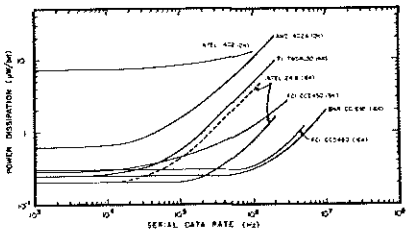

Fig.9. Active power vs. data rate.

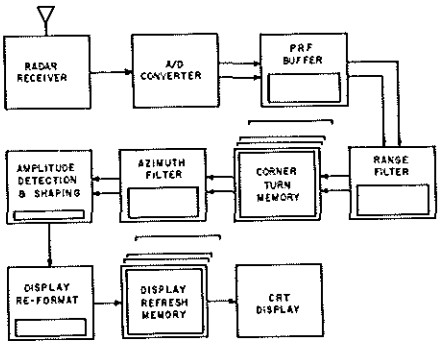

Fig.10. Typical SAR block diagram.

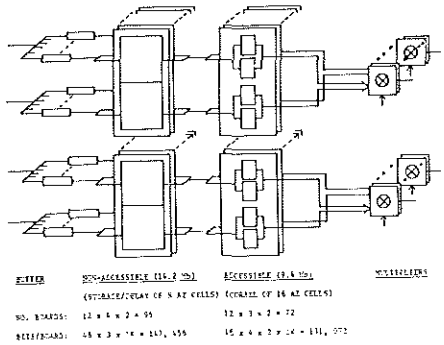

Fig.11. SAPPHIRE memory organization.

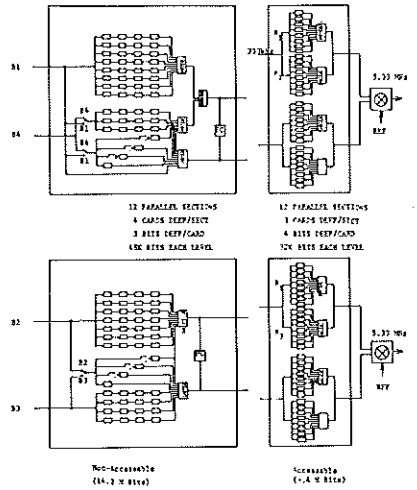

Fig.12. SAPPHIRE circuit boards.

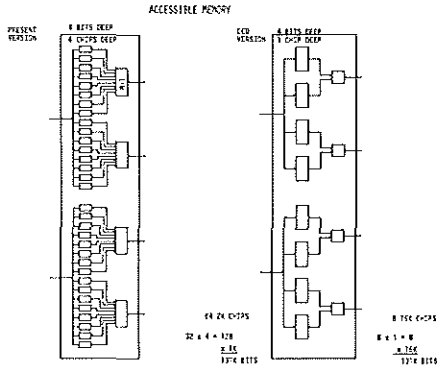

Fig.13. CCD vs. MOS version.

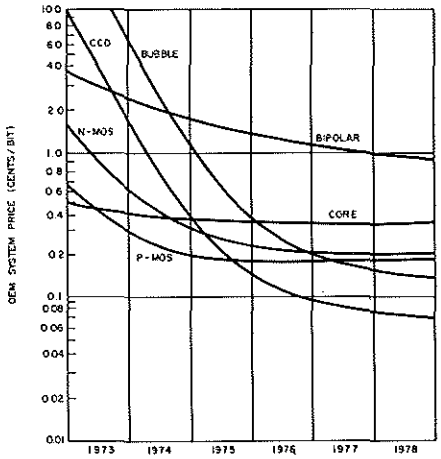

Fig.14. Projected CCD cost.