HIGH SPEED OPERATION OF CCD's*

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ABSTRACT CCD's require a complex array of peripheral circuitry to support their operation in most applications. This includes input gating, multiple-phase clock signals and output gating, all synchronously functioning. Buried channel and peristaltic CCD's which can approach or attain VHF rates of operation require very sophisticated supporting circuits to fully realize their capabilities. Such circuits are in many cases not off-the-shelf items which can be independently selected. Good RF circuit techniques must be used in designing and combining circuits along with a thorough knowledge of CCD input and output parameters, to effectively develop a CCD analog system. This paper presents the development of peripheral circuitry for an analog CCD application at 62.5 Msamples/second. Unique aspects of input, output, and propagation gate drive circuits are considered both in terms of the CCD and its host system. The overall system application as a transient data recorder[7] and the specific device development[8], which was subcontracted to Rockwell International by GARD, are presented in separate papers at this conference.

INTRODUCTION

CCD analog shift registers are used for both delaying and expanding the time base of quantized analog data. The functional system required for either application is shown in Figure 1. A constant clocking rate provides a continuous quantizing of data with a constant delay. The time base of high speed data is expanded by reducing the clock rate after the data is loaded. The degree of expansion is proportional to the reduction in clock frequency. The operational requirements of the CCD peripheral elements in Figure 1 are the same with the possible exception of speed and bandwidth. The system described in this paper operates in the time base expansion mode with 62.5 Msample/second input rate and 100 Ksample/second output rate using a 128 cell peristaltic device. The discussion of the CCD supporting circuitry is divided into the three areas designated in Figure 1, namely, input, drive, and output sections.

INPUT

The high possible shifting rate and large dynamic ranges of various CCD's demands extremely high performance input techniques if the full capability of the devices are to be realized within a system. The state of the art in sampling techniques might well have to be advanced to meet these requirements. In a sampled data system, the aperture time requirement is a function of the maximum analog signal frequency and the resolution or accuracy desired. Sampling circuits with aperture times of well below one nanosecond and repetition rates approaching 100 MHz are needed. Several input approaches are discussed and compared below, followed by a description of a track and hold sampling circuit which has been developed and is compatible with the gate input methods.

INPUT TECHNIQUES

Potential Equilibrium Input

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The potential equilibrium or fill and spill input technique has been shown to be a linear and low-noise method of applying input data to a CCD[1,2]. It involves generating a potential well under an input gate, flooding it with charge and allowing the excess charge to spill back over the potential barrier of the adjacent gate. After the charge spilling process is completed, the measured charge packet is ready for transfer down the channel. The charge flooding can be achieved by a current pulse applied to the input diffusion. A major advantage of this method is that the measured charge quantity is independent of the exact nature of this diffusion pulse and is determined solely by the two input gate voltages. A disadvantage is that the charge spilling process requires a finite amount of time which increases with high accuracy requirements and thus places a frequency limitation and/or stringent timing requirement on the device clocking. This method is also susceptible to noise and interference components coupled to the input gates during the charge spilling period. These effects may be reduced, however, if the common mode rejection of the two input gates is significant and properly utilized in the input circuit design.

For high-speed high-resolution applications, a sample and hold circuit is required to reduce the aperture error to an acceptable level. The generation of the input diffusion current pulse must be sufficiently controlled within limits to insure adequate forward charge flow. Using standard fast ECL logic elements and high speed switching transistors, pulses with rise times and timing accuracies approaching one nanosecond have been constructed and proved adequate for generating input diffusion waveforms.

Gated Charge Input

A second input technique is the gated charge method, where the channel transconductance below the input gate is simply varied to regulate charge flow, which accumulates for each charge packet. This method is much simpler and faster, but it has been shown to be less linear than the first method. Unlike the first method, the input charge packets are a function of the input diffusion current amplitude and duration. This puts a much tighter control requirement on the input diffusion pulse waveform. In fact, the precision of the diffusion pulse generation must exceed the overall system accuracy requirement.

If the input current pulse width used is greater than the desired aperture time of the system, then a sample and hold circuit must be used. This method should be less susceptible to higher frequency noise and interference coupled to the input gate, since the input signal is effectively integrated over the input current pulse period. However, no common mode rejection is available with the single gate structure.

Direct Sampling Input

A third input approach is direct sampling of the analog signal on the CCD. To do this, the input structure must respond to pulse widths equal to or narrower than the desired aperture time. If this constraint is met, then in a manner similar to the second method, the analog signal can be applied to the input gate which controls the channel conductance during the diffusion pulse, which is now much shorter. Another version of this technique is to generate the narrow sampling pulse by gating the input current with a second input gate preceeding the input signal gate.

This method is susceptible to coupled interference and noise on the signal gate for a much shorter period than the first two methods. In addition, since it requires no sample and hold circuit ahead of it, a lower impedance is more easily presented to the gate. This reduces the effects of stray capacitive coupling which can introduce interference and noise to the signal path. The narrower input pulse required with this method is more difficult to generate and may require different circuit devices and design techniques, such as step recovery diodes and use of transmission line techniques.

TRACK AND HOLD

A track and hold circuit has been developed which provides voltage sampling of an analog signal with an aperture error on the order of 100 picoseconds, and thus holding quantization error to 2^{-6} at 100 MHz. This circuit provides a constant voltage

level to the CCD for a large portion of its sampling period. Thus the CCD can be accurately loaded with the correct input sample as long as the appropriate CCD clocking occurs sometime during the "hold period" of the track and hold circuit. This increased CCD clock timing margin is quite significant in view of the very high current propagation gate signals which must be generated. This circuit also provides some degree of buffering between the analog signal path and the CCD.

Description

Figure 2 shows the basic sections of the circuit. The sampling gate consists of four matched Schottky diodes as shown in Figure 3. A balanced drive is provided to switch the bridge on and off, thereby allowing the hold capacitance voltage to track the input signal or hold the signal voltage level existing at the instant of turn-off. This arrangement provides the very small aperture time desired (less than 100 picoseconds). The clock balun section presents a balanced drive waveform to the diode bridge and performs an impedance transformation to provide proper voltage and current levels to the bridge. The degree of waveform balance achieved is very critical to the accuracy of the circuit. Two toroidal wound transmission line transformers are connected in tandem to maximize drive waveform symmetry. The low impedance signal source consists of a precision wideband attenuator which provides the following three functions: 1) reduces signal levels down to those compatible with track and hold CCD requirements, 2) isolates the signal source and signal line from the transients which the diode switching generates, and 3) provides a reduced driving impedance to the hold capacitance which enables faster charging. The input impedance of the attenuator can be adjusted to a nominal level such as 50 ohms which can then easily be connected to the signal source with 50 ohm transmission line. The output load impedance is limited to some value of capacitance which is chosen on the basis of slewing, tracking, and hold voltage droop requirements of the circuit. This constraint makes the connection to the track and hold circuit to the CCD rather inflexible if the desired hold capacitance is low. A physically short connection minimizes stray shunt capacitance and decreases noise and interference pickup.

Design Considerations

The wideband response and common mode rejection of toroidal wound transmission line transformers make them excellent devices for generating the balanced bridge drive[3]. Good squarewave response with rise times well below 1 nanosecond are possible if proper resistive loading is provided. Any degree of unbalance in the drive to the bridge results in an output error as the bridge is turned off. Minimum common mode output from the transformer is desired for all frequency components contained in the clocking waveform. Two transformers are used in tandem to further increase the degree of output balance. The degraded common mode rejection of these transformers at higher frequencies due to winding dissymmetries may be improved somewhat by adding a small trimming capacitance to one side of the transformer output. Care must be taken to avoid presenting excessive reactive loads to the transformers, since this causes output ringing which adds to output error or increases settling time.

A first order analysis of the hold capacitance charging phenomenon has been performed for the model in Figure 3. Assume that the balanced bridge drive is a gated constant current, the input isgnal is a constant voltage, and the four diodes are perfectly matched and conform to the standard diode V-I relation[4]. If the output voltage is initially zero, it is then constrained by the following equation after the drive current is applied.

$$(1)\quad Vo + R_g C_h \frac{dVo}{dt} = V_g - .026 \frac{I + C_h \frac{dVo}{dt}}{I - C_h \frac{dVo}{dt}}$$

where V_g - signal voltage
R_g = signal source resistance
C_h = hold capacitance
I = bridge driving current
Vo = output voltage

The exact solution to this equation is difficult; however, it can be solved approximately

in three segments as shown in Figure 4. Equation (1) can be linearized and then solved yielding the following expression.

$$(2)\quad Vo = (V_g - V_B)\exp\left[\frac{-(t - t_B)}{(R_g + .052/I)C_h}\right]$$

This solution is increasingly accurate as the charging current, i_o, decreases. It is, therefore, used to describe the final portion of the charging curve, segment BF in Figure 4. Point B is defined as the time when the solution reaches an accuracy of 95%. This can be shown to be when i_o decreases to 0.39 I.

During the initial charging process, only two of the bridge diodes are conducting and essentially all of the drive current is flowing into the capacitor. The voltage is, therefore, described by equation (3).

$$(3)\quad Vo = \frac{I}{C_h}\,t$$

This expression defines segment OA of Figure 4. Point A is defined as the instant where i_o decreases to 0.95 I. Segment AB is linear connection of the two points where its slope is taken to be the arithmetic means of the adjoining segment slopes. Equation (4) describes segment AB.

$$(4)\quad Vo = V_A + \frac{V_g - V_B}{2(R_g + .052/I)\,C_h}(t - t_A)$$

This approximation is justified by verifying that $V_B - V_A$ is a very small fraction of V_g for typical parameter values. Using equations (2), (3), and (4), it is possible to determine the final output voltage V_F and hence the charging error for a given set of operating parameters.

Matching of the four Schottky diodes is critical to the accuracy of circuit. DC matching provides minimum offset error and best temperature tracking of the diodes. AC matching is required to maintain good common mode rejection of the clocking signal as the bridge is turning off. Diode leakage is critical in determining the droop characteristics of the circuit. Fast slewing and charging rates require a very small hold capacitance which in turn is susceptible to voltage droop. Since balanced leakage currents cannot be maintained under all operating conditions, worst case leakage at the maximum operating temperature should be considered.

The small value of the hold capacitance can lead to another problem. When the bridge is reverse biased, the signal source is still coupled to the output through the capacitance of the diodes. This results in a slight variation of the hold voltage as the input signal continues to change. This problem is reduced by increasing the hold capacitance and minimizing the diode capacitance. A neutralizing technique can also be employed which involves coupling a small controlled amount of inverted signal to the output to cancel the inherently fed through signal.

The signal attenuator can provide the lowest output impedance when a simple "L" section configuration is used. In general, increasing the amount of attenuation will decrease the output impedance which provides faster slewing, reduced charging error and faster transient recovery. It will also reduce the input VSWR and the switching transient levels resulting at the input. The input attenuator should be constructed with resistors which have good high frequency characteristics. Metal film resistors with minimum lead length or chip resistors are desirable.

Circuit layout techniques including component placement and connection methods greatly affect the operation of the entire circuit. Maintaining a symmetric configuration wherever possible helps maintain clocking balance and minimize common mode error. Stray capacitances, such as signal feed-through coupling, should be minimized. Minimum lead length and microstrip connections tend to reduce transformer ringing. High quality printed circuit board material with low dielectric loss characteristics up through microwave frequencies is desirable. Shielding techniques can be used to reduce stray coupling and susceptibility to interference. Track and hold circuits have been constructed which sample signal bandwidths up to 100 MHz at repetition rates in excess of 60 MHz. Thus far accuracies of 3% have been achieved.

Interface

The track and hold circuit developed is intended to drive only a small capacitive load, specifically an input gate shunted with a small capacitance of several picofarads. The bulk of the input gate capacitance for the devices used is due to the bonding pad and package lead capacitance and totals about three picofarads. The stray capacitance of the diode leads and the PC board plating to ground is significant when working at these levels and must be considered in determining the effective value of hold capacitance.

If the signal source impedance is equal to the attenuator input impedance, for example 50 ohms, then a transmission line connection between the two of any length can be made with no effects other than signal delay. If the signal source has an output impedance other than 50 ohms, care should be taken to avoid transient reflections. This can be done by choosing the transmission line length such that the total round trip propagation time from the attenuator to the signat source and back does not equal an integral multiple of the sampling rate period. This will insure that a sampling transient does not reflect back into the attenuator as a succeeding sample is being taken. The source impedance at frequencies well above the signal bandwidth must be considered since the sampling transients contain very high frequency components. If a low-pass filter exists between the signal source and the attenuator, its output impedance must be considered. Most filters have a high VSWR above the cut-off frequencies which means transient reflection errors may be introduced.

DRIVE

The Peristaltic CCD's (PCCD) developed for this application employ a four phase propagation gate structure. A four phase (4-Ø) clock is required to transport charge in the device. Each forward transition is accomplished by dropping the barrier in front of the charge packet and raising the well behind it. The following discussion covers the requirements and considerations regarding the development of the 4-Ø clock/driver system.

4-Ø CLOCK GENERATION

The 4-Ø clock signals required for the CCD's are generated using a pair of D-type Flip Flops connected as shown in Figure 5. When a clock frequency of 4 times the shift rate is applied to this clock generator, the four outputs will produce the waveforms shown in Figure 6. Each $\emptyset_n$ is 1/4 of the incoming clock frequency, and is delayed 1/4 period with respect to $\emptyset_{n-1}$. The logic family used must be consistent with the frequency of operation. To operate at a shift rate of 62.5 MHz, an input clock frequency of 250 MHz is required. The only logic family capable of handling these frequencies is Emitter Coupled Logic (ECL). New entries in the ECL family include D-Flip-Flops capable of toggling at frequencies up to 700 MHz. With this method of four phase generation, the clock frequency can be changed and still retain the quadrature relationship of the four $\emptyset_n$'s. This is important when considering time-expansion operation where two or more frequencies of operation are necessary. Also to be noted here is the fact that $\emptyset_1$ and $\emptyset_3$ are complementary as are $\emptyset_2$ and $\emptyset_4$.

GATE DRIVER CHARACTERISTICS

Gate Driver

Once the gate driver timing signals are generated as above, a driver must be used to provide CCD gate drive of the required amplitude. The load on the driver is primarily capacitive in nature. In order to specify the driver characteristics, it must first be determined what the drive requirements of the CCD are.

Driver Speed

When operating at 62.5 MHz shift rate, the period of the driver waveform is 16 nsec. The optimum waveform is shown in Figure 7. In the figure, T_o = 16 nsec. The transition times, t_r and t_f, must be $T_o/2$, or 8 nsec, maximum. It has been recommended by the device manufacturer that a minimum transition time be 5 nanoseconds. This is to insure that a well collapse (or barrier rise) does not occur so quickly as to spill charge over the channel stops or into adjacent charge packets. The end result of such operation would result in reduced dynamic range and charge transfer efficiency. This minimum

rise time puts an upper limit on the current drive necessary to drive the capacitive gate load.

Current and Voltage Requirements

Considering the waveform of Figure 7, the recommended peak-to-peak swing (V_H-V_L) is in the range of 12 to 15 volts for the devices used. With the high density gate structures, it is necessary to put every other gate on a different level, physically further away from the substrate. In order to compensate for that portion of the field lost in the additional insulating layer, upper gates must have a 15 to 25% greater voltage swing than that for lower gates. The driver design will be based on the larger voltage swing of 15 volts.

The current drive required of the driver is a function of voltage swing, rise/fall time, and the capacitive loading of the drive gates. The gate loading of the devices used at GARD was about 25 pf. The current required for the slewing of the gate voltage is given by:

$$I = C \frac{\Delta V}{\Delta t}$$

where C is the gate capacitance = 25 pf

ΔV = the peak-to-peak swing = 15 volts

Δt = transition time = 6 nsec

The required current is, therefore,:

$$I = 25 \times 10^{-12} \times \frac{15}{6 \times 10^{-9}} = 62.5 \text{ ma.}$$

The additional loading of the transmission path (cable or printed circuit) and stray capacitance could add as much as 10 to 15 pf to the driver load. This will increase the driver current requirement to 100 ma per CCD gate. The driver must be able to source as well as sink this current to provide both rise and fall times in the 6 nsec range.

Delay Stability

The driver must provide an output waveform with a constant delay with respect to the input waveform. This insures that the 4-Ø drive signals at the CCD remain in quadrature over the entire frequency range of interest. For a set of four drivers, the delays should not differ by more than ± 1 nsec. If the stability of each driver is within ± 0.5 nsec over the entire frequency range, any mismatch in the driver delays can be compensated for by using delay lines at the inputs of the drivers.

Transient Response

The transient response of the driver must be such that the clock can be halted, or a frequency change can be made, without having any output abberations which may destroy the barriers separating individual charge packets. This is important in the time expansion application where the input mode is at 62.5 MHz shift rate and the output is at a much lower rate. When the last high frequency clock pulse is received, the drivers will respond by changing two of the phase drive lines. After this change, the outputs should remain in their respective output states until the next clock pulse is received. This requirement prevents the use of tuning out the capacitive CCD gate load to minimize gate drive requirements.

DRIVER DESIGN CONSIDERATIONS

Power and Thermal Calculations

As indicated in an earlier section, the current required to slew the gate is 100 mA. Assume that this current is drawn from a 17 volt power supply and that the rise time takes up 6 out of each 16 nanoseconds. During the fall time, the driver current is sunk to ground, hence only a small amount of power is required. The average power at 62.5 MHz, not considering driver inefficiency, is:

$$P_{avg} = V_{PS} \times I_{peak} \times \text{duty cycle}$$
$$= 17 \times 0.1 \times \frac{6}{16}$$
$$= .637 \text{ watts}$$

The driver, however, will not be 100% efficient. Therefore, driver power of .7 to .8 watts will be required. For four drivers to support a single CCD, the power required will be 3.2 watts at 62.5 MHz. Because the driver is driving a reactive load, very little power is dissipated by the CCD gate;

virtually all of the 3.2 watts is dissipated in the 4-Ø driver circuit. Fortunately, the time expansion mode requires that the drivers be operating at the 62.5 MHz rate less than 10% of the time. The overall average power is, therefore, greatly reduced. The drivers must be designed, however, to withstand peak power of 3.2 watts for periods up to 10 milliseconds.

Physical Layout

The physical layout must take into consideration both the power requirements and the capacitive loading of the driver. The driver should be located as close as possible to the CCD so as to minimize the additional driver loading due to the transmission path. The CCD is sensitive to temperature; so it is important to isolate it from external heat sources.

An increase in chip temperature will increase the dark current (thermal well filling) of the CCD. This is not of great concern at high shift rates since a given charge packet will not be in residence in the chip for a sufficient length of time to be distorted by thermal filling, but a thermal filling at low shift rates can be significant. The driver circuitry, located close to the CCD, must be carefully laid out to avoid excess heat transfer to the CCD.

Circuit Techniques

Commercial MOS drivers with ECL-compatible inputs are available. Such a device is the Texas Instruments SN75368. This device is specified as having a typical transition time of 17 nanoseconds for a 15 volt swing when loaded with 390 pf. The current output to meet this transition time is:

$$I = C\frac{de}{dt} = 390 \times 10^{-12} \times \frac{15}{17 \times 10^{-9}} = 344 \text{ ma.}$$

This current is sufficient to slew a 40 pf load in 6 nsec indicating a more than adequate output stage, but an evaluation of sample devices indicates that the chip is not capable of high frequency operation due to limitations in the input or pre-driver stages.

DISCRET COMPONENT DRIVER IMPLEMENTATION

Since the single-chip CCD driver could not satisfy the stated requirements, a driver will have to be developed with discrete hardware. A block diagram of such a circuit is shown in Figure 8. In evaluation of circuit techniques for its design, the following factors must be considered:

(1) Interfacing with ECL logic levels of the 4-phase generator.

(2) Driver output configuration.

(3) Speed-up techniques.

Each of these will be individually discussed.

ECL Interface

The interface with the ECL logic swing of -0.9 volts to -1.6 volts is not trivial. The logic swing of 0.9 volts is not great enough to reliably switch the base-emitter junction of a bipolar transistor whose emitter is tied to a firm reference voltage. Variance in both the ECL voltage swing as well as transistor forward junction voltage with temperature make this method unreliable.

Commercially available ECL to TTL translators can be used. Such a device as the MC10125 converts ECL levels to TTL levels using a Schottky output stage. Operation at 62.5 MHz, however, is at the maximum limit of this device resulting in a sine wave output which may not achieve the maximum TTL logic swing. Also, the variance in the delay of these devices is not consistent with the driver requirements.

The remaining technique is to use a differential amplifier as the input stage using the center swing voltage of the ECL family (V_{BB}) as the reference input. V_{BB} can be generated with an ECL chip which will track the ECL swing to compensate for temperature variances. The differential transistor input can be purchased in one package. Therefore, the variance in base-emitter junction drop of one will be offset by a similar variance in the other. The resultant input structure will be stable and ECL-compatible at all temperatures.

Driver Output Configuration

At low frequencies, the number of active components can be reduced by using

a single transistor and a passive pull-up resistor to drive the CCD gates. However, to obtain the necessary rise time, the pull-up resistor value (for a time constant of 2 nanoseconds) is:

$$R = \frac{\tau}{C} = \frac{2 \times 10^{-9}}{40 \times 10^{-12}} = 50 \text{ ohms}$$

As a result, the output transistor would not only have to pull down the capacitive load of the CCD, but also the resistive load of the pull-up resistor. This also adds a DC component to the power required by the drivers and contributes to the heat which will be generated in the vicinity of the CCD's.

The only available approach is a form of push-pull or totem-pole output structure, in which significant power is consumed only during output transitions. Medium-power RF transistors are used in the final stage driven by low-power high-speed switching transistors connected in a Darlington configuration. The pull up and pull down transistors must be driven in a complementary manner. The necessary complementary signals can be obtained using the two outputs of the differential amplifier or with the use of a single stage phase inverter.

Speed-up Techniques

The switching time of the driver can be greatly reduced by preventing all transistors from going into saturation. A saturated transistor can take up to 400 nsec to turn off due to junction storage time. An effective method of preventing transistor saturation is through the use of Schottky clamping. The negative feedback provided by the clamp will allow the transistor to approach saturation but never enter it. As a result, the turn-off time can be made comparable to turn-on time.

Secondly, the use of speed-up capacitors in parallel with the resistors in transistor base circuits can improve turn-off and turn on time as well. When the transistor is turned on, the base is initially driven harder; when turned off, the base is driven below the emitter voltage to aid in removing charge from the base-emitter junction area.

Using the techniques discussed above, a circuit can be developed to meet the requirements. The combined circuit is shown in block diagram form in Figure 8. Other considerations are to keep the geometry as small as possible, while also being cognizant of power dissipation requirements.

OUTPUT

In the time expansion application of the PCCD which has been discussed, the output is required to operate at a greatly reduced speed, namely 125 KHz. This feature greatly reduces the degree of design difficulty and opens the door to a variety of approaches. A discussion of the various output approaches is beyond the scope of this paper. However, the output structure and operation for the PCCD discussed above will be described. The general considerations mentioned will apply to most output approaches operating in the same speed range. In the particular application discussed, the output of the CCD is to be digitized by an A/D converter. Since a CCD present valid output data for only 25% of the output clock period, it is important that all output circuits respond quickly to allow sufficient time for the A/D to complete the conversion before the output data becomes invalid.

CCD OUTPUT

The output of the PCCD is buffered by an on-chip FET. A reset FET is employed to remove the charge from the previous sample prior to shifting the next sample for read out. An equivalent circuit of the output structure is shown in Figure 9. Both devices are N-channel depletion-mode types. The output FET operates in a source-follower configuration. Hence, the output FET drain will be connected to some positive DC bias voltage. The output FET source is connected to a negative supply voltage via a load resistor. In the source-follower mode, the output voltage will be approximately the same as the gate voltage, which is a function of the amount of charge on the gate. This gate acts as a capacitor. The charge being propagated in the devices used are electrons. Hence, a larger charge packet will result in more negative output voltage. The reset FET source is connected to the output FET gate. This FET also operates in a source-follower mode. When a positive pulse signal is applied to the reset FET gate, the output FET

gate is reset to about the same potential as that of the reset FET gate unless it is driven into saturation, in which case the reset level is dependent on the reset FET drain voltage. The reset FET drain is connected to some positive voltage, usually the same as the N+ diffusion ring on the CCD. A description of each of the supporting external circuits for the output circuit follow. It should be remembered that the CCD's discussed in this paper were used in a time expansion mode exclusively. Hence, the output circuitry need not be the type that can operate at the high input frequencies, but only at the read out frequency of 125 KHz.

RESET CIRCUITS

The reset FET gate pulse must be properly timed with the four CCD gate drives. A properly timed reset occurs when both $\emptyset_1$ and $\emptyset_2$ are in the high state or the gate potentials are as shown in Figure 10. It is also strongly recommended by the device manufacturer that, during the high speed input of the CCD, the output be in a state of constant, or DC, reset, so the reset FET will remove the charge which is now entering the output at a high rate. The reset pulse width, during read out, is not critical, but the falling edge of the reset pulse must occur before the resing edge of $\emptyset_3$. The last propagation gate of the CCD is $\emptyset_3$. When $\emptyset_3$ gate voltage goes to the high state, the $\emptyset_3$ barrier drops and charges from the next sample begin to flow to the output FET gate. A portion of this charge will be removed by the reset FET should the reset signal remain in the high state after the rise of $\emptyset_3$, thus distoring the charge packet.

The reset pulse amplitude is very critical if the reset FET is not driven into saturation. This is because the reset FET is then operating as a source follower and when turned on will have reset the output to a voltage determined by the reset pulse voltage itself. Following the reset, the output voltage will become more negative as the next charge packet is shifted in. Provided that the CCD is correctly biased, this voltage change will be proportional to the amount of charge shifted to the output FET gate. Hence, a change in the amplitude of the reset FET gate pulse will result in an offset of the entire output voltage levels including the portion of the output waveform containing the usable output signal. Considering the fact that the output signal from full well to empty well is seen on the output FET source as a ΔV of less than 0.5V, it is imperative that the reset FET pulse amplitude be carefully regulated. This can be accomplished by clamping the reset FET gate to a precision reference or using a common emitter transistor as a reset driver. In the later case, the collector load can be a precision resistive divider on a well regulated voltage as shown in Figure 11. The precision resistors R_1 and R_2 can be selected in such a way as to result in the desired reset voltage when the driver transistor is turned off. The reset FET may be operated in saturation in which case the output reset level becomes relatively independent of the gate pulse voltage. The reset level in this case will be the bias voltage on the reset drain, which must then be well regulated to insure accurate reset. The "on" resistance of the saturated reset FET must be small enough to insure total dissipation of the signal charge within the duration of the reset pulse. An additional constraint on the reset FET is that it be capable of dissipating the residual charge which is dumped into the output diffusion during the input loading mode of the CCD. Failure to dissipate this charge will result in a back flooding of charge at the output which will completely destroy the initial signal charge packet.

SIGNAL OUTPUT

As mentioned above, the output of the CCD is a source-follower FET. The output waveform is shown in Figure 12. The useable signal output range of the CCD is about 0.2 to 0.4 volts. As shown in the figure, the output waveform has an overall voltage swing about an order of magnitude greater than the useable signal range. This must be contended with by the output interface circuitry and will be discussed later. Certain characteristics of the output FET must be considered here. The voltage gain of the output MOS-FET is constant over the operating temperature range, typically about 0.9. The output offset voltage is not as stable. As is typically the case with MOS-FET's, the output FET gate to source voltage has a temperature coefficient, TC, which is a function of drain current[5]. This TC can be as large as 1.5 mv/^{o}C. Considering an operating temperature range of 50^{o}C, this

results in an output offset shift of up to 75 mv as a function of temperature. This is about 25% of the dynamic range of the CCD output and, therefore, is a cause of concern. For a given FET, a particular drain current exists where the gate to source voltage has a zero temperature coefficient. At drain currents below this point, the V_{GS} has a positive TC, and higher drain currents yield a negative TC. It has been empirically determined that the drain current for zero TC of V_{gs} was about 0.1 ma for the devices used. The drain current is predominantly determined by the output voltage, the source resistance and the supply voltage V_{ss}. The supply voltage must be sufficiently negative to accommodate the negative signal voltage swing which in this case is about -8 to -10 volts. To operate at .1 ma, the source resistor R_S is:

$$R_s = \frac{V_s - V_{ss}}{I_{source}} = \frac{-5 - (-8)}{.1 \text{ ma}} = 30 \text{ K}\Omega$$

With this high impedance, the time constant of the output circuitry, assuming a 10 pf load resulting from stray capacitance, is:

$$\tau = R_s \cdot C_{out} = 3 \times 10^4 \times 10^{-11} = 0.3 \text{ } \mu\text{sec}$$

This is compared with the time when data is valid on the CCD output, which is less than 1/4 of the output shift period (in this case, 2 µsec). Hence, the time constant of the output circuit is a significant portion of the time when CCD data is available. To remedy this situation, the value of R_s must be reduced to lower the time constant which raises the bias current of the FET, resulting in a negative temperature coefficient V_{gs}.

One of two approaches can be taken to remove this temperature dependency. The first would be to correct for the output offset with external circuitry, which is a difficult task at best. Another method is to design the output FET such that the operating drain current yields a V_{gs} temperature coefficient of zero. The latter approach, while not possible in all applications, is very desirable.

As indicated previously, the dynamic range of the output is only .2 to .4v p-p. Since the ultimate goal in this application is to digitize this analog signal, amplification is required to produce a signal dynamic range of 10 volts p-p to be consistent with available analog to digital converters. To achieve this, an external amplifier gain of 20 to 50 is required. Also, the offset of 5 volts must be removed so the resultant amplifier output is +5 volts. It can be seen that with the high gain of the amplifier, the 5 volt swing on the input during reset will cause the amplifier to go into nonlinear operation. Care must be taken in the amplifier design to prevent device saturation when the reset pulse overdrives the input. If this saturation is not prevented, the amplifier will not settle to the desired output value within $T_0/8$ or 1 µsec. This latter requirement is necessary so the remaining 1 µsec, during which the CCD output presents valid data, may be allocated to the A/D for digitization time.

THERMAL FILLING AND RADIATION EFFECTS

The extent of filling of the CCD by thermal, or dark, current is a function of CCD chip temperature and shift rate. For a given chip temperature, the amount of charge in a given packet which is due to dark current is directly proportional to the time that the charge packet is in residence in the CCD channel. In this application of time expansion, the amount of time that a charge packet is in the CCD channel during the high-speed input mode is insignificant compared to the time required for the CCD read out. It will be assumed that the loading time is zero.

As the charge is shifted out at a relatively slow rate, the first charge packet will not be affected by thermal filling. As the read out progresses, subsequent charge packets will have been in residence in the channel for progressively longer periods of time. This can be seen by viewing the output of a CCD with zero input signal. The first sample is at cutoff, indicating an empty well, subsequent samples will become more negative, indicating increasing amount of charge, forming a negative sloping line. As the read out frequency is reduced, the slope of the line increases. Eventually, a frequency is reached where the last sample read is a full well. Ideally, it is desirable that the output shift rate be high enough that the slope of the output signal is essentially

zero. In all probability, such a frequency may not be consistent with moderate speed A/D converters, hence greatly increasing the cost of digitizing hardware. In addition, variance in dark current from one device to another makes compensation difficult.

The effects of gamma radiation are similar to those of thermal filling. When the CCD is exposed to such radiation, substrate atoms are ionized and the resultant electrons are able to enter the potential wells in the CCD channel. The extent of this well filling is not predictable, but it is reasonable to assume that all wells will experience the same amount of additional charge. If the gamma radiation pulse is incident on the CCD when half of the samples have been read, the remaining half of the samples will have a DC offset with respect to the first half.

A differential channel CCD can be used to remove the effects of thermal and radiation well filling. This is accomplished by using a two channel CCD on the same substrate, driven by the same clock signals. The input signal is applied to only one channel; the remaining channel will have only a DC level on its input. As a result, the only variation in the output of the second channel will be due to thermal and radiation effects. The two channel outputs are connected to a differential amplifier, possibly integrated with the output amplifier for signal gain. The radiation and thermal filling will be common to both channel outputs; consequently their effects will not be seen on the output of the amplifier.

CONCLUSION

The supporting peripheral circuitry required to operate a high speed CCD has been designed and implemented with discrete standardly available devices. The developed circuits enable the devices to approach their present full performance capability in a working system application. The cost-effective implementation of the major elements of the support system, such as propagation drivers and input circuits, suggest the CCD approach to many very high speed analog applications is a viable one. Standard high speed ECL logic families were found to be adequate for developing and timing the various clocking and control signals required. Because the time expansion application was of major concern, high-speed output circuitry was not considered extensively. The design and interface techniques required to develop such circuitry, however, are similar to those described.

Areas in which improvement could benefit overall system performance and ease of production are sample and hold amplitude accuracy and propagation gate driver delay consistency. Methods of increasing the isolation between sample and hold output and the high level CCD propagation gate signals are currently being investigated. More accurate control of propagation gate timing will improve accuracy of the potential equilibrium input method and insure maximum charge handling capability of the CCD (improved dynamic range). Differential channel CCD's have been successfully operated at lower speeds[6]. Significant advantages to a similar approach at high speed operation are anticipated. Greatly increased input common mode rejection should result if identical input structures are used. Thermal and radiation filling as well as EMI effects on the output signal will be greatly reduced if channel balance is maintained. Compensation of output device offsets and temperature drifts should be more easily achieved. GARD is currently developing a dual channel PCCD system operating at the speeds described.

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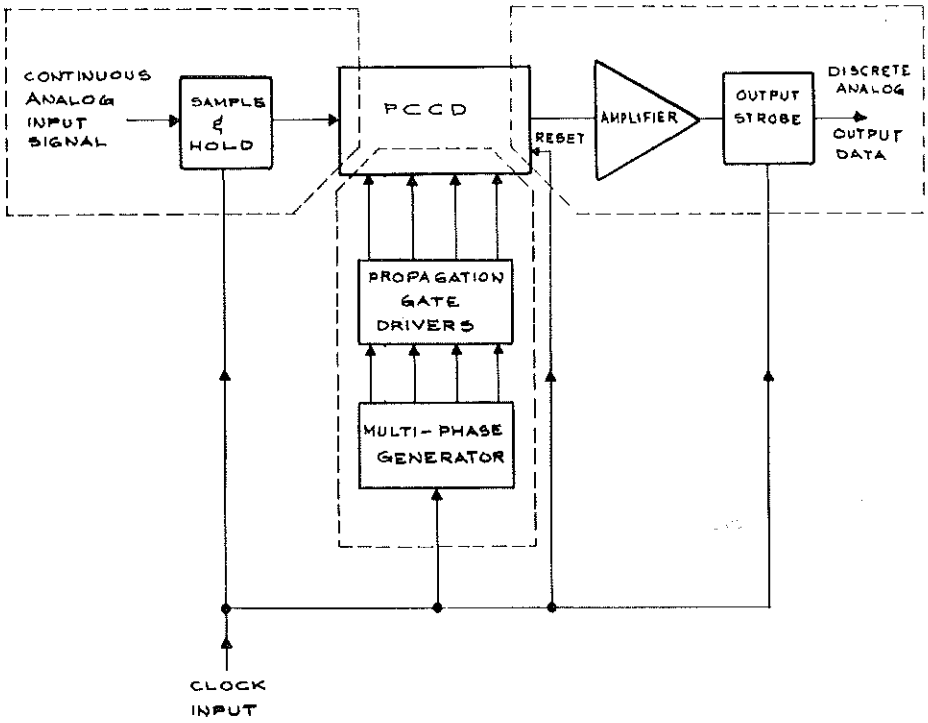

Figure 1. Functional CCD Analog System Block Diagram

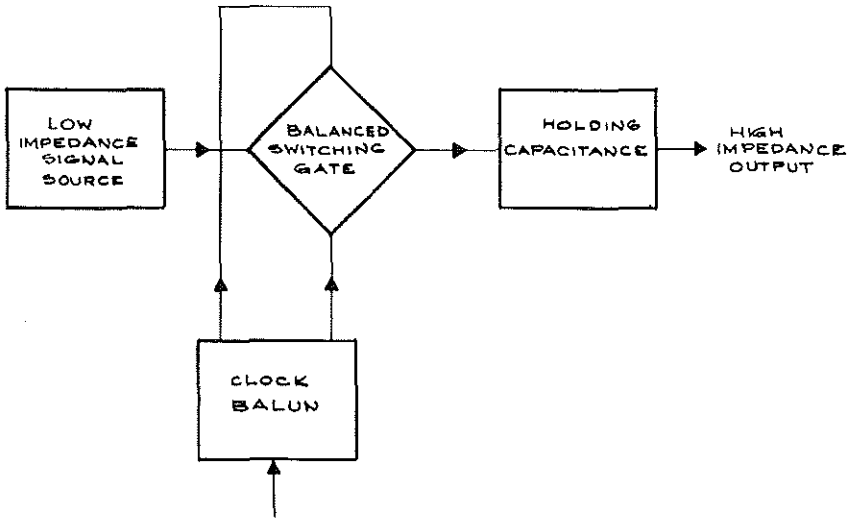

Figure 2. Track and Hold Circuit, Block Diagram

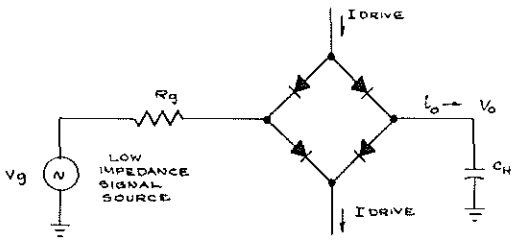

Figure 3. Track and Hold Circuit for Charging Analysis

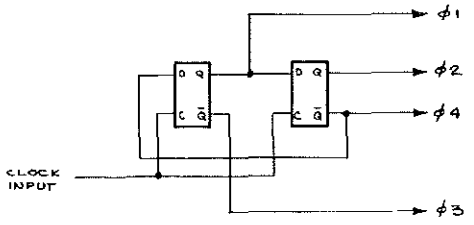

Figure 5. 4-Phase Generator, Logic Diagram

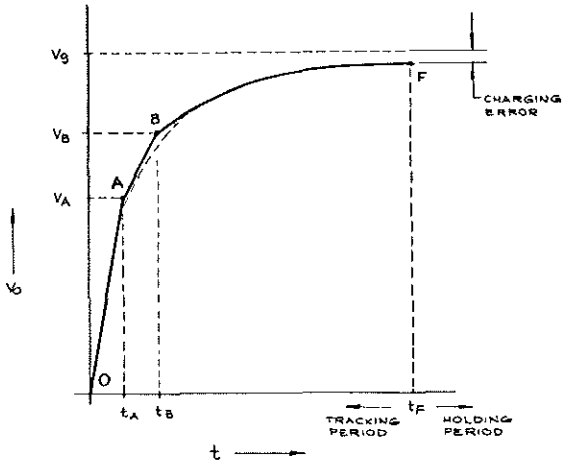

Figure 4. Track and Hold Charging Curve

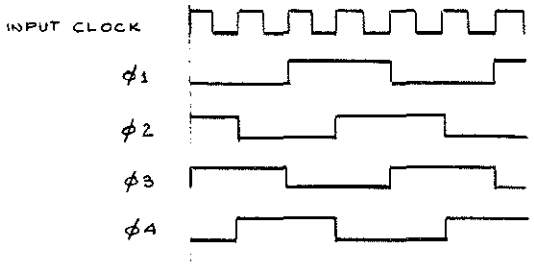

Figure 6. 4-Phase Generator Output, Timing Diagram

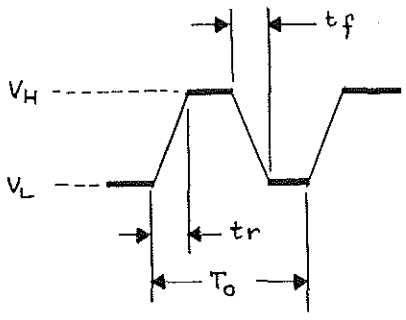

Figure 7. CCD Drive Waveform

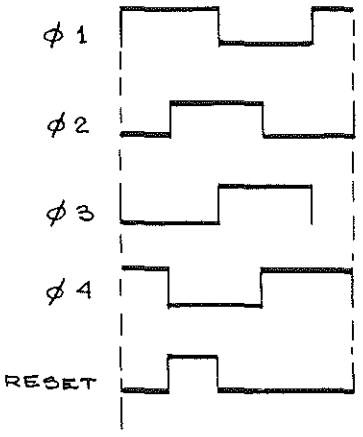

Figure 10. Reset FET Gate Driver, Timing Diagram

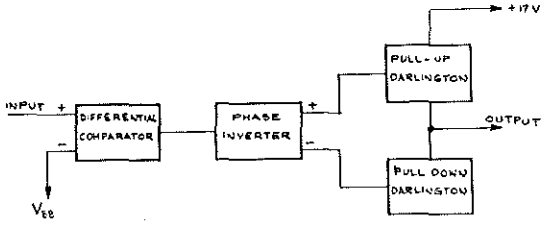

Figure 8. CCD Clock Driver, Block Diagram

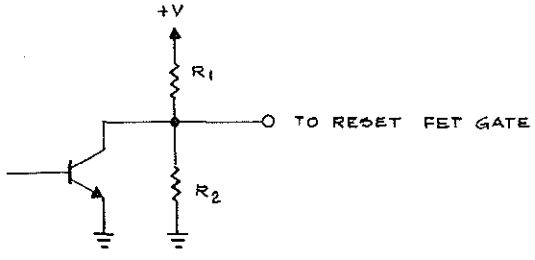

Figure 11. Reset FET Gate Drive Circuit

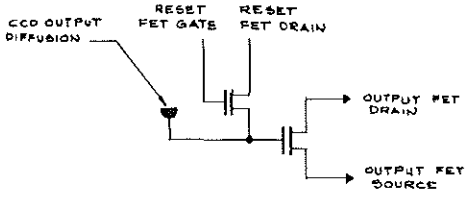

Figure 9. CCD Output Circuit

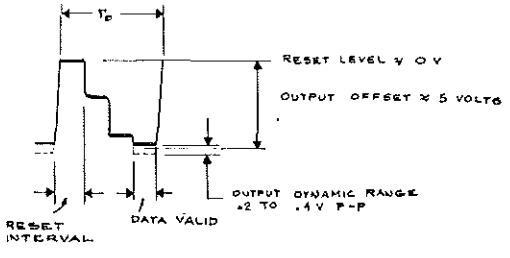

Figure 12. CCD Output Waveform