RADIATION HARDNESS OF SURFACE AND BURIED CHANNEL CCDs*

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ABSTRACT. A series of radiation tests have been performed to determine the effects of gamma, pulsed electron beam, and neutron radiation on several variations of double level electrode surface and buried channel CCD structures. The test samples were characterized in terms of leakage current, well capacity, noise spectrum, and linearity of the CCDs and plus leakage, capacitance, and threshold voltage of MOSFETs and gated diodes on the CCD chip before and after exposure. The latest group of tests included: 1) Neutron total fluence effects tests at levels of 10^{11} to 10^{13} neutrons/cm^2. 2) Total gamma dose effects tests at dose levels of 10^4 to 3×10^6 rad from Co^{60}. 3) Low rate gamma response tests at rates of 5 to 100 rad/sec. 4) High dose rate pulse survival and recovery time tests using 100 ns Linac electron beam pulses at dose rates of 10^9 to 10^{11} rad/sec. The results to date from examination of the test data are reported. Results from these tests include a comparison of the gamma total dose effects on aluminum gate and poly-silicon gate devices, neutron total dose effects, and photo current generation rates for Co^{60} gamma radiation.

INTRODUCTION

Many military and space applications of CCDs will require operation in nuclear radiation environments. A series of radiation tests have been performed to determine the effects of total gamma dose, low dose rate gamma, high dose rate pulsed electron beam, and fission spectrum neutron radiation on several variations of double level electrode surface and buried channel CCD structures. Both aluminum gate and poly-silicon gate devices were included in the latest tests.

The CCD chip used for the test samples contains: (1) a 150 bit 4Ø overlapping gate CCD with a precharge diffusion/source follower output, (2) an MOS gated diode and capacitor (3) a short channel MOSFET, and (4) a field oxide MOSFET. The test samples included aluminum and polysilicon gate devices from the same processing lot, devices with gate oxide through which ions had been implanted and devices which had a new gate oxide grown after ion-implantation. The gate oxide for all devices was grown dry at 1000°C.

Detailed electrical characterization of the test samples was done before and after irradiation on each sample. The measurements made are listed in Table 1. The variation of CCD leakage with temperature for a typical device before irradiation was measured from -15°C to +75°C and found to vary linearly with temperature, doubling for approximately each 80°C temperature increase. Analysis of the measurement data after irradiation is still in progress. Descriptions of the radiation tests and the results obtained to date are discussed in the remainder of this paper.

NEUTRON EFFECTS TESTS

The neutron total fluence test exposures were made at the Fast Burst Reactor (FBR) at the Nuclear Effects Laboratory at White Sands Missile Range. The test levels were 1.3×10^{11}, 1.4×10^{12}, and 1.0×10^{13} neutrons/cm^2, and one-third of the test samples were exposed to each of the levels. The corresponding gamma

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dose exposures were 40, 250, and 950 rad (Si). For the 10^{13} n/cm^2 exposure, a 10 cm thick lead shield was used to reduce the gamma dose level below 10^3 rad. Sulfur pellets were used for the neutron dosimetry and TLD-400 for the gamma dosimetry.

To reduce the effects of the small, unavoidable gamma exposure on the neutron test devices, all samples were irradiated under zero bias conditions. This was achieved by shorting the leads of the test samples together by means of a layer of conductive foam. This also protected the devices from any damage due to possible EMP effects during the reactor pulse transient.

Twenty-one test samples were used for the neutron tests, including nine SC aluminum gate samples, nine BC aluminum gate samples, and three SC polysilicon gate devices.

NEUTRON TEST RESULTS

The analysis of the neutron test results to date has shown no unexpected effects on CCD operation from neutron irradiation. As shown in Figure 1, the integrated CCD leakage current increases nearly linearly with increasing fluence in the 10^{11} to 10^{13} neutrons/cm^2 range. The leakage increased by approximately a factor of six for each decade increase in fluence for both BC and SC samples. The gated diode leakages as a function of gate voltage for these samples were examined to determine the source of this leakage increase. The changes of the bulk and surface components are plotted in Figure 2 for buried-channel samples and in Figure 3 for surface-channel samples. From these curves, it can be seen that the bulk component of leakage increases rapidly with neutron fluence, but the surface component increases only slightly. It is probable that the increase in surface component is due to the small gamma dose received with the neutron exposure. If the change in leakage with gamma dose shown in Figure 9 is extrapolated to lower dose levels, the values of surface leakage current obtained are of the same order as seen in Figure 2.

The changes in charge transfer inefficiency (CTI) with neutron fluence for typical SC and BC devices operated with fat zero are shown in Figure 4. For the 10^{13} n/cm^2 fluence samples it is seen that the CTI for BC devices is increased much more than for SC devices. This result, together with the leakage current data, shows that the neutron irradiation produces mainly bulk crystal damage and causes relatively small amounts of oxide charge buildup and surface state increase. The threshold voltage shifts which were less than 0.5 volt also indicate that very little oxide charge increase was caused by the neutron irradiation. No significant differences have been seen between the aluminum gate and polysilicon gate samples in regard to the effects of neutron exposure.

LOW DOSE RATE GAMMA EFFECTS TESTS

The low dose rate gamma tests were made at the Co^{60} gamma facility at Sandia Labs in Albuquerque. The minimum rate achievable with this source was 5 rad/sec, so the tests were made at dose levels of 5, 15, and 100 rad/sec, instead of the 1, 10, and 100 rad/sec levels originally planned. The dose rates were determined by TLD-400 dosimetry.

The samples used in these tests were six BC samples and six SC samples, including both aluminum and polysilicon gate devices. The samples were operated during irradiation in a test fixture that allows six test CCDs to be operated simultaneously. The clocks and input signals are provided to all six samples in parallel through coaxial cables from clock and signal generation electronics located outside the radiation chamber. The individual CCD outputs can be selected one at a time. The clock generator logic allows the test set to be operated in either the integrate and shift-out mode or the continuous clocking mode. For the gamma rate response tests, the samples were operated in the integrate mode with the integration time at each dose rate selected to provide an output signal large enough for accurate measurement, but not so large as to fill the well.

The results of these measurements are shown for three typical BC and three typical SC samples in Figures 5 and 6. These figures show the time required to completely fill the CCD well versus the dose rate. The times shown are extrapolated from the measured data. The variation between samples was due mainly to differences in full well capacity. Typical times range from 50 msec at 5.5 rad/sec to 5 msec at 100 rad/sec. This corresponds to generation rates of 3.1×10^{13} electrons/rad-cm^3 at 5.5 rad/sec to 1.27×10^{13} electrons/rad-cm^3 at 100 rad/sec, based on an

estimated collection volume of 7.86×10^{-7} cm^3.

GAMMA TOTAL DOSE TESTS

The gamma total dose tests were also made using the Co^{60} gamma facility at Sandia Labs. Dose rates used for the total dose test ranged from 100 to 230 rad/sec. Exposure levels were determined by TLD-400 and Cobalt Glass dosimetry. Table 2 summarizes the tests, showing the number and type of samples irradiated to each level and the dose levels at which data were taken for each group.

The same test set was used for these tests as was used for the low rate gamma test. During exposure, all the devices were run in the normal clocking mode with the common input level set so that all samples were operating at a charge level lower than full-well. The input level was set this way so that the BC units would be operating in the buried-channel mode, as is necessary to reduce oxide charge build-up effects. Any one of the six CCD outputs could be selected and observed by means of reed relay switches and a return cable driver in the test fixture. Before exposure and at each of the intermediate levels, the following CCD parameters were measured with the radiation off: (1) input diode threshold level, (2) charge transfer efficiency, (3) integrated CCD leakage current, and (4) output dc voltage level.

The CCDs were operated with normal bias and continuous clocking during irradiation. The clock voltage levels for all the active tests were 0 and +12 volts. For the other tests devices, the source and drain diffusions were reverse-biased with +20 volts, and a 0 to +12 volt 50% duty cycle pulse was applied to all gates except the gate of the field oxide transistor, which was connected to +28 volts.

GAMMA TOTAL DOSE TEST RESULTS

Analysis to date of the data from the post-exposure measurements of the gamma test samples showed that the results for BC devices are similar to those from the earlier tests. The most serious degradation from gamma radiation is the very large leakage current increase and the resulting reductions in storage time and dynamic range and increase in noise. One new result from these tests is that this leakage increase is large even at low dose levels, as seen in Figure 7. The leakage for sample 130-4-89, which initially was 2.0 nA/cm^2, increased to 160 nA/cm^2 at 3×10^4 rad and to 385 nA/cm^2 at 10^5 rad. At the 10^6 rad level, the leakage was measured with the substrate voltage first at 0 volt as at the lower dose levels, and then at a positive substrate bias to reduce the potential difference between the channel and the channel stop. It can be seen that this reduced the leakage by nearly 50%. It was then decided to run the next group of samples at a positive substrate bias(relative to the low clock level) during exposure. The result of this change is illustrated by the curve for sample 130-4-88. The leakage current increase was significantly less at 3×10^4 and 10^5 rad, but at 3×10^5 rad and higher it was equal to the zero substrate bias case.

The limitations that leakage currents of this magnitude impose on a given system depend, of course, on the particular system requirements for storage time, dynamic range, and noise. However, the leakage levels seen even at 10^5 rad are too high for many applications. Figure 8 is a series of curves obtained by combining the measured effects of photocurrent resulting from a background level of gamma radiation and the leakage caused by the permanent damage effect of the accumulated gamma radiation dose. The curves give the calculated time to reach a level of 10% of full-well for a typical BC sample. That is, if a maximum leakage generated charge of 10% of a full signal charge is allowed, the times shown are the maximum time that a given information bit can be stored in the CCD. The 10% full-well criterion is too high for most analog applications, but might be allowable in a digital memory. For the case of zero background radiation, a dose of 10^6 rad reduces the storage time at room temperature from more than one second to 3.2 msec. At background radiation levels of about 15 rad/sec, the leakage due to photocurrent is about equal to that caused by 10^6 rad accumulated dose, and at higher background levels the photocurrent component is dominant.

The leakage current versus gate voltage characteristics of the gated diodes were studied to determine the source of this radiation-induced leakage. The typical variation of the surface and bulk components of leakage for these samples is shown in

Figure 9. Before irradiation, both components were about 1 pA, but after 10^5 rad the surface component had increased about 75 times, while the bulk component had only doubled.

The gated diode leakage vs gate voltage plots of Figures 10 and 11 show the very large increases in total leakage as the gate voltage goes positive that were seen on devices from the earlier tests. At the 3×10^6 level this leakage, which is thought to be due to breakdown caused by high surface fields at the channel stop junction, is so large that it nearly obscures the leakage step due to depletion of the surface. A more detailed investigation of the nature and cause of the effect is being performed.

The change in charge transfer inefficiency with gamma dose for these test samples was similar to earlier results. Figure 12 shows results for typical samples. Again, there was considerable variation from sample to sample in CTI, as in the last tests. The only difference seen so far between aluminum and polysilicon metallization is a larger V_T shift with the polysilicon gate for gamma radiation. For the gate oxide MOSFET after 10^6 rad the typical ΔV_T for aluminum was 2.5 volts, and for polysilicon it was 4.5 volts.

HIGH DOSE RATE IONIZING PULSE RECOVERY TESTS

The high dose rate ionizing pulse recovery tests were made on the Linac at WSMR operating in the direct electron beam mode. The tests were made in the same way as in the previous series, but the new test fixture permitted closer approach of the sample to the Linac exit window so that the maximum dose rate achieved was 10^{11} rad/sec. The electron energy was 20 MeV and the pulse width was 100 nsec. Series current-limiting resistors of 100 to 200 Ω were placed in each of the CCD supply leads.

Seven samples were tested, including surface and buried-channel devices and aluminum and silicon gate devices. The test data have not yet been completely analyzed, but no evidence has been found of the thermal damage that was seen in the previous test when no current-limiting resistors were used. The time required for the output circuit to return to normal operating levels and to remove the full wells of photo current from the CCD channel was from 250-300 μsec at a clock rate of 1 MHz.

SUMMARY OF RESULTS TO DATE

The main effect of neutron exposure in the 10^{11} to 10^{13} neutrons/cm^2 range is an increase in the bulk component of leakage, which apparently is due to lattice displacement damage. Above 10^{12} neutrons/cm^2 this damage also significantly degrades the charge transfer efficiency of buried-channel CCDs.

Photon-generated charge from continuous gamma radiation was found to fill the wells of BC devices in times ranging from about 50 msec at 5.0 rad/sec to 5 msec at 100 rad/sec.

The total gamma dose effects results that have been analyzed are similar to those from earlier tests, with the new result that the surface leakage buildup is large enough to seriously affect storage times even at doses as low as 3×10^4 rad. The recovery times seen in the high dose rate transient tests were from 250 to 300 μsec for a clock rate of 1 MHz. By use of current-limiting resistors, thermal damage from photocurrent can be prevented for dose rates up to at least 10^{11} rad/sec for 100 nsec pulses.

The only significant difference found between aluminum and polysilicon gates is a larger threshold voltage shift with polysilicon from gamma dose effects.

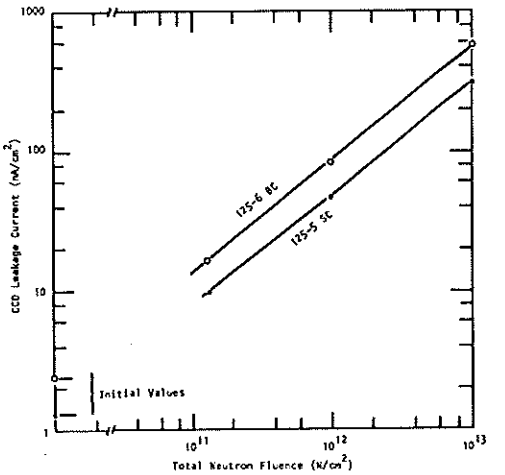


Figure 1 Typical CCD Integrated Leakage vs Neutron Fluence

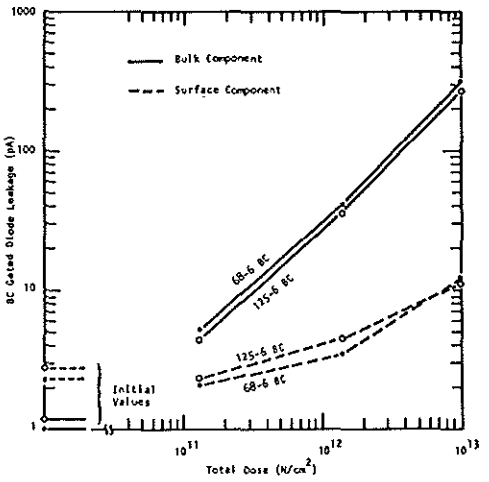


Figure 2 BC Gated Diode Leakage vs Neutron Fluence

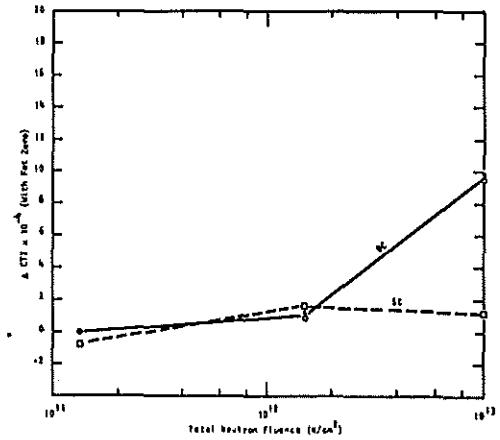


Figure 4 Change in Charge Transfer Inefficiency (CTI) with Neutron Fluence for Typical Surface- and Buried-Channel CCDs

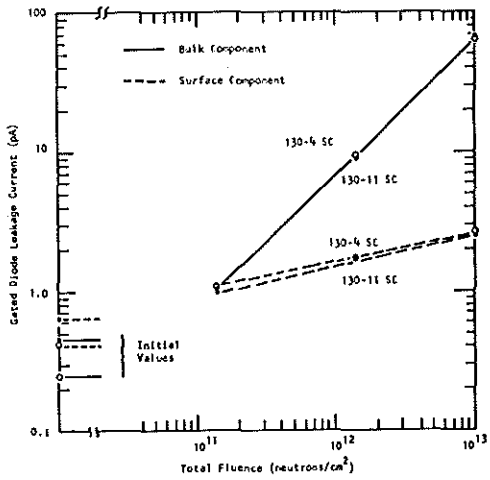


Figure 3 SC Gated Diode Leakage vs Neutron Fluence

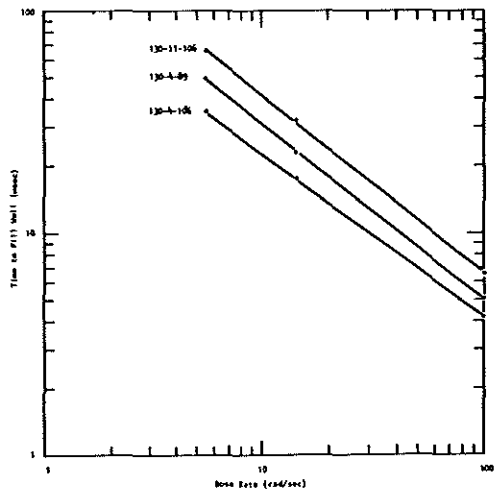


Figure 5 Fill Time of BC CCDs as a Function of Gamma Radiation

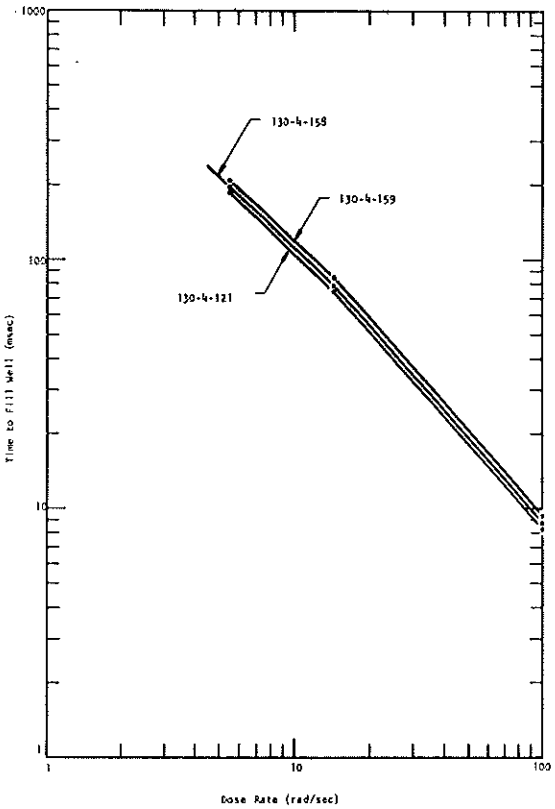


Figure 6 Fill Time of SC CCDs as a Function of Gamma Radiation

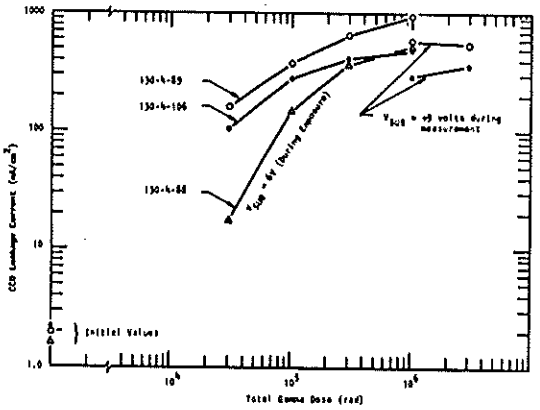


Figure 7 Typical Buried Channel CCD Leakage vs Gamma Dose

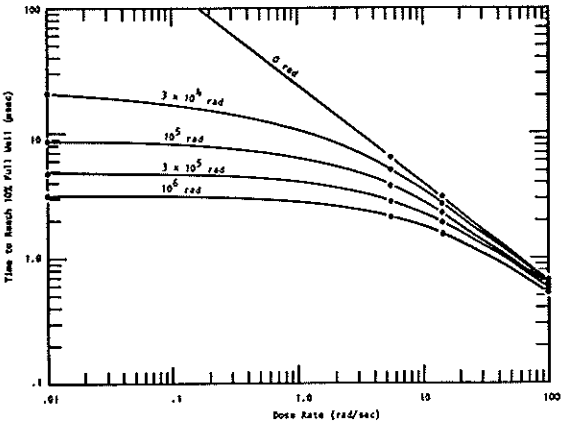


Figure 8 Effects of Low Rate Gamma Radiation on CCD Storage Time After Various Total Dose Levels

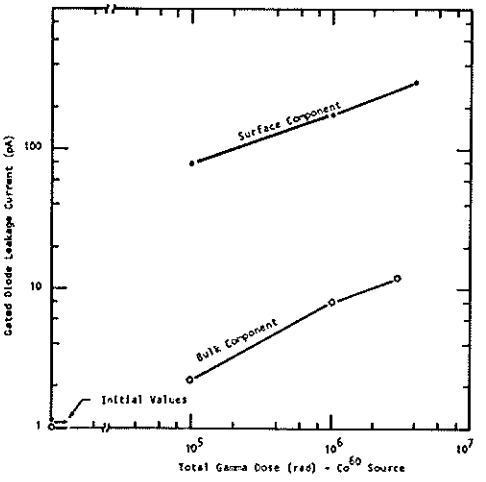


Figure 9 Graph of Bulk and Surface Components of Gated Diode Leakage vs Gamma Dose for BC Samples

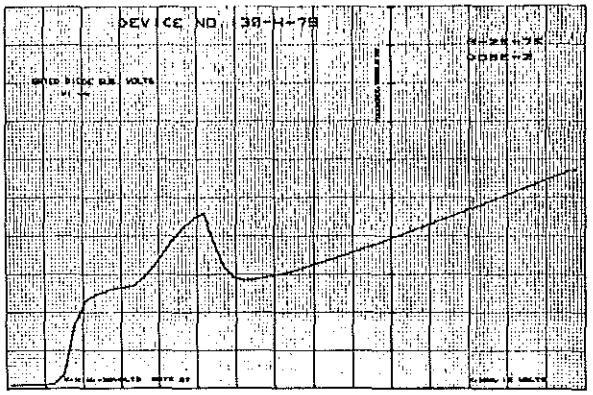


Figure 10 Plot of Gated Diode Leakage vs Gate Voltage for BC Sample After 10^6 Rad. Vertical scale is 100 pA/mark; horizontal scale is 2.0 volts/mark.

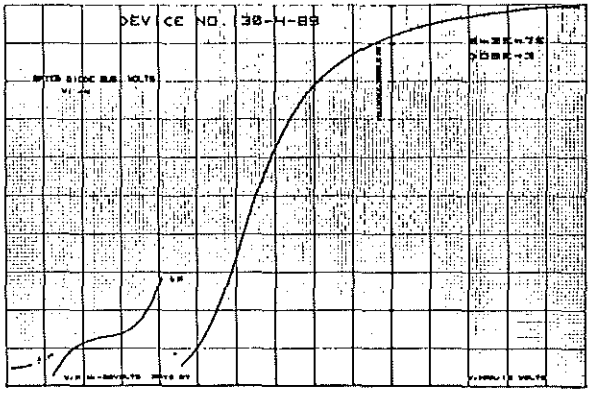


Figure 11 Plot of Gated Diode Leakage vs Gate Voltage for BC Sample After 3×10^6 Rad. Vertical scale is 25,000 pA/mark for $V_G > 11$ volts, 2500 pA/mark for 11 volts $< V_G < 18$ volts, and 250 pA/mark for $V_G < 18$ volts. Horizontal scale is 2.0 volts/mark.

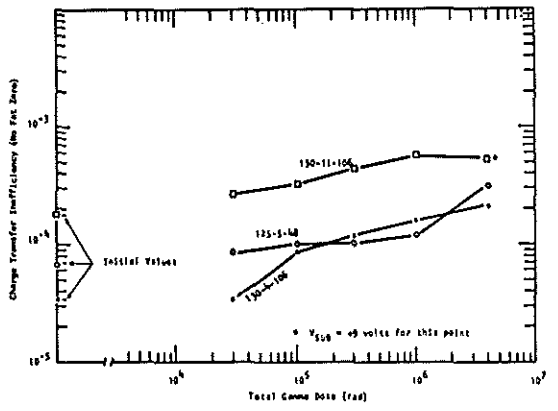


Figure 12 Charge Transfer Inefficiency vs Gamma Dose for Typical BC CCDs

TABLE 1

Test Sample Characterization

Measurement	Test Device	Parameters Sought
Integrated Leakage Current	CCD	CCD Leakage Current
Leakage Versus Gate Voltage	Gated Diode	MOS Capacitor I_L, τ_{Bulk}, S_0, and N_{SS}
Charge Transfer Efficiency	CCD	No Fat Zero CTE, Fat Zero CTE
Channel Current Versus Gate Voltage	CCD	Surface and Bulk Mobility
Threshold Voltage	CCD and MOSFET	V_T and Q_{SS}
Harmonic Distortion	CCD	CCD Linearity
Output Detector Current/ Voltage	CCD	CCD Full Well Capacity and Output Detector Transfer Curve
Output Noise Versus Frequency	CCD	Spectral Noise Density
Diode C-V	Gated Diode	Pinch-Off Voltage and Oxide Thickness

TABLE 2

Summary of Gamma Total Dose Test Units and Dose Levels

Total Dose (rad)	Test Samples	Data Points (rad)
3×10^6	4 Aℓ Gate BC 2 Si Gate BC	0, 3×10^4, 10^5, 3×10^5, 10^6, 3×10^6
10^6	4 Aℓ Gate BC 2 Si Gate BC	0, 3×10^4, 10^5, 3×10^5, 10^6
10^5	4 Aℓ Gate BC 2 Si Gate BC	0, 10^5
10^6	4 Aℓ Gate BC 2 Si Gate BC	0, 10^6
10^5	3 SC	0, 10^5
3×10^5	3 SC	0, 3×10^5
10^4	3 SC	0, 10^4

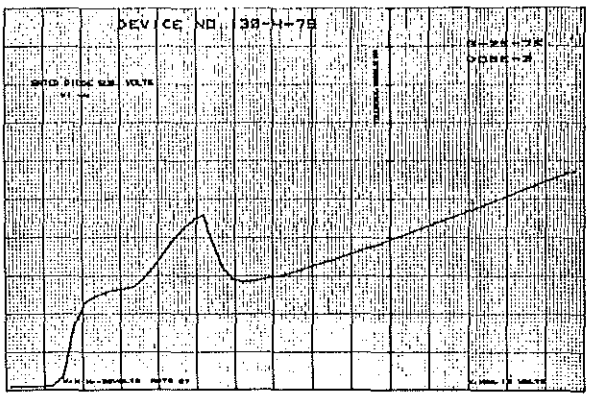
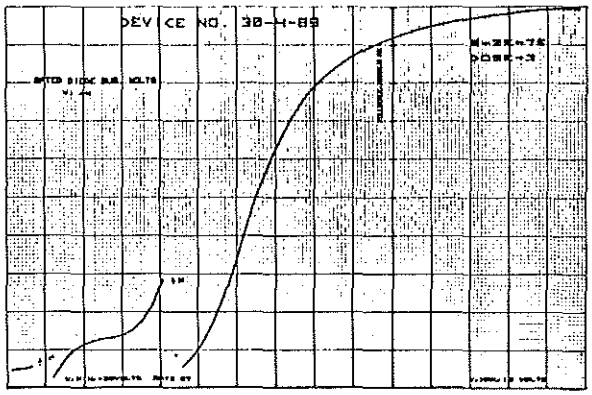


Figure 10 Plot of Gated Diode Leakage vs Gate Voltage for BC Sample After 10^6 Rad. Vertical scale is 100 pA/mark; horizontal scale is 2.0 volts/mark.



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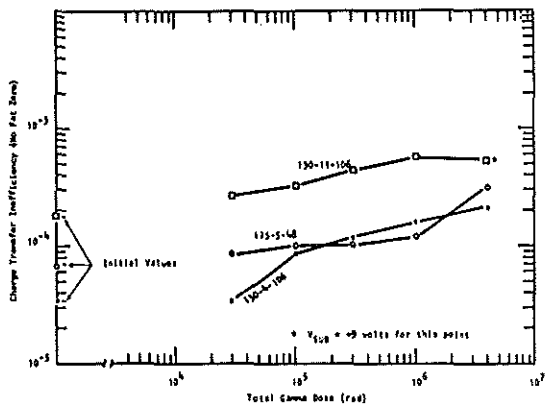

Figure 12 Charge Transfer Inefficiency vs Gamma Dose for Typical BC CCDs

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10^5	4 Aℓ Gate BC 2 Si Gate BC	0, 10^5
10^6	4 Aℓ Gate BC 2 Si Gate BC	0, 10^6
10^5	3 SC	0, 10^5
3×10^5	3 SC	0, 3×10^5
10^4	3 SC	0, 10^4