ANTI-ALIASING CHARACTERISTICS OF THE FLOATING DIFFUSION INPUT*

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ABSTRACT. The CCD is inherently a sample-data device. It follows that preservation of signal-to-noise ratio requires that the noise on the processed signal be bandlimited to avoid aliasing. In many applications, particularly those involving integration of pre-CCD electronics onto the CCD monolith, it is desirable that this low-pass filtering be accomplished by the CCD input itself.

An analysis is presented of the small-signal frequency response of the floating diffusion (FD) input[1,2] which predicts a band-limiting effect approaching the sin x/x response of an ideal integrator. The analysis applies with equal validity to all inputs using the potential equilibration technique.[1,2,3,4,5]

Frequency response data are presented together with noise measurements which agree well with theory. These measurements made on the FD input indicate excellent noise anti-aliasing under practical conditions of operation which maintain the insensitivity to threshold voltage inherent in this input.

I. INTRODUCTION

In most signal processing applications using CCDs, noise and dynamic range are important considerations. Because the CCD is inherently a sample-data device, the band-limiting of high frequency noise and signals (those above the Nyquist frequency) is essential to prevent aliasing. This is often accomplished using RC filters in the interface electronics preceding the CCD input.

This paper deals with the small-signal frequency response of the floating-diffusion input[1,2], a common input technique for injecting charge into CCDs. An analysis is presented which predicts that, properly operated, this input exhibits a frequency response approaching the sin x/x response of an ideal integrator and may be used to effectively prevent noise aliasing. Data are presented verifying this performance. The analysis is equally valid for the "fill-and spill" or "potential equilibration" input[1,2,3,4,5].

The inherent anti-aliasing characteristics of the floating-diffusion input are particularly beneficial in applications where it is desired to integrate all of the pre-CCD interface electronics onto the CCD monolith itself in a high density format. Noise band-limiting is achieved without the undesirable threshold voltage sensitivity characteristic of the true integrator or "direct injection" mode of charge injection.[6]

II. REVIEW OF THE FLOATING DIFFUSION INPUT

The structure of the floating diffusion input is shown in Figure 1. In simple terms, the technique involves first setting the intermediate node to a voltage dependent on the signal voltage applied to the first transfer electrode Vg_1 and then resetting the node to a reference voltage applied to the transfer electrode Vg_2. The

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second process is accomplished through transfer of charge into the receiving CCD well; as such, the charge introduced is derived from the difference in the two preset levels multiplied by the capacitance of the floating node and is insensitive to threshold voltage (V_t) to the extent that V_t is the same under closely spaced electrodes.[6] The noise characteristics of this input are known to be approximately described by kTC.[1,2]

The first process in the two step sampling operation of the floating diffusion input is essentially the "fill-and spill" or "potential equilibration"[1,2,3,4,5] procedure applied to a diffusion instead of a CCD or MIS node. This process is initiated by pulsing the input diode (V_{id}) negatively (for an N channel CCD) to introduce excess charge onto the diffused node and then returning it to a high positive value to extract charge from the node while the channel current is controlled by the signal voltage applied to the input gate (Vgl). The first process is terminated by the pulsing of the second gate, (Vg2) which, for a multiplexer, is the serial-parallel transfer electrode. An analysis will next be presented which predicts that for noise, the time interval associated with the first process constitutes an effective integration time, τ, and the input acts to band-limit the noise.[7,8]

III. FREQUENCY RESPONSE ANALYSIS OF THE "FILL-AND-SPILL" OR "POTENTIAL EQUILIBRATION" TECHNIQUE

As pointed out in the preceding section, the first step in the two-step sampling process of the floating diffusion input is identical to the "fill-and spill" or "potential equilibration" technique. The only difference is that for the floating diffusion case, as charge is being extracted the gate Vgl acts as the gate of the MOSFET whose drain is the input diode and whose source is the diffused node; for the fill-and-spill input, the CCD potential well (or intermediate MIS node) acts as a virtual source. The equations describing the channel current are essentially identical. The input voltage is applied to the gate (Vgl) of the input transistor, and when the input diode V_{id} is pulsed positive, current flows into the capacitor (electrons "spill" out) until the channel current decreases to a small value, i.e., until $V_{fd} \cong V_{in} - V_t$. When V_{in} is a constant value, the problem is well defined and the voltage transient can be calculated.[2] In reference 2, V_{in} is assumed to be constant, and the effect of channel noise is calculated. In this section an analysis is given of the case where the input voltage varies with time during the "spill" transient. The analysis applies to noise on the input or to small input signals.

The circuit diagram for the floating diffusion input during the spill cycle is shown in Fig. 2b. The capacitor voltage v(t) increases after the input diode V_{id} is pulsed positive at t = 0. In the case where the input voltage is constant ($v_n(t) \equiv 0$), the spill transient follows the curve $v_o(t)$ shown in Fig. 2a. For the above threshold case, $v_o(t)$ asymptotically approaches $V_{in}-V_t$ where V_t is the MOS threshold voltage. The spill transient is terminated after time τ when the charge on the capacitor is clocked further into the CCD.

Assume that a small ac signal $v_n(t)$ is applied to the input gate along with the time invariant V_{in}. The asymptotic value which the spill transient approaches changes with time, and the analysis which follows is based upon the fact that the form of the spill transient v(t) depends only upon the asymptotic final value it would be approaching if the gate voltage remained at its instantaneous value $V_{in} + v_n(t)$. This follows from the fact that the channel current is controlled by the voltage between the gate and the floating diffusion node (i.e., the transistor gate-to-source voltage).

Suppose, as shown in Fig. 2a, an incremental change in gate voltage dv_{n1} occurs at some time t_1. The result is to cause the transient to be further away from its new asymptotic final value $V_{in} - V_t + dv_{n1}$. By our assumption the waveform should have the same shape that $v_o(t)$ had at an earlier time $t_1 - dt_{n1}$, where

$$dt_{n1} = \left(\frac{dv_o}{dt}\right)_{t_1}^{-1} dv_{n1} \qquad (1)$$

Analytically, we have defined a new function $v_1(t)$ for the transient, which would be valid for all $t \geq t_1$ if no further incremental changes occurred at the gate. This function $v_1(t)$ is given by

$$v_1(t) = v_o(t - dt_{n1}) + dv_{n1} \qquad (2)$$

where the dv_{n1} reflects the increase in asymptotic final value. Now, suppose a second incremental change occurs at time t_2. In an identical manner a new delay time dt_{n2} is defined by

$$dt_{n2} = \left(\frac{dv_1}{dt}\right)^{-1}_{t_2} dv_{n2} \tag{3}$$

and a new functional form for the transient becomes

$$\begin{aligned} v_2(t) &= v_1(t - dt_{n2}) + dv_{n2} \\ &= v_o(t - dt_{n1} - dt_{n2}) + dv_{n1} + dv_{n2} \end{aligned} \tag{4}$$

Which, as before, would be valid for all $t \geq t_2$ if no further changes in gate voltage were to occur.

As a result of numerous incremental changes in input voltage, the node voltage at the end of the spill transient becomes

$$v(\tau) = v_o\left(\tau - \int_o^\tau dt_n\right) + \int_o^\tau dv_n \tag{5}$$

with dt_n given by

$$dt_n = \left(\frac{dv}{dt}\right)^{-1} dv_n \tag{6}$$

In calculating $\int dt_n$, it is assumed that the time varying input voltage $v_n(t)$ is sufficiently small that dv_o/dt can be used to approximate dv/dt in Eq. (6). This small signal restriction effectively linearizes a highly non-linear input and permits the definition of a linear transfer function. The physical significance of this linearization in terms of its restrictions on the amplitude of $v_n(t)$ remains the primary area for future analysis and experimental work. The simplifying effect of this assumption is that Eq. (5) can be integrated to give

$$v(\tau) = v_o(\tau - t_n) + \int_o^\tau \frac{dv_n}{dt}\, dt \tag{7}$$

where

$$t_n \equiv \int_o^\tau \frac{dv_n/dt}{dv_o/dt}\, dt \tag{8}$$

At this point a further linearization is made. It is assumed that t_n is sufficiently small that $v_o(\tau - t_n)$ can be approximated by

$$v_o(\tau - t_n) = v_o(\tau) - \left(\frac{dv_o}{dt}\right)_\tau t_n \tag{9}$$

whereby Eq. (7) can be written

$$\begin{aligned} v(\tau) = v_o(\tau) &- \left(\frac{dv_o}{dt}\right)_\tau \int_o^\tau \frac{dv_n/dt}{dv_o/dt}\, dt \\ &+ \int_o^\tau \frac{dv_n}{dt}\, dt \end{aligned} \tag{10}$$

The quantity of interest is $\Delta v \equiv v(\tau) - v_o(\tau)$ which represents the difference in final voltage which results from $v_n(t)$. From Eq. (10)

$$\Delta v = \int_o^\tau \left[1 - \frac{(dv_o/dt)_\tau}{dv_o/dt}\right] \frac{dv_n}{dt}\, dt \tag{11}$$

Equation (11) can be used to determine the frequency response of the floating diffusion input. Let us assume that $v_n(t)$ is of the form

$$v_n(t) = V_n\, e^{j2\pi ft}\, u_{-1}(t) \tag{12}$$

where V_n is the complex amplitude of the input noise or signal voltage at frequency f and $u_{-1}(t)$ is the unit step at $t = 0$. Inserting Eq. (12) into (11) and assuming that $(dv_o/dt)_\tau \ll (dv_o/dt)_{t=0}$ gives

$$\Delta v = V_n \left\{1 + \int_o^\tau \left[1 - \frac{(dv_o/dt)_\tau}{dv_o/dt}\right] s e^{st}\, dt\right\} \tag{13}$$

where the shorthand $s \equiv j2\pi f$ has been used.

In order to proceed further with the evaluation of Eq. (13), equations for $v_o(t)$ must be used. Two cases will be considered. 1) The case where τ is so short that the above-threshold transistor equation[9] describes the spill transient.

$$I_D(t) = \frac{\beta}{2}\left(V_{in} - V_t - v(t)\right)^2 \tag{14}$$

In this expression

$$\beta \equiv \frac{W}{L} C_{ox}\, u \tag{15}$$

characterizes the transistor channel width W, channel length L, oxide capacitance per unit area C_{ox} and majority carrier mobility u.

2) The case where τ is so long that the transistor operates in the subthreshold regime during most of its spill transient. In this case the subthreshold transistor equation applies.[10]

$$I_D(t) = \beta \frac{1}{m}\left(n\frac{kT}{q}\right)^2 \exp\left[\frac{q}{nkT}\left(V_{in}-V_t-n\frac{kT}{q}-v(t)\right)\right] \quad (16)$$

where m and n are capacitance ratios on the order of unity which are defined in Ref. 10.

Case 1 applies when

$$\tau < \frac{2C}{\beta}\,\frac{q}{nkT} \quad (17)$$

and case 2 applies when

$$\tau \gg \frac{2C}{\beta}\,\frac{q}{nkT} \quad (18)$$

(See Ref. (11))

Case 1

Assuming Eq. (14) for the transistor drain current, the spill transient $v_o(t)$ can be calculated to be[2,11]

$$v_o(t) = V_{in} - V_t - \frac{V_{in} - V_t - v_o(o)}{1 + \frac{\beta t}{2C}\left[V_{in} - V_t - v_o(o)\right]}, \quad (19)$$

which, apart from an initial transient, is approximately

$$v_o(t) = V_{in} - V_t - \frac{2C}{\beta t}, \quad (20)$$

from which

$$\frac{dv_o}{dt} = \frac{2C}{\beta t^2} \quad (21)$$

Inserting Eq. (21) into Eq. (13) gives

$$\Delta v = V_n\left\{1 + \int_o^\tau \left[1 - \frac{t^2}{\tau^2}\right] se^{st}\,dt\right\} \quad (22)$$

which can be integrated to give the transfer function $H \equiv \Delta v/V_n$

$$H(s) = \frac{2}{s\tau} + \frac{2}{(s\tau)^2}\left(e^{-s\tau} - 1\right). \quad (23)$$

The magnitude of this function is shown in Figure 3 as a solid line.

Case 2

When the transistor is characterized by Eq. (16), the spill transient $v_o(t)$ is given by[11]

$$v_o(t) = V_{in} - V_t - \frac{nkT}{q} + \frac{nkT}{q}\ln\left[\frac{\beta}{C}\frac{n}{m}\frac{kT}{q}(t-t_o)+1\right] \quad (24)$$

where t_o is the time at which the transistor enters the subthreshold regime, i.e., the time at which $v = V_{in}-V_t - nkT/q$. In this analysis it is assumed that $\tau \gg t_o$, and since the form of dv_o/dt is important only at large t, it is approximated by

$$\frac{dv_o}{dt} = \frac{nkT}{q}\,\frac{1}{t} \quad (25)$$

Inserting Eq. (25) into Eq. (13) gives

$$\Delta v = V_n\left\{1 + \int_o^\tau \left[1 - \frac{\tau}{t}\right] se^{st}\,dt\right\} \quad (26)$$

from which H(s) is determined to be

$$H(s) = \frac{1}{s\tau}\left(1 - e^{-s\tau}\right). \quad (27)$$

The magnitude of this is identical to the ideal integrator and is given by the dotted line in Figure 3.

Work is continuing to determine the range of signal amplitudes over which the above linearizations are valid. However, data in the following section support these results.

IV. EXPERIMENTAL RESULTS

A.) Experimental Setup. A schematic is shown in Figure 4 of the experimental setup used for measuring the small-signal frequency response and noise aliasing characteristics of the floating diffusion input.

The output of the CCD is a conventional preset or floating diffusion amplifier, buffered by a bipolar emitter follower. The output waveform is sampled-and-held by an Analog Devices SHA-2. The amplified output of the SHA-2 sample-and-hold circuit is fed into a Hewlett-Packard HP 302A wave analyzer for determination of the RMS level of signal and spectral intensity of noise. At the

input the option exists to apply either a small-signal sinusoid excitation (from the wave-analyzer oscillator) or a white noise voltage from a GR 1390B noise generator. The bandwidth of the applied noise is controllable using a KH 3550 tunable filter. Provisions are also made in the CCD clocking electronics to vary the effective integration, τ.

B.) Small-Signal Frequency Response. The data plotted in Figure 5 were obtained by biasing the input to approximately 50% full well and then modulating this charge level with peak-to-peak charge excursions of the order of 1% (or less) of a full well while varying the normalized integration time, τ/T_c. The clock frequency was 18 kHz. The data in its raw form does not readily indicate the frequency response of the input because of the sin x / x frequency response of the output due to the SHA-2 sample-and-hold circuit. The data was massaged by dividing through, point by point, by the measured frequency response of the SHA-2. The massaged data is shown plotted in Figure 6. For an effective integration time τ of 0.1 T_c, the input response was quite flat well beyond the clock frequency, f_c, in good agreement with the predictions of Figure 3.

For the case of τ = 0.9 T_c, on the other hand, the small-signal response of the input was very nearly that of an ideal sin x / x integrator. This response is in good agreement with the subthreshold model depicted in Figure 3. From an aliasing standpoint, substantial aliasing would be anticipated for the case of τ = 0.1 T_c, where τ = 0.9 T_c mode of operation should yield little or no aliasing.

C.) Noise Aliasing. To corroborate the aliasing conclusions based on the massaged small-signal data, the GR 1390B noise generator was connected to the input (See Figure 4). The raw data is shown in Figure 7. Although again the spectral intensity is effected by the output sin x / x at high frequencies, the aliasing properties can easily be inferred by the low frequency noise intensity. The lowest curve represents the inherent noise obtained with the GR 1390 cut off. The second lowest curve denoted by the solid dots was obtained with the KH 3550 upper cut off frequency set to the Nyquist frequency. The elevated noise indicated input-noise dominated performance. Because of the bandlimiting of the 3550, however, no aliasing was present.

Coincident with the second lowest curve is shown a set of data points denoted by X's. These data were obtained with the KH 3550 bandwidth set at 20 times the Nyquist frequency (or 10 f_c) and with the integration time τ approximately 0.9 T_c. No increase in low-frequency noise was observed; i.e., no aliasing occurred. The two higher noise curves were obtained for smaller values of normalized integration time τ/T_c.

Figure 8 shows a normalized plot of noise data obtained at f = 0.1 f_c for different values of normalized integration time τ/T_c. The dashed line is the theoretical aliasing factor, defined as the fractional increase in low frequency noise due to aliasing, as predicted by the above-threshold model of Figure 3. The data actually indicates better agreement with the subthreshold model, consistent with the small-signal response data of Figure 6.

V. Conclusions

In summary, the small-signal frequency response analysis of section III predicted that substantial anti-aliasing performance may be realized using the floating-diffusion input. The data presented verified this prediction for practical conditions of operation. From an application standpoint, these anti-aliasing characteristics can be a valuable benefit, especially for high density applications where additional filter circuitry is undesirable. The results obtained are equally valid for all inputs incorporating the "fill-and-spill" or "potential equilibration" technique and are achievable while maintaining the high level of threshold voltage insensitivity characteristic of the input technique.

Some important work remains in exploring analytically and experimentally the range of signal amplitudes over which this bandlimiting effect remains operative. Of equal importance is the determination of the effect on the anti-aliasing characteristic resulting from spurious voltage transients in a system, both coherent and random.

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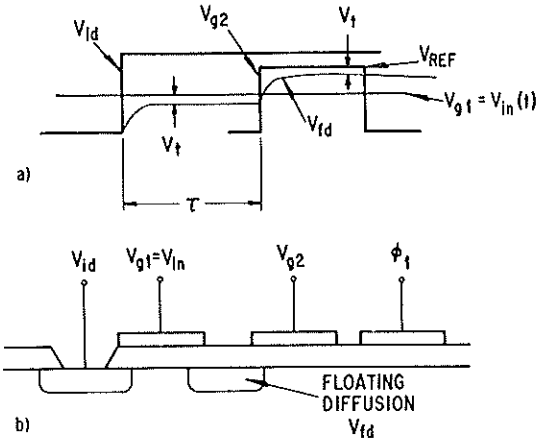

Fig. 1 FLOATING DIFFUSION INPUT
a) Waveforms
b) Structure

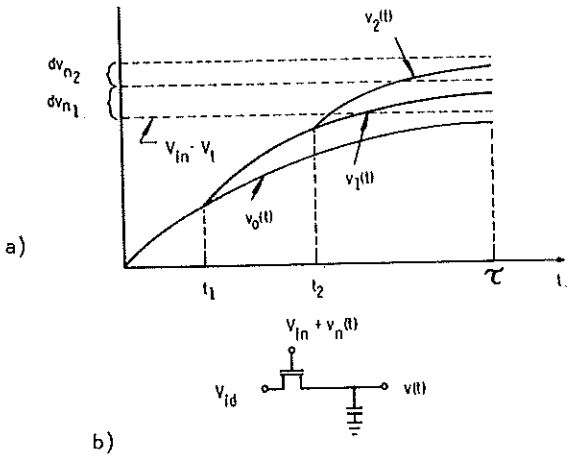

Fig. 2 MODEL FOR ANALYSIS OF SMALL SIGNAL FREQUENCY RESPONSE OF FLOATING DIFFUSION INPUT
a) Transient "spill" curves
b) Circuit diagram

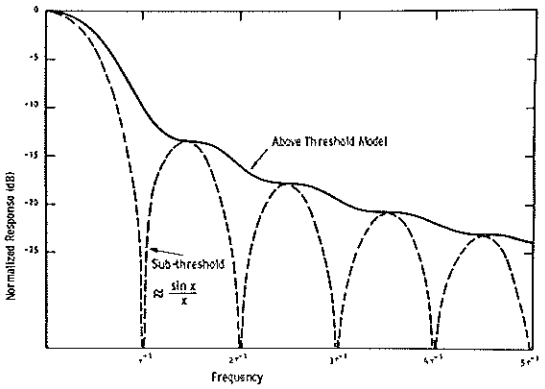

Fig. 3 CALCULATED FREQUENCY RESPONSE OF FLOATING DIFFUSION INPUT

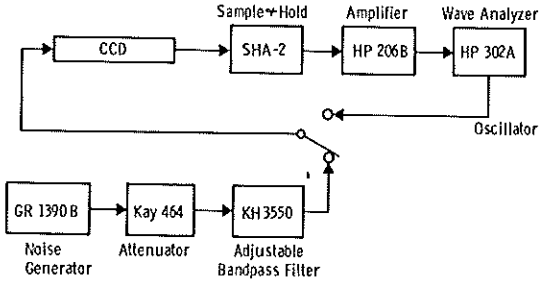

Fig. 4 EXPERIMENTAL SETUP FOR MEASURING FREQUENCY RESPONSE AND ALIASING CHARACTERISTICS

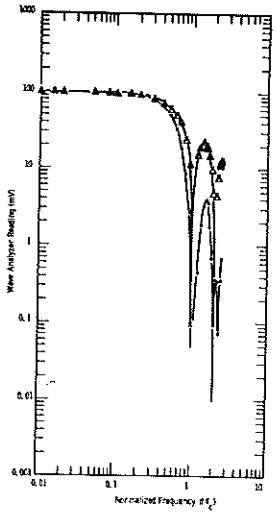

Fig. 5 MEASURED FREQUENCY RESPONSE OF CCD SYSTEM (INCLUDES $\frac{\sin x}{x}$ OF SAMPLE AND HOLD)

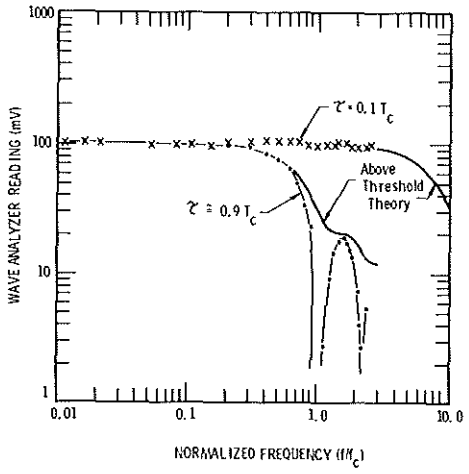

Fig. 6 REPLOTTED FREQUENCY RESPONSE WITH SAMPLE AND HOLD $(\frac{\sin x}{x})$ EFFECT REMOVED

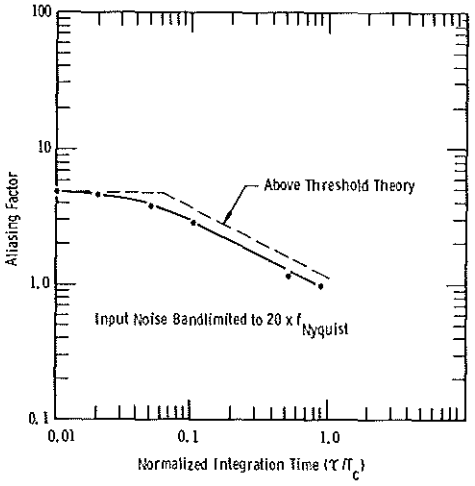

Fig. 8 MEASURED ANTI-ALIASING CHARACTERISTIC OF FLOATING DIFFUSION INPUT

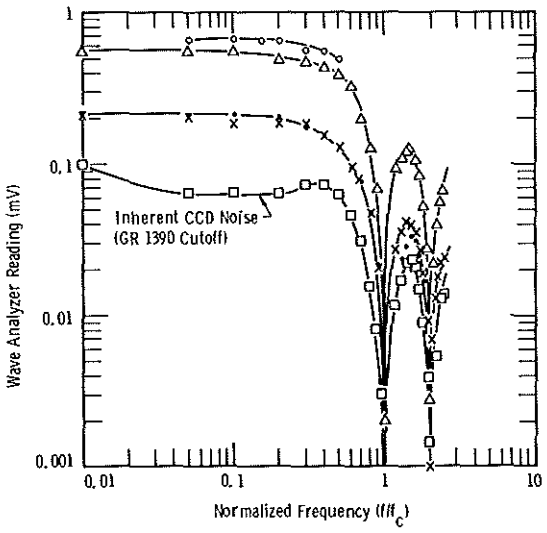

Fig. 7 MEASURED SPECTRAL INTENSITY OF NOISE VOLTAGE AT WAVE ANALYZER (INCLUDES sin x/x OF SAMPLE AND HOLD)