A SELF CONTAINED 800 STAGE CCD TRANSVERSAL FILTER

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ABSTRACT. CCD transversal filters are capable of high performance in a wide variety of filtering applications. To date the widespread application of CCD filters has been hampered by the complexity of peripheral external circuits required to operate the CCD. We have exploited the MOS/LSI compatability of CCD's to fabricate a completely integrated and self-contained 800 stage CCD transversal filter. The device is designed as a tunable bandpass filter with a 3 dB bandwidth of 0.7% of the center frequency and 40 dB sidelobes. A novel concept employing CCD structures as voltage amplifiers has been utilized in this device. Preliminary measurements of the device performance are presented.

I. INTRODUCTION

The tremendous signal processing capability of CCD transversal filters has been demonstrated in applications such as spectral filtering,[1,2,3] the chirp z transform,[4,5,6] and correlators for radar[7] and spread spectrum communication.[7] The relative simplicity of the split electrode tap weight technique[1] is the major reason for the versatility of CCD filters. However, a serious drawback to CCD filters used to date has been the complexity of external peripheral circuits required to operate the CCD. The full potential of CCD filters can only be realized by taking advantage of the MOS/LSI compatibility of CCD structures and integrating the required CCD support functions on the chip with the CCD. This paper deals with the design and performance of a fully integrated, 800-stage transversal filter chip which contains the CCD filter, its clock generator and drivers, an input amplifier, and an output amplifier as shown in Figure 1. On this CCD chip the clock waveforms are derived from a single master clock signal. The input and output amplifiers employ a charge coupled structure to achieve voltage amplification with low noise, high speed, and low power consumption. The device is designed so that only DC voltages and one master clock signal are required to be supplied externally. To facilitate analysis and testing of this prototype design, five different DC biases are required, but some of these levels could be derived on the chip in future designs. The weighting coefficients were designed for a tunable narrow bandpass with a 3 dB bandwidth of 0.7% of the center frequency and a -40 dB sidelobes. A simple reprogramming of two photomask levels would convert the filter to other correlator functions or to transfer functions such as lowpass, highpass, Hilbert transform or notch filters.

II. DESIGN

A) CCD STRUCTURE

Although CCD transversal filters can be constructed with two phase, three phase, or four phase CCD structures, we selected a three phase structure as a compromise between charge handling capacity, fabricational difficulty, overall size of the CCD, and clocking complexity. The device structure is an adaptation of the three metalization level, three phase CCD described by Bertram, et al.[8] In this case as illustrated in Figure 2 the device is fabricated with two polysilicon levels and one aluminum level. Each clock phase is on a sepa-

rate metallization level thus easing photolithographic requirements. As pointed out by Bertram et. al. this structure offers significant yield advantages for large CCD structures. Furthermore it simplifies layout of the electrode structure for the split electrode tap weighting technique. Each electrode is 0.3 mils by 6 mils with 0.05 mil overlap to adjacent electrodes. Thus each cell of the CCD is 0.9 mils by 6 mils. The packing density of this structure is higher than four phase and comparable to the packing density we could obtain with two phase structures of comparable charge capacity. Another advantage of the three level structure is that it allows the use of a four level sandwich consisting of the three metallization levels and an n+ diode diffusion to construct large capacitors in a minimum area. Two 300 pf capacitors were constructed in this way for use in the output circuit of the filter. The CCD is fabricated on 40-70 ohm cm p-type substrates with 1500A gate oxides.

The CCD has 800 stages and in order to achieve practical dimensions it is folded into four 200-stage segments. This technique of folding the CCD allows the CCD portion of the filter to be fabricated in a 200 by 60 mil area. The remainder of the 200 mil by 140 mil chip is devoted to the CCD support circuitry and test devices which are devoted to process monitoring.

Folding the CCD into four segments is made possible by the use of a diode and dc bias gate[5,6] as shown schematically in Figure 2. The basic principle of operation is that the corner diode is preset to fixed potential during each clock period by spilling charge over the dc gate. Once each clock period a new charge packet is introduced onto the corner N^+ diffusion from the preceding clock electrode ϕ_3, thereby lowering its potential below the threshold of the DC gate. Current then flows under the DC gate until the diffusion is restored to the threshold point at which time essentially all of the signal charge is transferred to the following clock electrode ϕ_1 and the diode is left at the same potential it had at the beginning of the cycle. Great care is taken to minimize the capacitance of the corner diffusion and minimize its charge transfer loss. Analysis of the corner leads us to expect the fractional transfer loss to be less than 1% at frequencies up to 10 MHz if a fat zero charge equal to 10% of a full CCD well is maintained.[6] Computer simulations of the transversal filter show that the effects of the corner loss at this level and below are negligible in the performance of the filter.

B) OUTPUT DIFFERENTIAL CURRENT INTEGRATOR

Realization of the full performance capabilities of CCD transversal filters places difficult requirements on the output amplifier circuit. As reviewed below, the split electrode tap weight technique requires a differential voltage amplifier having a high common mode rejection, high dynamic range, wide bandwidth, and good linearity. Low power consumption is also desirable particularly for very low frequency operation where chip heating would increase dark current and limit the useful delay time in the filter. Conventional linear MOS circuits are inadequate to meet these requirements and a new concept has been incorporated in this CCD filter design. The new concept utilizes a CCD structure as a differential voltage amplifier as described below.

We shall review the operation of the transversal filters constructed with the split electrode tap weighting technique. This review is followed by a discussion of the output amplifier circuit requirements. The amplifier design integrated on our chip is then presented.

The split electrode tap weighting technique[1] takes advantage of the fact that as signal charges are transferred along a CCD an image charge must flow into the clock electrodes. By splitting all of the phase two electrodes at various lateral positions along the CCD and measuring the difference in charge required by the clock lines driving the split electrodes we obtain the output signal. The differential charge at time nT_c is given by

$$q_{out}(nT_c) = \sum_{m=1}^{N} h_m C_e v_{in}(nT_c - mT_c) \quad (1)$$

where T_c is the clock period, N is the number of delay stages, and the sign and magnitude of each weighting coefficient h_m is determined by the position of the split in the electrode. The signal charge packet which is introduced at the input at $t=nT_c$ is $q_{in}=C_e v_{in}(nT_c)$ and C_e is the gate oxide capacitance of one CCD electrode. As Illus-

trated in Figure 3 the differential charge is measured by integrating the clock line current in series capacitors $C_I^{\pm}$ and amplifying the resulting differential voltage variations on the capacitors. The differential output voltage of the CCD filter which appears at the input of the voltage amplifier is related to the input signal by

$$v_o(nT_c) = \frac{1}{R\,NC_e} \sum_{m=1}^{N} h_m C_e v_{in} \quad (nT_c - mT_c) \qquad (2)$$

where

$$R = \frac{C_I^{\pm} + C_{\phi 2}^{\pm}}{NC_e},$$

$-1 < h_m < +1$, and $C_{\phi 2}^{\pm}$ is the total capacitance of each of the split phase clock lines. The gain required of the voltage amplifier depends on the gain factor of the CCD filter which is less than unity. This attenuation of the filter depends on the capacitance ratio R and the weighting coefficients or transfer function used in the filter. A small value of the integrating capacitors C_I increases the gain of the filter but attenuates the clock amplitude. We selected a compromise value of C_I = 300 pf to obtain a ratio R = 2.2. This value of R and the narrow bandpass weighting coefficients result in a filter gain of

$$\left| V_o/V_{in} \right| \approx 0.14 \qquad (3)$$

when the input signal at the passband frequency is

$$v_{in}(t) = V_{in} \sin(\pi f_c t/2). \qquad (4)$$

The designed gain of the differential voltage amplifier on this chip is G = 10 resulting in an overall gain $\left| V_{out}/V_{in} \right|$ = 1.4. Note that the differential voltage amplifier must reject the common mode 15V clock waveform. Also, if the filter is to be operated at frequencies up to a few megahertz the differential amplifier must have sufficient bandwidth to operate in this range.

The overall dynamic range is largely determined by the noise level of the output amplifier. The reason is that the CCD filter is an inherently low noise device. Furthermore, noise introduced at the filter input or internally generated in the CCD is filtered by the device. Stated differently, charge packets in the CCD due to the matched signal waveform add coherently in the filter output while noise charges do not. However, noise inherent in the output amplifier is not filtered by the CCD. The expected noise level of the CCD filter is on the order of 10 μV rms referred to the input of the output amplifier. This estimate includes input noise of the CCD, fast interface state noise, and the preset noise associated with driving the clock line capacitance. Therefore the wideband noise introduced by the output amplifier should be less than this level if the full dynamic range of the CCD is to be exploited. Assuming a signal bandwidth of 1 MHz the noise level corresponds to a spot noise spectral density of a few nanovolts/$Hz^{\frac{1}{2}}$. This goal is difficult to meet and as we shall see the output amplifier determines the output noise level.

C) CHARGE COUPLED DIFFERENTIAL VOLTAGE AMPLIFIER

The amplifier integrated on our IC was designed with the previously discussed requirements in mind. The amplifier is shown schematically in Figure 4. The amplifier is basically a one delay stage CCD with a differential input circuit and a standard precharge output[9] circuit. The inputs are applied to the gates labeled v^+ and v^- which correspond to the nodes with the same designation in Figure 3.

The input circuit of the amplifier utilizes a floating diffusion structure[10] which operates on a "fill and spill" principle[10,11,12] which is reviewed below. The amplifier described here makes use of the fact that the floating diffusion structure can be used with an inverting and a non-inverting input simultaneously to achieve a differential input. Also a metal gate was placed over the floating diode to increase its capacitance and minimize the contributions of the diode's nonlinear depletion capacitance.

Voltage gain is achieved by differentially presetting a large floating diffusion capacitor (C_1) with the input voltages and then transferring the charge to a smaller capacitance (C_2) at the output. The operation of differential input is illustrated in Figure 5. At the beginning of the input cycle the input diode is at a high positive potential (down on the potential energy plot in Figure 5b). When charge transfers under the ϕ_2 electrodes of the CCD filter, the differential output signal appears at v^+ and

v^- superposed on the ϕ_2 clock voltage. The input diode is pulsed to a low potential and then returned to its initial state. During this process electrons flow under the v^- gate and fill the surface under the v^+ gate and the capacitor C_1 (which is formed by diode diffusion under a dc biased gate). As the input diode is returned to the initial state electrons flow back to the input diode until the surface, potential on C_1 reaches the threshold of gate v^- and current stops. The surface potential profile at this time is illustrated in Figure 5b. Next the gate ϕ_2' is turned on, and electrons flow into the CCD well formed by the ϕ_2 electrode until the threshold of the v^+ gate is reached resulting in the surface potential profile of Figure (5c). This charge packet is then transferred in the normal way to the output node shown in Figure 4. The input charge is

$$Q_{in} = C_{in}(v^+ - v^-) \qquad (5)$$

where $C_{in} = C_1 + C_{v+}$ is the sum of the floating diffusion and the gate capacitance of the v^+ gate. The output voltage is

$$v_{out} = C_{in}/C_2\ (v^+ - v^-). \qquad (6)$$

Thus the gain of the amplifier is simply the capacitance ratio C_{in}/C_2. The amplifier was constructed with nominal values of $C_{in} = 3$ pf and $C_2 = 0.3$ pf for a gain of 10. Small non-linearities due to the depletion layer charge were neglected in (5) and (6). These non-linearities are small because: (a) the maximum signal swing for $(v^+ - v^-)$ is about 1V for the maximum signal level in the CCD filter. (b) these voltage changes are small relative to the back gate bias ($\sim$15V) which minimizes changes in the threshold due to changes in depletion charge under the gates, and (c) the high resistivity substrates used minimize the depletion charge effects.

Note that the operation of the amplifier requires a dc offset between v^+ and v^- so that a bias change of 50% of the charge capacity of the amplifier is injected in the absence of a differential signal. The amplitude of the clock waveform applied to ϕ_2' electrode in the amplifier must be a few volts greater than the waveform applied to ϕ_2 of the filter. We used 20V pulses on ϕ_2' and 14V pulses on ϕ_2.

All of the clock waveforms for the amplifier were derived from the clock waveforms required by the CCD filter. The total power required for the amplifier is approximately 20 mW. The speed of operation is determined by the rate at which the input capacitor C_1 can be preset by the gates v^+ and v^-. Following the results of Emmons and Buss[7] and using the standard MOSFET equation $I = \frac{\beta}{2}(V_{gs} - V_T)^2$, we can determine the time required to achieve the full gain of the amplifier. The condition to be met is

$$\tau q \gg \frac{C_1^2}{\beta/2} \qquad (7)$$

We shall assume a sufficient offset bias between v^+ and v^- such that $q \cong 6\times10^{-13}$ coulombs is the minimum charge injected. We have designed the input such that $\beta/2 = 5\times10^{-4}$. Evaluation of 7 reveals that $\tau \gg 30$ nsec is required. This condition is easily met at clock frequencies of 1-2 MHz or below.

The noise level of the charge coupled differential amplifier is dominated by the preset noise of the input capacitance C_{in}. There are two presets per input charge packet; one for the v^- gate and one for the v^+ gate. Each preset results in a variance of $(2kT/3C_{in})$ in the capacitor voltages.[9] The resulting rms noise voltage at the output of the amplifier

$$v_{out}^n = 10\left(\frac{4kT}{3\,C_{in}}\right)^{\frac{1}{2}} = 410\ \mu V$$

The maximum usable output signal of the amplifier approximately 2V rms. Therefore we expect a dynamic range of approximately 74 dB. The expected noise level of the amplifier is about 4 times greater than the noise generated in the CCD filter itself. Thus we have lost 12 dB of dynamic range due to the output amplifier noise.

Several advantages of the charge-coupled differential amplifier (CCDA) over a conventional differential MOSFET amplifier are summarized below. First the nature of the input circuit of the CCDA automatically performs a differential sample and hold operation. Use of an MOSFET amplifier would require sampling and holding of the v^+ and v^- voltages to avoid saturating the MOS amplifier with the large common mode clock signal. The gain of the CCDA is stable since it is determined by the ratio of two capacitances and is insensitive to

temperature or supply voltage fluctuations. Similar gain stability with an MOSFET circuit requires the use of high gain amplifier with feedback. The power requirement for the CCDA is approximately 20 mW as it is implemented in this filter. An MOS differential amplifier with similar bandwidth would require considerably more power particulatly if the gain were feedback stabilized.

D) INPUT AMPLIFIER

Since the output noise level is dominated by the noise in the output amplifier, it is desirable to introduce gain at the input of the CCD filter for low signal level applications. This procedure of course does not increase the dynamic range but rather scales both the minimum and maximum signal levels by the same amount. On this CCD filter we have included a charge-coupled input amplifier which operates similarly to the output amplifier. The gain of 10 preamplifier can be bypassed if the input gain is not needed. If gain is required at the input of a tarnsversal filter it is necessary to use linear voltage gain before the input of the filter. It is not desirable to achieve gain directly in the input of the CCD filter by the use of a large input capacitance such as the floating diffusion. The reason is that transversal filters utilizing split electrode tap weights require the use of an input in which the nonlinear contribution of the bulk charge under the tapped electrodes is exactly cancelled by the introduction of compensating charge at the input of the filter.[1,5] This compensation is accomplished by the use of the diode input scheme shown in Figure 6, in which the signal is applied directly to the input diode. A dc gate isolates the input circuit from the clock transients and the input is gated on and off by the ϕ_1 clock voltage which is applied to the first CCD transfer electrode. This input scheme results in a linear relationship between the input signal voltage and the filtered output signal voltage appearing on the integrating capacitors. Therefore, we drive the input diode of the CCD filter with the voltage amplifier when gain is required at the filter input.

E) CLOCK CIRCUITRY

An important step in fully integrating a CCD transversal filter is efficiently generating the clock voltages on-chip. The logic for our three-phase drivers is shown in Figure 7. The master clock C operates at twice the clock frequency and toggles the bistable flip-flop on each positive transition, generating Q and $\overline{Q}$. C is inverted and delayed through two series inverters to generate $\overline{C}'$. The clock phases ϕ_1 through ϕ_3 are generated by NOR-ing appropriate combinations of $Q,\overline{Q}$ with $C,\overline{C}'$.

The NOR gates and drivers are shown in Figure 8. When both inputs to the NOR gate are low, T_4 is on and the bootstrap capacitor $C_B(\approx 2$ pF) becomes charged positively, thereby turning on the driver T_6 and pulling ϕ_n toward 15 V. The bootstrap capacitor remains charged and keeps the pullup driver on even after the clock line reaches 15 V. When the following phase ϕ_{n+1} goes positive, the voltage on the bootstrap capacitor is discharged through T_5, thereby turning off the pullup driver; and the pulldown transistor T_7 is activated, thereby returning ϕ_n to ground. All clock circuitry is n-channel MOS with depletion loads and switching thresholds obtained by means of ion implants.

Advantageous properties of these drivers are (1) they provide three-phase clocks that overlap slightly at the crossover point; (2) they draw small quiescent power when they are not switching; (3) they present a low impedance to the clock line capacitance C_1 in both the ON and OFF state; and (4) they provide a 25%, 50%, 25% duty cycle for ϕ_1, ϕ_2, and ϕ_3 respectively. This last characteristic is advantageous for transversal filtering because when the ϕ_2 electrodes are tapped, the 50% duty cycle of the ϕ_2 clock gives a longer time to sense and sample the filter output.

F) WEIGHTING COEFFICIENT DESIGN

Another important design goal of this filter was to obtain a very narrow bandpass characteristic. In order to achieve this goal a large number of delay stages is required since the sharpness of passband to stopband transitions is inversely proportional to the length of the transversal filter. As a compromise between a very narrow response and a practical CCD size, a length of 800 delay stages was selected. A number of design techniques[13] have been developed for determining the weighting coefficients of digital finite impulse response (FIR) linear phase filters. These digital filter design techni-

ques are directly applicable to CCD transversal filters. The weighting coefficients for the 800 stage bandpass filter were designed using a computer program[14] which optimizes the weighting coefficients under the criteria of minimum sidelobe amplitude for a specified transition bandwidth from passband to stop band. This design algorithm results in equiripple sidelobes. The parameters used in out design resulted in a narrow bandpass filter with a center frequency at $f_o = f_c/4$. The width of the bandpass is $0.007 \times f_o$ at -3 dB and $0.017 \times f_o$ at -40 dB. The peaks of the sidelobes are uniform at -40 dB. Higher stopband attenuation could have been obtained at the expense of a broader bandpass.

The weighting coefficients are quantized in the photomasks due to the use of computer generated photomasks. In this CCD design, the weighting coefficients are coded into the channel stop level by placing a small region of p+ diffusion under the gap in the split electrode clock phase. With this technique, the weighting coefficients are defined with the resolution of the channel stop photomask and are therefore insensitive to small offsets in alignment of other photomask levels during the fabrication process. The expected resolution of the weighting coefficients is 0.3 to 0.6% of the maximum value. The filter with weighting coefficient quantization can be modeled as two filters in parallel one of which is the ideal filter and the other is an error filter having weighting coeffficients equal to the difference between the quantized weighting coefficient values and the ideal values.[5] Because the quantization errors are random, a good qualitative model of the spectral response of the error filter can be obtained by assuming a flat spectrum. The magnitude of the error filter frequency response has an expected rms value proportional to

$$\Delta H_{rms} = (\delta^2/12)^{\frac{1}{2}} \times N^{\frac{1}{2}} \qquad (9)$$

where δ is the relative quantization increment of the weighting coefficients ($\Delta h/h_{max}$). The peak response of the ideal bandpass filter is proportional to

$$Ho = \frac{1}{2\Delta f/f_c} \qquad (10)$$

where $\Delta f/f_c$ is the ratio of the 3 dB bandwidth to the clock frequency. Combining (9) and (10) we obtain the relative contribution of the error filter

$$\frac{\Delta H_{rms}}{Ho} = \frac{\delta}{\sqrt{3}} \left(\frac{\Delta f}{f_c}\right) N^{\frac{1}{2}}. \qquad (11)$$

Evaluating (11) for the 800 stage bandpass filter with a weighting coefficient quantization of $\delta = 0.5\%$ yields an expected error response of -76 dB. Thus we do not expect to see the effects of weighting coefficient quantization in the transfer function of this filter.

III. EXPERIMENTAL RESULTS AND CONCLUSIONS

Preliminary evaluation of the performance of these devices is presented here. The frequency response of the filter is very close to the design as presented in Figures 9 and 10. The response curves shown in Figure 9(a) and 9(b) were obtained with clock frequencies of 100 kHz, where the bandpass center frequency is 25 kHz and the 3 dB bandwidth is 0.7% of the bandpass or 175 Hz. The highest sidelobe response is about -37 dB which is 3 dB higher than the design value of -40 dB. The small deviations in the sidelobe response from the design level is caused by a spurious feedthrough of the input signal to the output at a level about -55 dB below the bandpass peak response. The feedthrough response has a different phase relationship to different sidelobes, thus it adds constructively to some and destructively to others. The path of this feedthrough signal is being investigated. Similar performance is observed at a clock frequency of 1 MHz as shown in Figure 10. As expected the bandpass center frequency scales to 250 kHz and the bandwidth to 1.75 kHz. The highest sidelobes are -36 dB and as above the deviation from the ideal characteristics results from the spurious direct feedthrough of the input signal to the output.

The measured gain of the overall filter is approximately 0.56 (-5 dB insertion loss) at the bandpass center frequency. As described in Section II a gain of 1.4 (+3 dB) was expected for the ideal filter. Part of the attenuation can be accounted for by the effects of charge transfer inefficiency. Measurements indicate that these devices typically have charge transfer inefficiency ranging from $\epsilon = .00025$ $\epsilon \approx .0003$. The effect of transfer inefficiency is to attenuate the frequency response by the factor[6]

$$A(f) = e^{-\frac{N\epsilon}{2}} (1 - \cos 2\pi f/f_c) \quad (12)$$

which reduces the bandpass frequency by about 3 dB with the observed values of ϵ. Another 3 dB attenuation results from a measured capacitance ratio of R = 3 instead of the design value R = 2.2 used in (12).

The measured voltage gains of the differential voltage amplifier and the input voltage amplifier were each approximately G = 9 at both f_c = 100 kHz and f_c = 1 MHz. At a signal voltage level of 1 V^crms at the output of the input amplifier, the second a and third harmonics were -40 and -50 dB respectively. Since the two amplifiers are constructed identically the same characteristics should apply to the output amplifier as well.

Detailed measurements are under way to determine the noise, linearity, frequency range, and power requirements of the entire filter. The preliminary results above indicate that performance consistent with design goals will be achieved.

ACKNOWLEDGEMENTS

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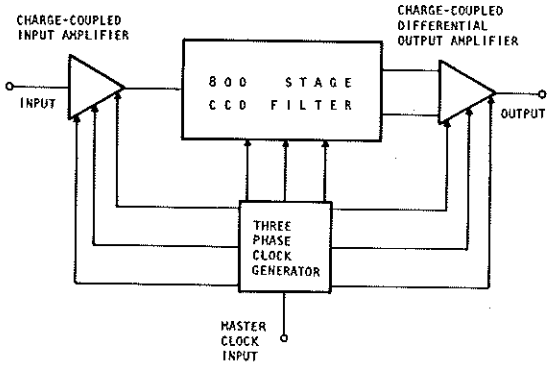

FIGURE 1. Block diagram of the 800 stage CCD transversal filter.

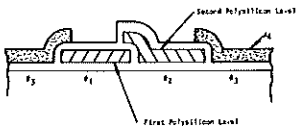

FIGURE 2. Electrode structure of the three metalization three phase CCD.

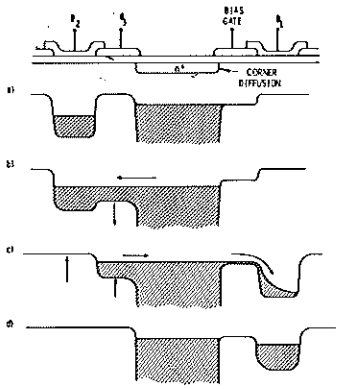

FIGURE 3. Schematic of the operation of the CCD corner showing the surface potential at various stages in transfer.

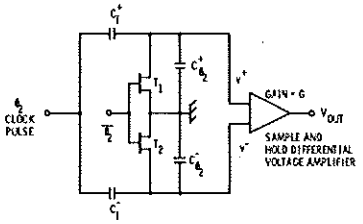

FIGURE 4. Schematic of the differential current integrator showing the clock line current integrating capacitors $C_1^{\pm}$.

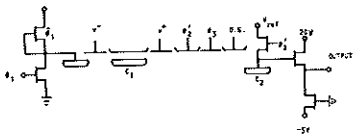

FIGURE 5. Schematic of the charge-coupled differential amplifier (CCDA). A large capacitor C_{IN} is used to transfer an amount of charge C_{IN} $(v^+ - v^-)$ to capacitor C_2 giving a gain $G = C_{IN}/C_2$.

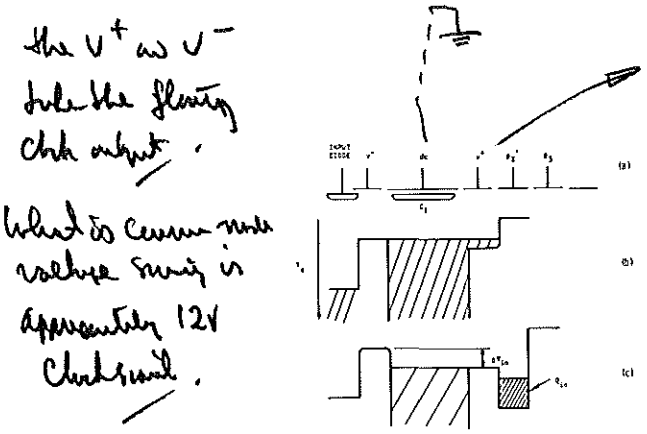

FIGURE 6. Potential energy diagram demonstrating the operation of the charge-coupled differential amplifier. An amount of charge $Q=C_{IN}(v^+ - v^-)$ is transferred into an output diode having capacitance C_2, thereby resulting in an output voltage $V_{out} = C_{IN}/C_2 (v^+ - v^-)$.

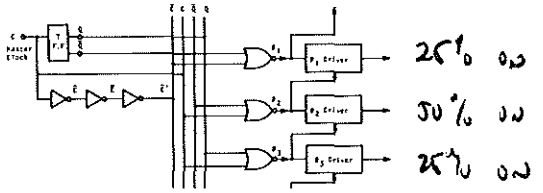

FIGURE 7. Timing and logic to generate three-phase clocks. Phase 2 has a 50% duty cycle while Phase 1 and Phase 3 each have a 25% duty cycle.

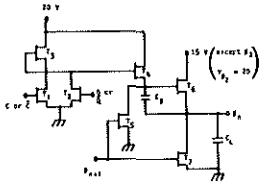

FIGURE 8. Clock Line Drivers

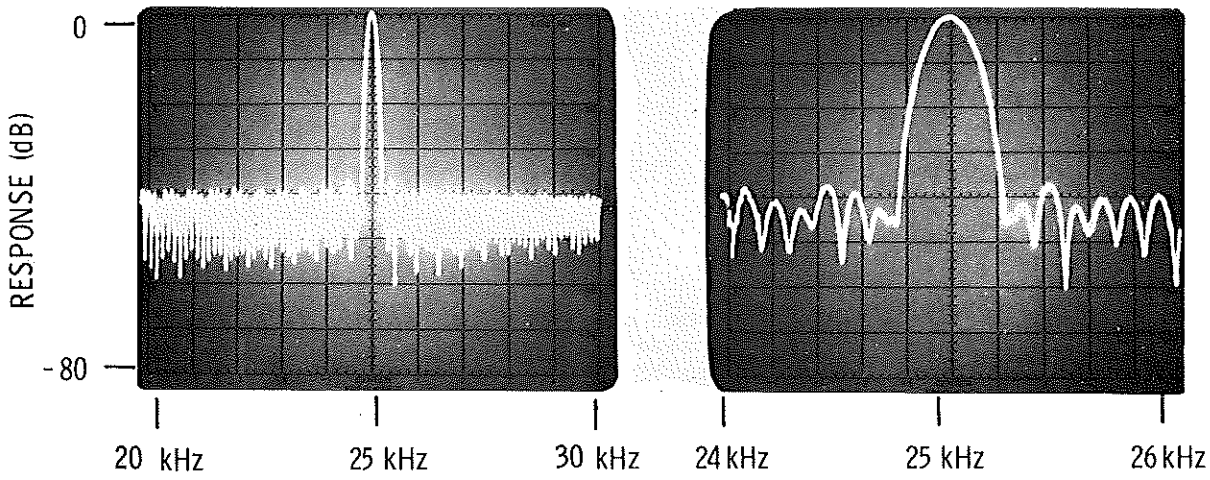

FIGURE 9. Frequency response of the 800 stage CCD filter operated at a clock frequency of 100 kHz.

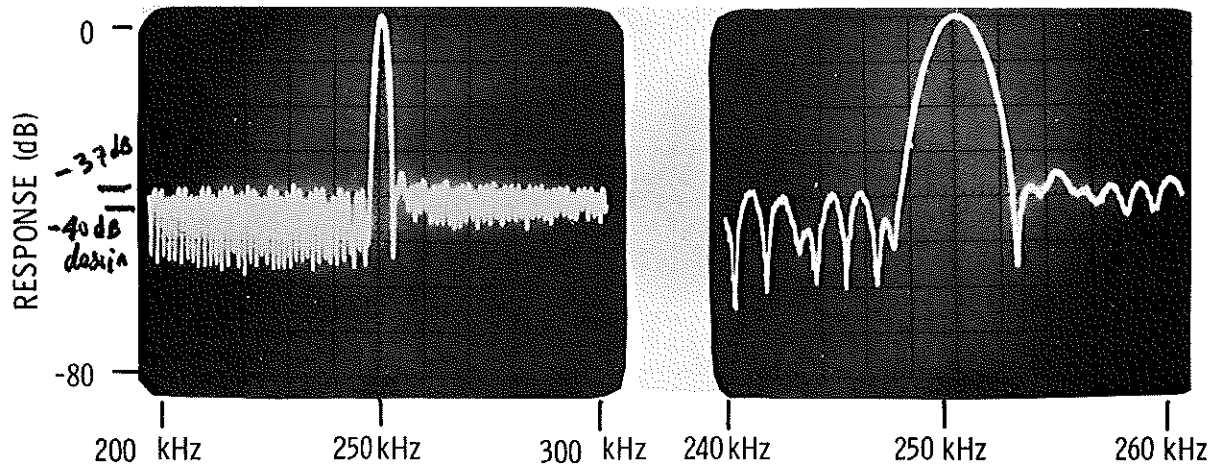

FIGURE 10. Frequency response of the 800 stage CCD filter operated at a clock frequency of 1 MHz.