A CCD-SAW PROCESSOR FOR PULSE DOPPLER RADAR SIGNALS

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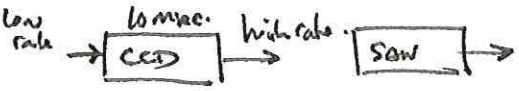
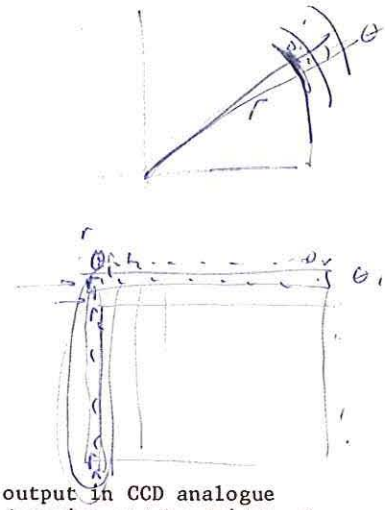




ABSTRACT The use of different clock rates for data input and output in CCD analogue signal processors provides a convenient means of adjusting the duration and bandwidth of signals to suit subsequent operations. This feature can be usefully incorporated into a CCD analogue store for radar data which is also designed to re-order the data sequence for doppler-frequency analysis using surface acoustic wave chirp filters. The combination of msec storage times available with CCD and the precision high-speed processing of SAW devices, made compatible by the flexibility of CCD time scales, provides a powerful capability for high resolution multi-channel frequency analysis involving comparatively simple hardware which can accommodate a range of radar parameters.

INTRODUCTION

A coherent pulse radar signal contains much information which it is usually uneconomic to extract because of hardware size and complexity. In particular, it is advantageous to resolve the doppler frequencies of targets even when their velocities are not required because narrowband detection excludes much of the noise (or jamming) which tends to obscure the target. Full doppler processing of this kind requires a bank of many narrow (eg tens of Hz) band filters for each resolved range cell or some equivalent hardware, for example using digital Fourier transformation. Such processing is rarely implemented because of the complexity and cost of existing methods but it now appears that the advent of CCD and surface acoustic wave (SAW) signal processing methods may change this situation, allowing a processor to be built up to suit a given requirement (specified in terms of pulse repetition frequency (prf), number and size of range cells and number of pulses to be coherently processed) from fairly simple standard modules.

The basis for this is that the established capability of SAW spectrum analysers using 'chirp' filters (linearly dispersive delay lines) can be applied to radar doppler analysis by time-compressing the data using a CCD. This expands the bandwidth and shortens the duration by a factor of order 1000 so that these parameters are brought within the scope of SAW processing. The CCD store can also be configured so as to separate the incoming data stream into sequences from different range cells, for individual spectral analysis. Because of the shortened time scale, data from many range bins can be analysed in a time equal to the accumulation period. The duration of the CCD output streams are matched to the fixed length of the SAW filters but the input rate is set by the radar pulse repetition rate (prf) and range cell spacing.

ARCHITECTURE OF THE PROCESSOR

The CCD data store required is a serial-to-parallel arrangement schematically shown in Fig 1. The input accepts a video signal as discrete analogue samples clocked into the upper (serial) CCD register during the strobed time interval following the transmission of a radar pulse and corresponding to the range interval of interest. For simplicity we will assume that 1 sample per range gate interval is used (2 would allow more protection against range straddling loss). After the serial acquisition of data from each radar pulse, the serial clock is stopped and the clock for the parallel registers taken through one cycle so that

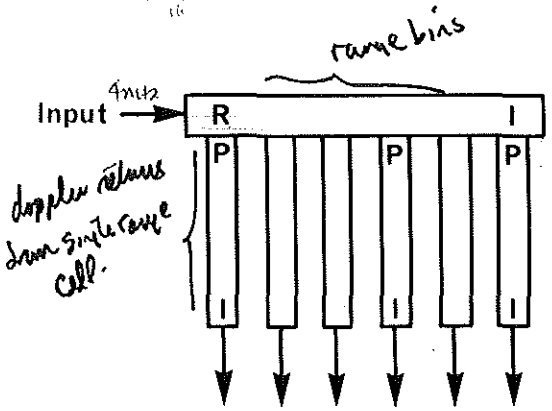


Fig 1 Storage Format

the latest samples enter the top of the parallel stacks. After a number of radar pulses, these each contain the history of the video amplitude corresponding to a particular range.

In the simplest mode of operation, a data matrix is filled containing RP samples from P radar pulses and R range cells, the input is inhibited or directed to another similar store, and the stacks are clocked in turn to output the data streams at high speed for rapid spectral analysis. Frequently only a restricted proportion of the pulse repetition interval, T, is to be analysed so that some dead time is available between pulses during which the readout of one parallel register can occur. In this case the Doppler frequency processing for successive range cells is based on slightly offset time windows. For the particularly simple case of R = P each range store is just filled as its turn for readout occurs. If P>R then each new cycle of readouts has to await the refilling of the store while if P<R, more than one range readout is necessary between radar pulses to avoid losing data.

The output data is put through a sample-hold circuit to strip off the unwanted clock transients and presented to the spectrum analyser. Since only the power spectrum is required, this takes a simple form built around two 'chirp' or linear FM filters. The first is impulsed to generate a chirp signal at a convenient IF which is mixed with the signal to form the input for the second chirp filter.

The second filter acts as a pulse compressor for each frequency component of the original signal, delivering an amplitude peak delayed in time proportionally with the input frequency. The detected output then represents

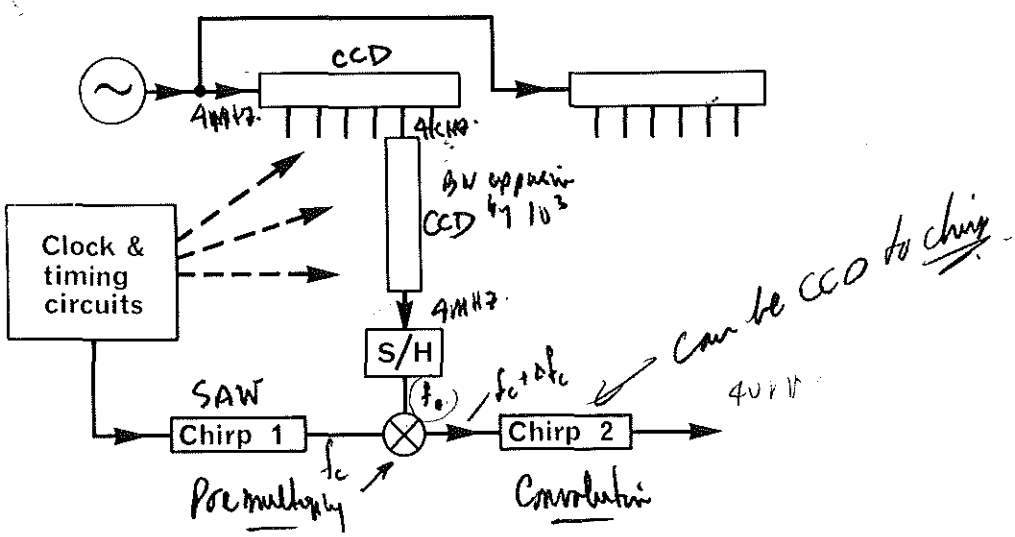


Fig 2 Experimental Configuration

TI does parallel processing instead of data store.

the essential difference between this approach and the TI chirp-z approach is the use of a real time, high-speed spectrum analyser with a data store and conversion method to provide the data to a SAW or CCD which generates a chirp waveform to perform the chirp-z by a chirp deconvolver.

the amplitude-frequency spectrum of the input signal from one range interval and threshold detection can be applied. The noise against which the signal competes is limited to that within the resolved Doppler bandwidth which is of order $(P\ T)^{-1}$ and the time of threshold crossing can be interpreted in terms of the target radial velocity.

EXPERIMENTAL VALIDATION

Available components have been assembled to establish the feasibility of the CCD-SAW approach. A 100-sample linear CCD has been used to store data in a way representing a single range cell system. Fig 2 shows how the data is fed to the store from a tapped analogue delay line which receives the radar bipolar video signal. The choice of tap used represents the radar range examined (the first tap corresponding to the furthest range cell). Each tapped line is clocked at 4 MHz, corresponding to a range cell spacing of about 40 m, in bursts repeated at 4 kHz (the simulated prf). Following each burst the CCD store is clocked once until, after 100 cycles, it is filled with new data. At this point 100 clock cycles are applied at 4 MHz to read out the store into the spectrum analyser. Readout takes only 25 µs and therefore can be fitted in during an inter-pulse period of 250 µs provided that less than 90% of the unambiguous radar range is being processed.

Key point.

The time compression of 1000 (25 ms: 25 µs) expands the bandwidth so that a spectral resolution of ~ 40 kHz, achievable with SAW processing, becomes adequate since it corresponds to 40 Hz for the real-time signal. The unwanted clock waveform components present in the CCD output are removed using a sample-hold circuit so that a reasonably smooth signal is presented to the spectrum analyser. The spectrum is derived using the principles given by Edwards and Withers (1), here using dispersive SAW filters both to replace the active swept oscillator and to provide the pulse compression which separates the spectral components of the signal.

An impulse to the first SAW filter produces a chirp signal at a convenient IF, starting at the same time as the CCD output. The mixer then outputs chirp signals offset by frequencies $\pm f$ for each frequency component f of the CCD output. The second SAW disperser, having an impulse response with the same frequency-versus-time slope but opposite sign, acts as a pulse compression filter: each offset chirp giving rise to a peaked output with a time delay proportional to f.

Fig 3 makes this clearer for the case when only one component, at frequency f, is present and the second filter, chirp 2, has twice the bandwidth W of the generated chirp in order to accommodate frequency shifts due to input signals within a bandwidth W without amplitude loss. It will be seen that the time sidelobe levels are increased by the proximity of the image component peaks. This can be avoided by first mixing the baseband signal to an IF of at least W, enabling the lower sideband from the mixer to be suppressed by filtering as described by Edwards and Withers.

The present experimental system is below optimum in many respects but the means of improving its performance are at hand. The single range cell limitation can be overcome by adding more CCD storage elements and it should be noticed that the serial-to-parallel section can be extended indefinitely as in Fig 2 using suitably clocked tapped lines rather than a single longer one. The direct CCD output to the mixer will be replaced by a multipole analogue switch and the timing circuits elaborated to sequence the operations. Up to the present SAW filters designed for other purposes have been used: an amplitude weighted chirp 1 with 2 MHz dispersion over 20 µs (not 25 µs) has been combined with a similar but unweighted filter for chirp 2. The Taylor weighting is desirable to reduce the spectral sidelobes but its effect is vitiated by the inadequate bandwidth of chirp 2 which does not accommodate frequency shifted signals, thereby losing signal energy, worsening the spectral resolution and abruptly truncating the weighting function. A special purpose pair of filters will shortly be available to overcome these disadvantages.

Fig 4 illustrates the important waveforms in the existing system. Trace (a) shows a simulated video input to the analyser, a sinusoidal signal representing a target doppler frequency of 200 Hz. After the clocking-in sequence, each terminal of the tapped line holds an amplitude sample for a particular simulated range ready for input to the CCD store. Trace (b) shows the output from one such tap. The samples

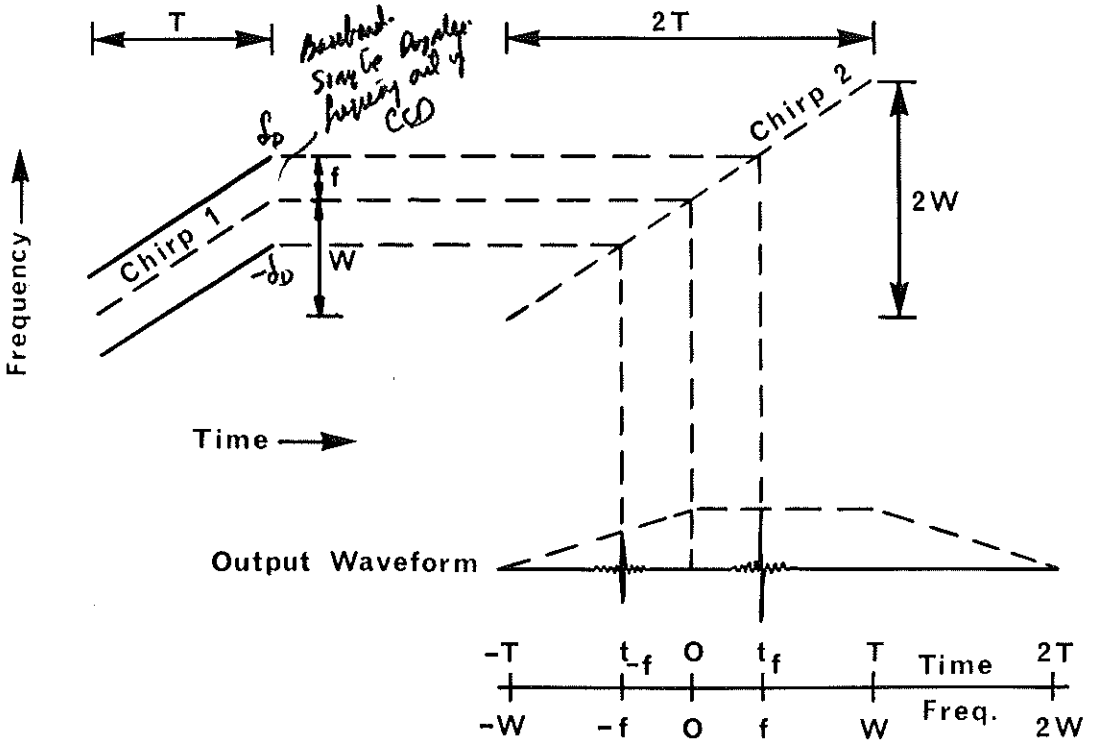


Fig 3 Time-Frequency relations for Spectrum Analyser

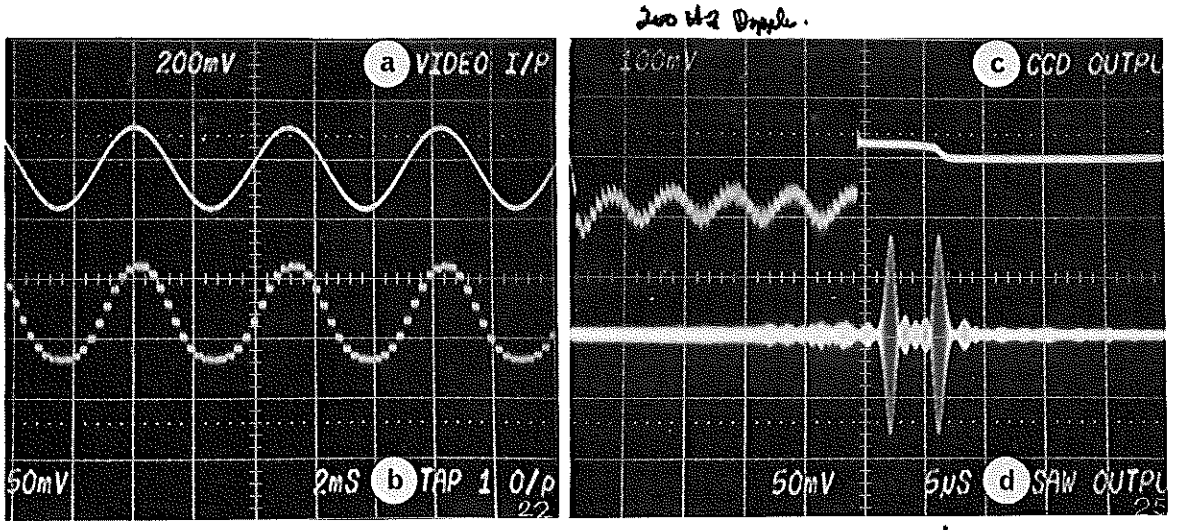
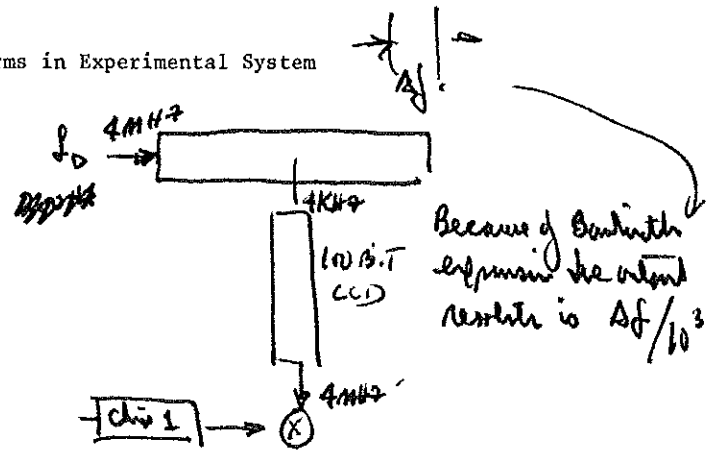


Fig 4 Waveforms in Experimental System



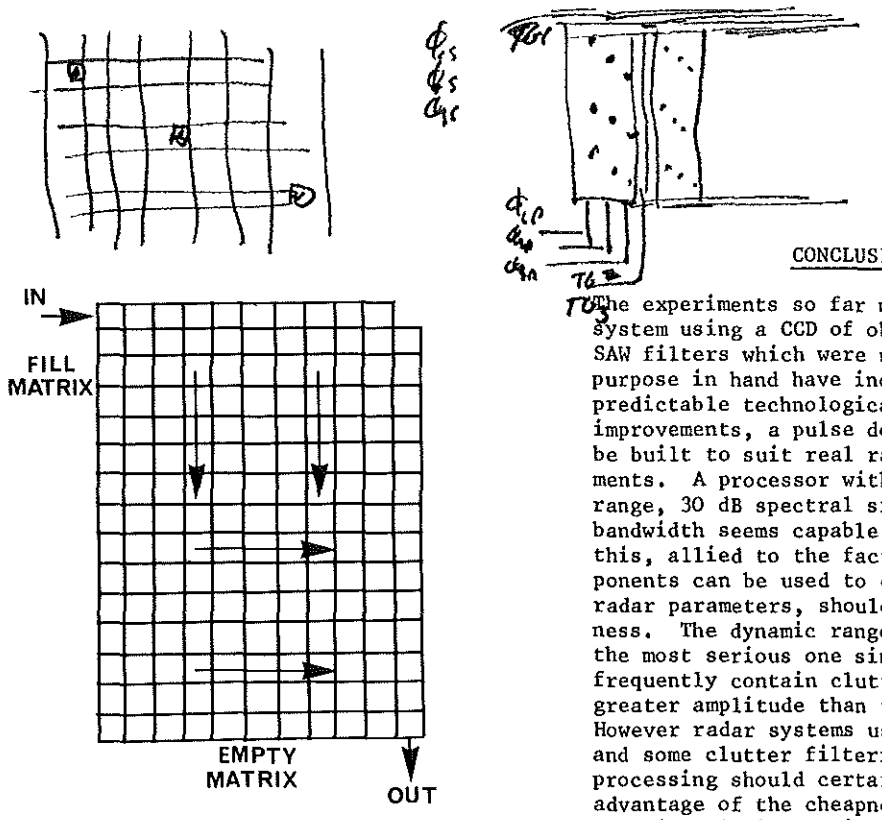


Fig 5 Integrated Storage Module Concept

corresponding to a particular range are transferred to the CCD store by a single cycle of the 4 kHz input clock. When the CCD store is filled, a burst of 100 clock cycles at 4 MHz is applied to empty it, producing the active section of waveform (c), the time-compressed range gated video in a form compatible with the SAW analyser. Some distortion of the ideal sinusoidal trace is evident. This is expected to improve in the next generation of devices but even this degree of distortion does not prevent the spectral peaks being easily distinguished in the spectrum output (d) from the SAW analyzer. The two main peaks correspond to the upper and lower sidebands of chirp 1, both are of equal amplitude because the up and down-shifted chirps have both moved partially outside the bandpass of the compression filter, by equal amounts in opposite directions. Zero frequency of the input spectrum corresponds to the point midway between the peaks. The first peak is in a region that would normally be suppressed by time gating in a real system context. The spurious frequency sidelobe levels arise from the signal distortions within the CCD and from the upsetting of the Taylor weighting of chirp 1 by the use of too short a compression filter (chirp 2).

CONCLUSIONS

The experiments so far made with a skeleton system using a CCD of obsolescent type and SAW filters which were not designed for the purpose in hand have indicated that with predictable technological and design improvements, a pulse doppler processor can be built to suit real radar system requirements. A processor with 40 dB dynamic range, 30 dB spectral sidelobes and 10 MHz bandwidth seems capable of achievement and this, allied to the fact that standard components can be used to cover a range of radar parameters, should ensure its usefulness. The dynamic range limitation may be the most serious one since radar signals frequently contain clutter echoes of much greater amplitude than the wanted targets. However radar systems using swept gain (STC) and some clutter filtering prior to doppler processing should certainly be able to take advantage of the cheapness and flexibility of this relatively simple processor.

FURTHER DEVELOPMENT

We have described a processor conceived in terms of discrete component CCD elements combined to form an analogue storage matrix with orthogonal and dual speed input/output. This function is strongly reminiscent of the serial-parallel-serial CCD which suggests that an integrated circuit form of orthogonal input/output store might be possible. The difficulty is in building in sufficiently flexible clocking controls so that the contents of individual range stores can be accessed one by one without disturbing the others. The attractions of using such an integrated store are such that we are developing one storing data from 100 pulses and 10 ranges which will effectively do this by right-shifting the whole data matrix as indicated in Fig 5 so as to successively bring columns of data into a fast readout register with independent clock control. The freedom to move the matrix either vertically (during input) or horizontally (for output) demands a new type of clock line structure, a possible one using a two-level polysilicon process with an aluminium overlay being proposed elsewhere (2). The storage module will allow coherent processing of data from up to 100 radar pulses. If the requirement is smaller than this (it is usually limited by the number of pulses

directed on to a target by a scanning beam), storage capacity can be wasted merely by clocking the CCD output at a rate which matches the duration of the data to the length of chirp 1, and impulsing the chirp only when real data begins to appear. The required number of range cells is accommodated by using sufficient storage modules, each being clocked in sequence for input and output.

The integrated circuit architecture is incompatible with the interleaved input/output scheme described previously so that a duplicate store is required, one acquiring data while the other is read out for analysis, nevertheless there should be a worthwhile saving in package count compared with the discrete CCD version.

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