MULTIPLE FILTER CHARACTERISTICS USING A SINGLE CCD STRUCTURE

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ABSTRACT

The split electrode approach to the design and implementation of on-chip tap weights has been generalized to obtain several types of filter functions using a single CCD delay line. The concept was used to implement two types of transversal filters using a 32 stage 2 phase CCD delay line. The ϕ_1 storage electrodes were split to obtain a low-pass filter whereas the ϕ_2 storage electrodes were split to obtain a bandpass filter.

The design and operation will be described and the theoretical and experimental characteristics will be compared. An analysis of the tap weight errors introduced by design layout aids will be presented. The advantages and limitations of this technique will be compared to the single filter approach.

INTRODUCTION:

The use of CCD's in transversal filter applications have been discussed in the literature[1-5]. In all these studies a single CCD delay line was used to obtain a single type of filter frequency response. Although different CCD structures and technologies have been used in the implementation, the design principles are similar. The on-chip tap weights were achieved by splitting one of the CCD storage electrodes of every delay stage. The tap weight values were obtained by varying the split location along the channel width and differentiating between the charge signal on the two outputs. The output was obtained either by floating gate voltage sensing[2], or current sensing methods[1,4]. The trade-off between the two methods are in the linearity and dynamic range of the filter output. Using these approaches lowpass, bandpass and highpass filters have been fabricated. Typical filter parameters of 50dB rejection in the stopband, ripples of less than 0.2dB in the passband and linearity of 50dB were experimentally obtained.[2,4]

The purpose of this paper is to discuss the performance of CCD transversal filters where a single CCD was used to obtain two different types of filters.

DEVICE DESCRIPTION

Figure (1) shows a schematic diagram of the structure as applied to the two phase CCD's. As shown, not only ϕ_1 storage electrodes are split to form one type of filter function but also ϕ_2 storage electrodes are split to obtain another type. Each clock phase has a positive and negative output. The circuit was designed to operate with the floating gate voltage sensing technique as shown in Figure (2a). Figure (2b) shows the timing diagram for the circuit operation. For signal sensing under ϕ_1 electrodes, ϕ_1 goes high and the potential of the floating gates increases positively until $\phi 13$ is applied. Through bootstrap action, the potential at A becomes stable and the electrodes are left floating. At this point ϕ_2 goes low and charge is transfered to the floating gate causing a drop in the surface potential. This change is measured at the source follower output using sample and hold pulse ϕ_{1S}. A similar reset and sample and hold timing scheme is applied on ϕ_2 floating gate

electrodes.

Figure (3) shows the test chip used to evaluate the structure. It consists of 33 stages of CCD delays. A 32 tap lowpass and 32 tap bandpass filters were implemented under ϕ_1 and ϕ_2 storage electrodes respectively using split electrode technique. The 33rd stage was used to monitor the output charge signal for efficiency of transfer measurements. The structure was fabricated using n-channel two-level polysilicon gate technology on 3 Ω cm p-type silicon substrate. Input and output logic and timing circuitry were fabricated on the same chip using n-channel MOS transistors. Also protection against surge pulses were fabricated on the address lines.

At the split in each electrode a floating diffusion was used to couple the two channels under the positive and negative sections. Thus the surface potential across the channel will be equal. In the current sensing method, where a constant voltage is maintained on the gate, the diffusion will equalize the charge density in both sides and consequently when the next transfer occurs the charge will split according to the new capacitive ratio. The charge equalization could have been established during the transfer process if a true four phase clocking system had been used. However, in the devices discussed here, the sample & hold pulse has to occur as shown in Figure 2(b), immediately after the charge transfer, so that the voltage change is measured before surface potential equalization can be established.

A LINFIR (Linear phase impulse response) program, which is an adaptation of the Parks, McClellan and Rabiner[6] program, was used for the design and performance measurement of Linear phase transversal filter. Also a MCPOST (Monte Carlo post processor) program was used to analyze the effect of random tap weight errors. The layout and process errors have been compensated for, using inhouse developed CAD program. Figure (4) shows the impulse frequency response of the two filters.

The operation will be described and the theoretical and experimental characteristics will be compared. An analysis of tap weight error introduced by design layout aids will be presented. The advantage and limitation of this design technique will be compared with the with the single filter approach.

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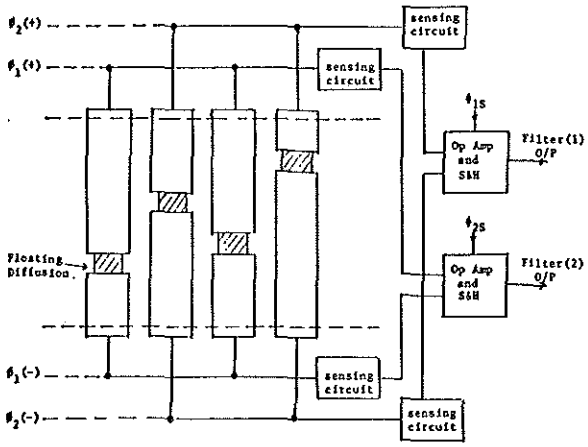


FIGURE 1 - Implementation of split electrode approach under ϕ_1 and ϕ_2 storage electrodes.

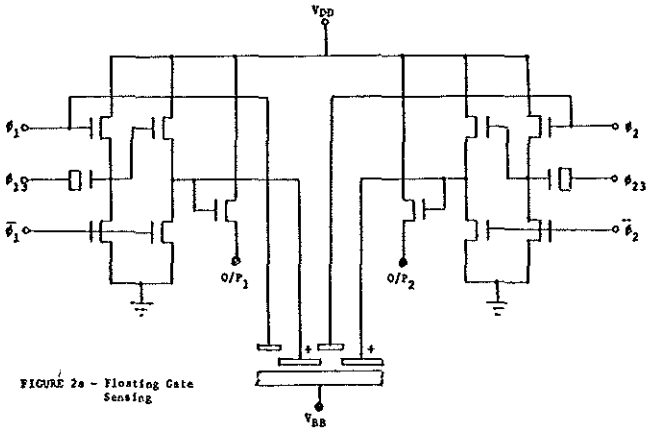


FIGURE 2a - Floating Gate Sensing

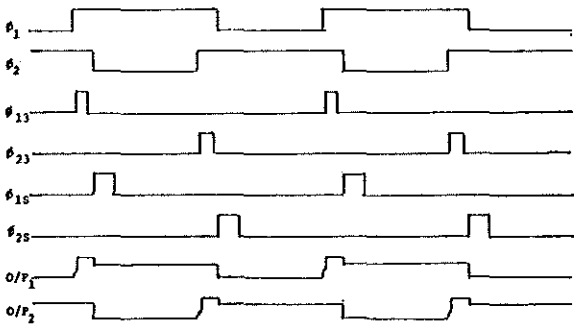


FIGURE 2b - Proposed Timing Diagram

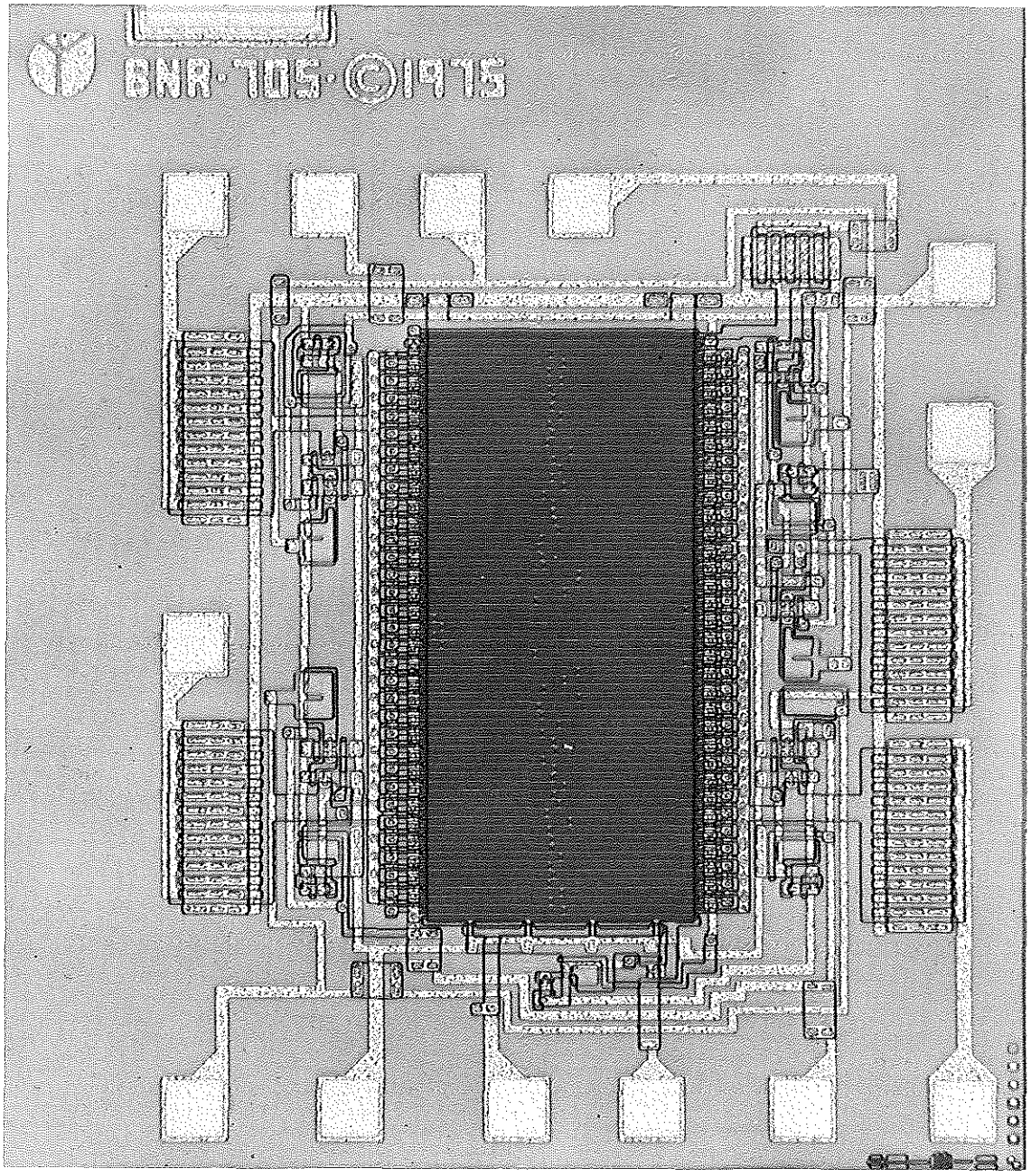
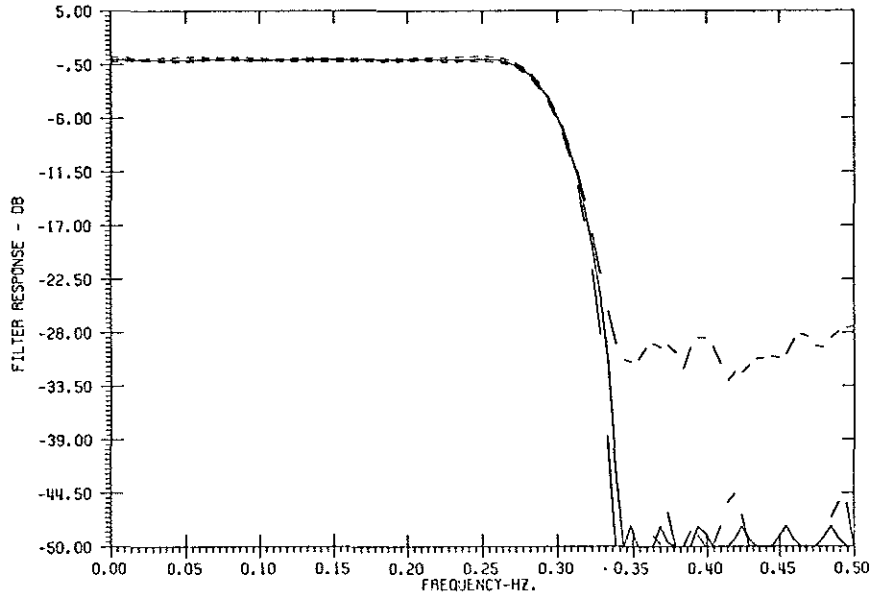


FIGURE 3 – FABRICATED TEST CHIP



C.C.D. TRANSVERSAL FILTER RESPONSE
SOLID LINE = IDEAL RESPONSE
BROKEN LINE = WORST CASE MONTE CARLO

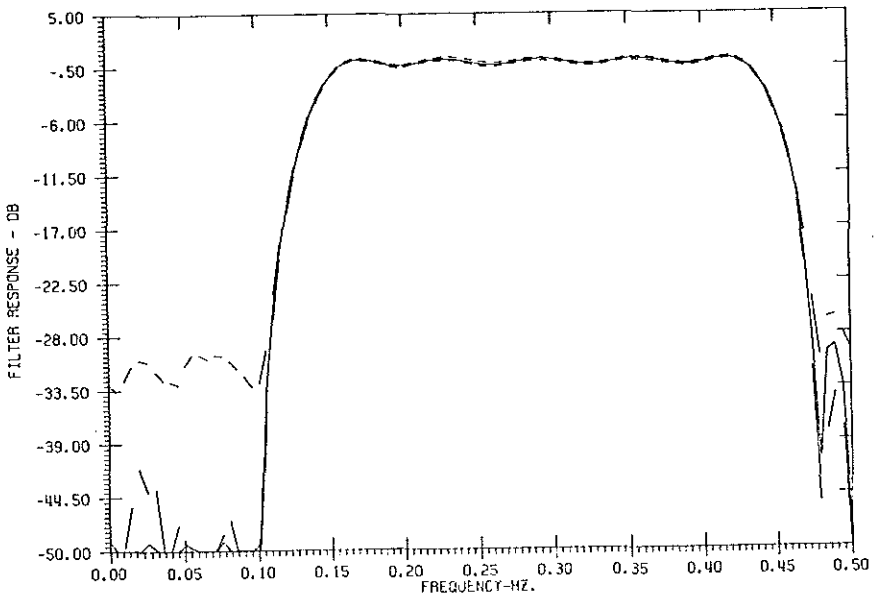


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FIGURE 4 - SIMULATED FREQUENCY RESPONSE