ANALOGUE CORRELATORS USING CHARGE COUPLED DEVICES

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ABSTRACT

One of the desirable objectives in the development of CCD signal processing devices is to produce a fully integrated analogue cross-correlator. A processor with a code storage capability of, say 32, samples would meet a range of requirements. The ability to cascade such processors allows extended system applications. This paper reports on two developments towards such a processor, the construction and operation of a hybrid cross-correlator and the design of a 32 bit integrated correlator chip.

HYBRID CORRELATOR

User provides Reference Code

The CCD is capable of sampling and storing analogue signals using a shift register action. When this function is combined with non-destructive tapping circuitry feeding into analogue multipliers, then it is possible to perform real time cross-correlation of analogue signals. A processor of this form is shown schematically in figure 1.

A hybrid correlator was assembled using two CCD's each using 8 taps, the respective tapped signals were fed into separate monolithic multipliers and the products were then summed in an operational amplifier. The CCD's were constructed using a simple single level aluminium structure with etched gaps 2-3 microns wide. They were three phase surface channel devices using an n-type substrate. A floating gate reset technique[1,2] was used as the basis of the tap circuitry.

The analogue multipliers used were of type MC 1594 L. The maximum bandwidth of these multipliers is 0.8 MHz and it has a linearity of 0.5%. The summing function was performed using an operational amplifier, type LH0032CG, with a slew rate of 500 V/μS. The summed output was then fed into a sample and hold circuit type DMC 651. This device produces considerable transient noise due to logic feedthrough, limiting its dynamic range to 22 db.

The ability to make use of the full performance of the CCD is obviously constrained by the performance of the peripheral circuitry. If the CCD has a dynamic range of m:1 then the multiplier needs to be capable of processing a signal range of m^2:1 and the amplifier a range of nm^2:1 if there are n taps.

The maximum bandwidth of the correlator was limited by the multipliers to 0.8 MHz. At the output of the correlator the maximum observable signal was limited by the feedthrough in the sample and hold circuit, reducing the dynamic range from 30 db at the output of the CCD to 20 db at the output of the sample and hold.

The storage time for the reference channel of the processor was limited by dark current in the CCD to the order of a few milliseconds. Very much larger storage times (many seconds) are theoretically possible and times of 100 msecs are typical experimentally.

TV LINE CORRELATION

The processor described was used to correlate a portion of one television line

with the remaining lines of the same television frame. The video output from a CCD camera was fed into an interface unit which had controls to select any portion of the TV frame. The selected signals were stored in the reference channel and held constant by inhibiting the clock waveforms to the reference channel. The lines succeeding the reference line were then passed through the signal channel of the processor and correlated with the stored signal. A two dimensional picture could be built up by feeding the output to a monitor as shown in figure 2a. The upper trace is the reference line correlated with the reference signal (the reference signal is only part of the reference line). Successive lines on the display show the correlation function from successive TV lines correlated with the reference signal. For simplicity, only 16 lines have been displayed. An alternative method of display is to use the correlation output to intensity modulate a raster scan synchronised to the TV frame.

The performance of the correlator was measured using a test pattern, consisting of eight grey levels, one per reference sample, offset by one bit on each succeeding line, and repeating after 8 lines. The correlator display from this test pattern is shown in figure 2a and the theoretical correlation functions are shown in figure 2b.

This form of one-dimensional correlator can be extended to perform two dimension spatial correlation for images which are available as raster scanned video. This is illustrated in figure 3 where a sub-frame taken from a complete TV frame may be correlated with other portions of the picture, perhaps over the duration of several frames, to detect the magnitude and direction of movements of objects in the field of view.

The video is clocked through the reference and signal channels of M correlators in cascade, with discrete time delays interleaved, so that each correlator-plus-delay stores the L elements of a complete TV line (or as much of it as needs to be processed). The clock waveform to the reference channel is inhibited when a complete line is stored. At that time the M correlators between them hold the NxM sub-frame to be compared with the rest of the complete frame. The correlation output will now show a maximum but as the video continues clocking through the signal channels, the correlation will fall off as the picture decorrelates in the horizontal dimension, until a new video line enters the system. For typical TV images, a new correlation peak will occur when the signal preserved as a reference in one correlator occupies the signal register of succeeding correlators in the system. The heights of these peaks represent the degree of correlation between vertically displaced subframes.

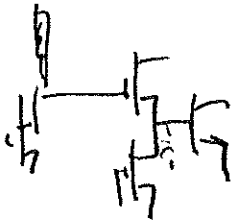
If the reference is held over succeeding frames and the correlator output is used to give a display similar to figure 2, the position of the central peak would represent the best estimate of the direction, and extent of the movement, of an image included in the original picture, or alternatively might represent a drift in the boresight direction of the camera.

INTEGRATED CORRELATOR

A 32 bit integrated correlator chip has been designed using an n-channel polysilicon gate technology. This device contains two 32 bit tapped CCDs, each incorporating facilities for feedback linearisation[3]. The signal register taps drive simple MOS multiplier circuits[4] (figure 4), the outputs of which are taken via positive and negative coefficient bus-bars to current summing amplifiers. The amplifiers are at present off-chip, but have been fabricated in a CCD compatible technology to allow full integration in future designs. The reference register taps drive the other multiplier terminal via sample and hold circuitry to provide true four-quadrant multiplication.

CIRCUIT DESCRIPTION

A floating gate reset technique[1,5,6] was utilised for the tap circuitry. The multiplier circuit (figure 4) consists of two identical MOS transistors, the gates of which are driven in anti-phase about a quiescent voltage, V_B, by a phase splitter circuit. The phase splitter circuit is driven from the reference register, V_{ref}. The output of the signal register taps, V_{sig}, is applied to the drain terminals of



the transistors, the source terminals being connected to the positive and negative coefficient current summing amplifiers.

A first order approximation[7] to the current flowing in the MOSTs is given by:-

$$I_D = \beta ((V_{GS} - V_T) V_{DS} - V_{DS}^2/2),$$

$$V_{DS} \leqslant V_{GS}-V_T$$

where β = constant

V_{GS} = gate to source voltage

V_T = threshold voltage

V_{DS} = drain to source voltage.

The difference in the drain currents flowing in the transistors is given by:-

$$\Delta I_D = \beta (V_{GS1} - V_{GS2}) V_{DS}$$

and since

$$V_{GS1} = V_B + V_{ref}$$

$$V_{GS2} = V_B - V_{ref}$$

and $V_{DS} = V_{sig}$

the difference in currents may be written as

$$\Delta I_D = 2\beta V_{sig} \times V_{ref}.$$

A more accurate computer simulation of the circuit indicates that a multiplication accuracy for typical signal levels of better than 1% can easily be achieved by careful design.

The operation of such a multiplier fabricated on 10 Ω.cm, p-type material, is shown in figure 5. The upper and lower traces are the reference and signal inputs respectively, the output is shown in the centre.

CONCLUSIONS

It has been shown that it is feasible to use CCDs in correlators. Practical techniques have been demonstrated allowing the design of a fully integrated analogue correlator using CCDs. The adoption of these devices should enable high speed real-time processing systems of small size and low power consumption to be constructed.

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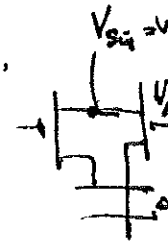
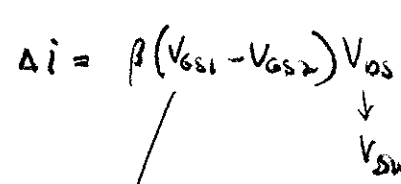
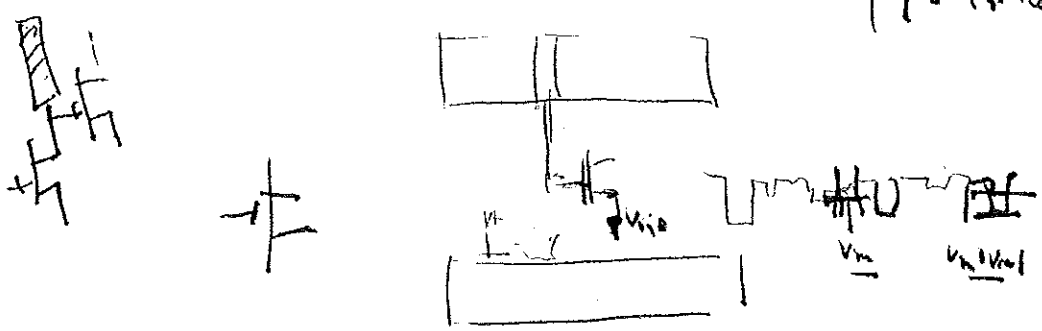






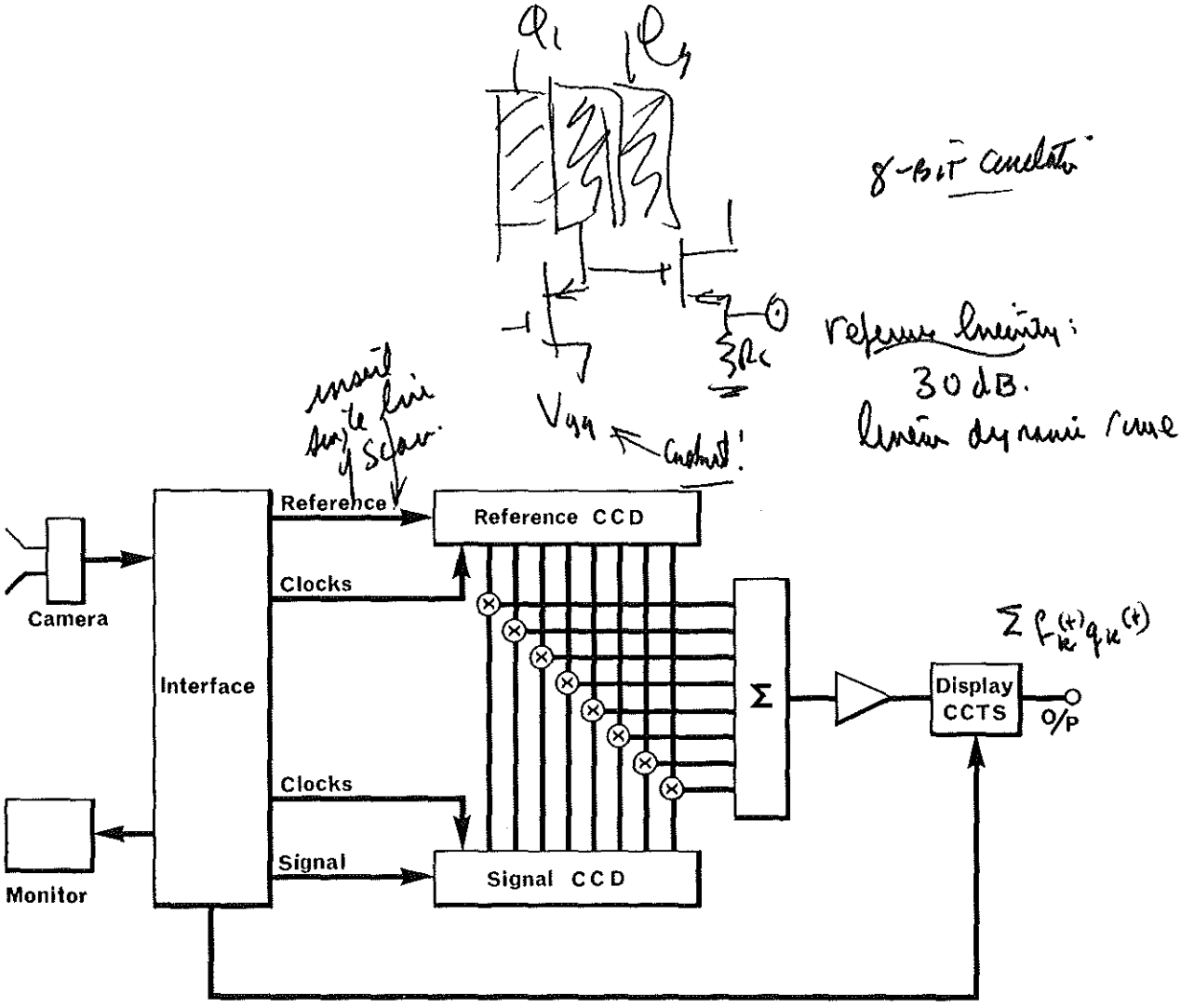
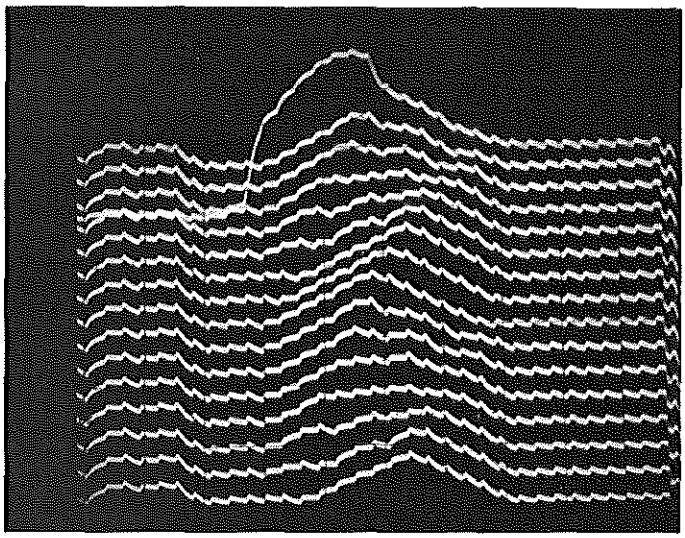


Fig. 1

Analogue correlator

8-bit correlator with 8 grey levels 64 across array.



16 lines

FIG 2A CORRELATOR OUTPUT

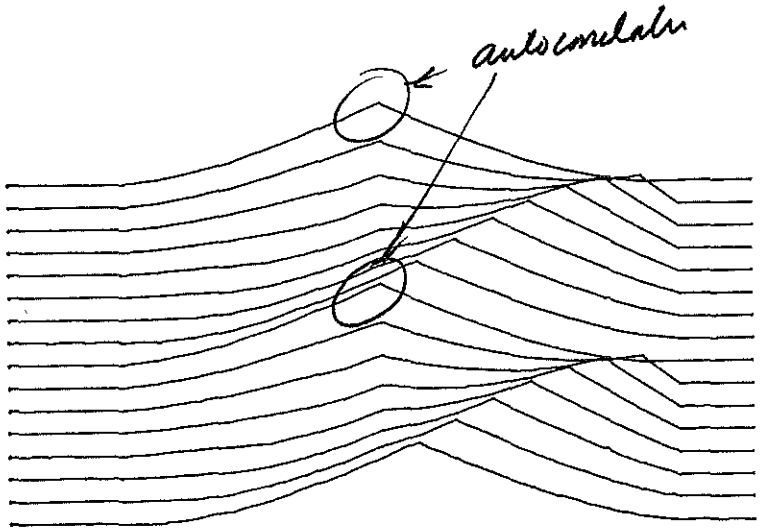


FIG 2B THEORETICAL OUTPUT

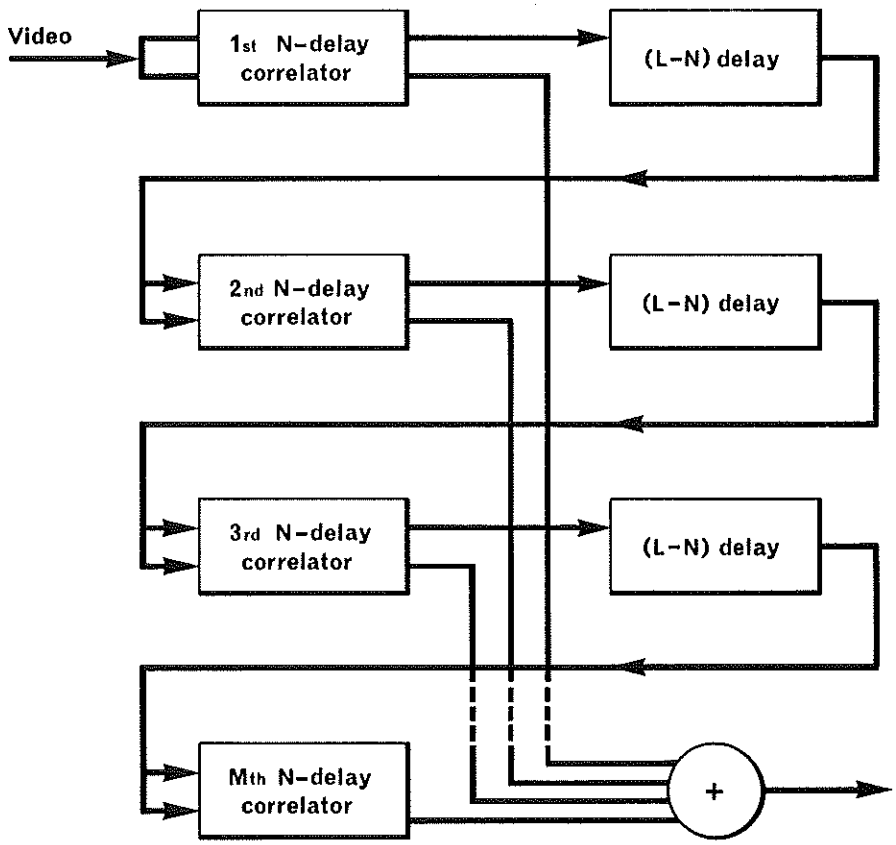


Fig. 3

Two dimensional correlator

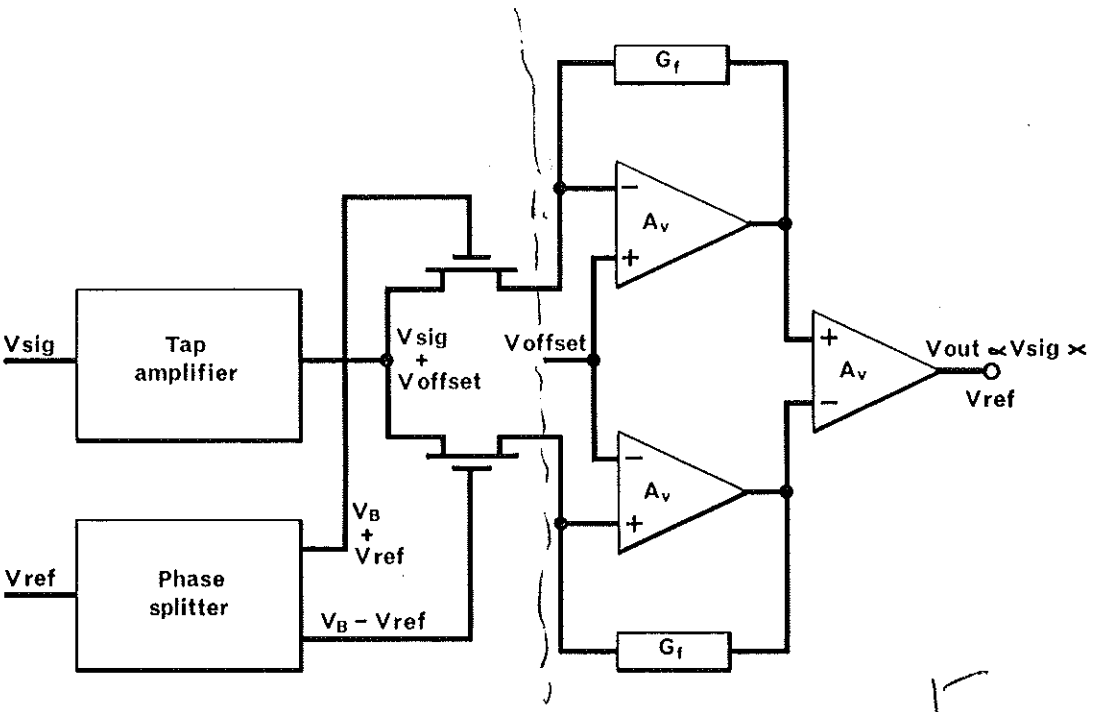
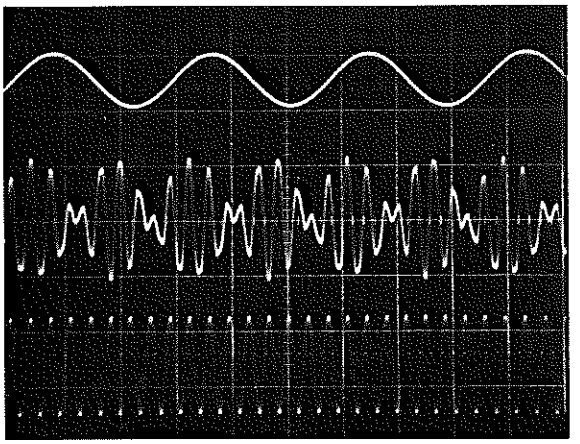


Fig. 4

4 Quadrant multiplier operation



Reference input 2V/Div

Multiplier output 0.5V/Div

Signal input 1V/Div

Time 50 µs/Div

Figure 5 Multiplier Waveforms