DEVELOPMENT OF A 400 x 400 ELEMENT, BACKSIDE ILLUMINATED CCD IMAGER*

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ABSTRACT. Thinned, backside illuminated CCD imagers with 400 x 400 resolution elements have been fabricated using a double level anodized aluminum electrode system. These imagers have been developed for application to deep space photography where array read out rates of about 10 kHz and operating temperature near -40°C are envisioned. The performance of the 400 x 400 will be discussed and comparisons made to the operating parameters of a smaller 160 x 100 array fabricated with the same technology.

INTRODUCTION

Several CCD technologies have been successfully applied to fabricate large area imaging arrays.[1-3] Illumination may be incident on the front, or electrode side of the array, but interference and absorption in either polysilicon or metal oxide electrodes can limit performance. Backside illumination, where radiation is focused on the planar back surface remote from the CCD electrodes, gives uniform and high spectral responsivity. Backside illumination[4-7] requires however that the CCD be thinned to about 10 μm to provide high resolution.

Large area CCD arrays are being considered for application in deep space photography where the requirements are such that the imager should operate at low data rates (~ 10 kHz) which requires device cooling (~ -40°C) to reduce thermally generated dark current during the long read out sequence. In this application the self-canned CCD may replace the conventional electron beam scanned vidicon. However, the processing complexity of the CCD as compared to the vidicon presents formidable problems in obtaining high quality, defect free devices which are greater in area than present commercial MOS integrated circuits.

This paper describes the development at Texas Instruments of a three phase 400 x 400 thinned, backside illuminated CCD array. Double level anodized aluminum technology[4] is utilized. The performance of a 160 x 100 array was discussed recently,[6] and in this paper we extend this discussion to the 400 x 400 imager. Both arrays have essentially the same serial-parallel-serial organization. Some of the processing details of particular concern with large arrays will be discussed.

DESIGN AND FABRICATION

The 400 x 400 is an n-channel, three-phase (3ϕ) CCD, typically fabricated on 10-15 ohm-cm p-silicon. The resolution element size is 0.9 x 0.9 mil^2 which requires that each parallel and serial electrode be 0.3 mil in width. The channel width in the parallel section is 0.7 mil with 0.2 mil channel stop regions for an active area of 360 x 360 mil^2 on a 496 x 496 mil^2 chip of silicon. First and second level aluminum electrodes are isolated by about 2500 Å of Al_2O_3 formed by first level anodization. The structure is shown schematically in Figure 1 where it is apparent that a given phase occurs alternatively on first and second level electrodes. A photomicrograph of the corner of the array showing the output amplifier is shown in Figure 2. Since in the 3ϕ design,[7] each level is formed at an independent step in the CCD process, integration under a single parallel phase could possibly introduce line to line variation in the video output. Oscilloscope photographs showing several video lines are shown in Figure 3. Figure 3a indicates

video resulting from integration under ϕ_1 only and Figure 3b shows video after integration under both ϕ_2 and ϕ_3. The line pairing, which is a feature of the 3ϕ design is completely eliminated by using two electrodes. Square wave amplitude response (SWAR) data, giving resolution performance of the imager, is more reproducible using the two electrode scheme.

The second level electrodes overlap those on the first level by 0.05 mils to give a completely sealed electrode system. This allows buried channel array operation with high charge transfer efficiency (CTE). This design leaves 0.2 mil separation between electrodes which is the minimum that can reliably be opened by conventional wet etching technique. To maintain the design overlap of 0.05 mil in both parallel and serial sections presents formidable difficulties in both optical photomask generation and slice processing. CCD processing requires nine photomask levels which must be registered with each other, although of course, some are more critical than others. Random variations inherent in the generation of the master masks, which are due to mechanical limitations, can amount to ±0.015 mil and this can significantly affect a design overlap of 0.05 mil. The design overlap must also be maintained over many repeated arrays on the working photomasks used in processing. For processing on two inch diameter silicon slices, six to seven bars can be used while for three inch processing, 21 bars can be used.

A second factor which impacts device yield is the occurence of random defects in the photomasks such as accidental bridging between two channel stops (nonfatal) or between two metal electrodes (fatal). Individual treatment to eliminate these defects is often necessary on the master reticle. These defects can be due to imperfections in the Si_3N_4 used for the working masks or to dust particles in related processing and individual treatment is again used in most cases to remove most of these defects. In spite of these problems, however, it has been found that the design tolerances can be maintained over sufficiently wide fields so that processing can be performed on three inch silicon slices. At the present time device performance in so far as it is effected by photolithography, does not appear to be significantly affected by location on a processed slice. Extension to larger arrays, for which the tolerance must be maintained over larger areas will be a progressively more difficult problem.

The 400 x 400 is designed to operate in the full frame imaging mode. An upper and lower output serial register is provided to allow forward or reverse array operation which increases device yield in the event of a malfunction of one of the on-chip output amplifiers. The array is divided electrically into four independent 100 x 400 sections so that a fatal processing defect in one section does not preclude operation of a partial array. This design feature allows an increased amount of performance data from a processed lot to be obtained for evaluation purposes. All electrical inputs necessary for array operation can be brought to bond pads along two edges of the CCD chip. Thus each 400 x 400 chip can be cut with a few mils of the two remaining array edges to allow a 800 x 800 mosaic to be made with the loss of only 5-10% of the active area.

The output from the CCD is by a simple precharge amplifier with reset switch (buried channel) and source follower (generally surface channel). For generation at 10 kHz follower load, resistors of up to 50 K are possible to reduce on chip power dissipation and membrane heating while maintaining low MOSFET noise.

Bond pads are extended some 50 mils from the active array so that the edges of the thinned silicon can extend outside this area but still leave a thicker 25 mil rim for membrane support. Thinning is performed by chemical etching techniques in which either a selected chip or complete slice can be thinned. The resulting membrane surface is highly reflective and can readily be coated with an antireflection (AR)/passivating layer of SiO. Although the membrane is generally somewhat nonplanar due to process-induced stress, device performance does not appear to be affected, even by repeated temperature cycling between 24°C and -40°C. A photograph of a CCD mounted in a 40 pin dual in line header is shown in Figure 4.

Buried channel operation of the array is necessary to achieve high performance at all points in the array. A 0.5 to 1.0 µm deep channel is formed by implanting phosphorus and a CTE > 0.9999 is measured in the serial register with 8-10 V clocks and no electrically introduced fat zero. Equally good CTE

in the parallel section is inferred from the square wave amplitude response (SWAR) data and is also measured by electrically injecting a pulse into the upper serial register and transferring through the parallel section to the power output amplifier.

CCD device processing generally makes use of conventional MOS techniques. p^+ channel stops and n^+ diodes are formed by boron and phosphorus diffusion, respectively. Typical gate oxide thickness for the CCD's is 1350 - 1500 Å. The buried channel is then formed by the phosphorus implant and subsequent drive in diffusion. This process is critical to obtain low dark current imagers. After first level metal patterning, the metal is protected by a layer of photoresist (vias) in certain areas which must connect to subsequent second level metal electrodes. Vias eliminate the need for less reliable n^+ diffused tunnels as a means of interconnection for the electrode structure and allows all electrodes to be brought out on the same side of the array (Figure 2). The exposed metal is anodized and interconnects which had been required for electrical continuity during anodization are removed. Second level metal is then patterned to give a completely sealed electrode system. Detailed inspection of the first level pattern after etching generally revealed undesirable accidental bridges between adjacent metal electrodes due to either resist contamination during processing or to photomask defects. These would result in intralevel shorts if not removed prior to anodization. Pinholes in the anodic oxide which isolates first and second level electrodes will result in interlevel shorts. Anodization is a self-healing process and the quality of the interlevel isolation is very high. Nevertheless, metal defects are the dominant failure mode for our CCD's. Pinholes in the gate insulator are also fatal defects and considerable effort has been mode to grow high quality SiO_2 layers. Dry oxidation between 1000°C and 1100°C, with and without HCl impurity doping and steam oxidation at 950° have been investigated as well as the influence of chemical and vapor cleaning techniques on the pinhole density in the gate oxide layer. At present, the CCD gate is grown by steam oxidation and pinhole densities well below 1/cm² have been achieved. The formation of pinholes appears to result from nonrandom defects or particles at the silicon surface prior to oxidation. Over the range 1000 Å to 1500 Å, the pinhole density does not appear to depend strongly on oxide thickness.

The thermally generated array dark current in the buried channel arrays can be very low (1 nA/cm), provided bulk gettering processes are applied in processing. At these levels the dominant dark current contribution is generated at the surface rather than in the bulk silicon as evidenced by a weak dependence of array dark current on clock voltage. Storage times to reach full well of 15 sec at 24°C and about three hours at -40°C have been achieved with the smaller 160 x 100 array. The incidence of localized dark current spikes in these deices is essentially zero. Since the generation rate for these spikes does not decrease with temperature as does the bulk silicon contribution, long storage times (or low dark currents) at reduced temperature require low defect density devices.

IMAGER PERFORMANCE

The successful use of large area CCD imagers in any application requires that an array meet many performance criteria simultaneously. In particular, low dark current with high uniformity must be combined with high uniform spectral responsivity to optical radiation. This latter parameter is of particular concern because large pixel to pixel nonuniformity in response may require excessive data reduction programs to allow maximum information to be obtained from the array. High CTE will result in maximum SWAR across the array while the backside illuminated geometry will provide the highest responsivity and quantum efficiency. Other parameters, such as their membrane planarity, will impact the final design of the optics which focus the image onto the CCD surface.

Operation of a 400 x 400 array at 10 kHz requires a read out time of 16 sec versus 1.6 sec for the 160 x 100. The read out sequence must be performed in the dark to avoid image streaking. Low data rates also streak out any individual blemished pixels so that defects which appear strongly localized at 3 MHz are not as well defined at 10 kHz. While this will improve uniformity of response, it limits the dynamic range of the imager. Imagery taken with the 400 x 400 at -40°C with a 0.25 sec integration time and a 10 kHz read out is shown in Figure 4.

Performance parameters for two representative 160 x 100 buried channel arrays

have been presented elsewhere. In Table I,

TABLE I

Characteristics of Typical (Best in Brackets) 160 x 100 Arrays and Initial 400 x 400 Arrays

CTE	160 x 100: 0.9999 (8V Clocks)	400 x 400: 0.9999 (8V Clocks)
Dark Current 24°C	6.5 (1.8) nA/cm^2	7.4 nA/cm^2
-40°C	0.008 (0.0011) nA/cm^2	0.19 nA/cm^2
Responsivity	90 mA/watt (No AR)	72 mA/watt (No AR)
SWAR at the Nyquist Frequency		
Parallel to Serial	49% (Array center)	39% (Center)
Perpendicular to Serial	50% (Array center)	36% (Center)
Uniformity of Response (-40°C)	0.12 (0.08)	0.16
Dark Uniformity (-40°C)	0.50 (0.14)	0.43

representative average and best parameter values are given for 160 x 100 devices based on experience gained during a twelve-month period. Also shown are values for initial buried channel, 400 x 400 arrays. Excellent charge transfer characteristics are evidenced by high CTE and SWAR. For the larger array, there is only a few percent decrease in SWAR going from a pixel near the output to one far from the output.

The 160 x 100 array design has on chip preamplifiers with MOSFET loads which result in heating of the membrane and this can limit device storage time. The storage times quoted above were determined by disabling the amplifiers during a variable integration period and reading out the serial register rapidly at 1 MHz. Membrane heating from the source follower on the 400 x 400 can also be observed at long integration times where typical on chip power dissipation is 20-40 milliwatts for a 5 KΩ off chip load. This lead to increased dark current nonuniformity. These effects can be minimized however by positioning the amplifier on the thick silicon rim or by using a higher load resistor (say, 50 KΩ) which is certainly permissable for 10 kHz data rates. As indicated in Table I, initial 400 x 400's, which were processed on three-inch silicon, typically showed a higher density of localized dark current blemishes than expected from recent 160 x 100's. The contribution of these blemished pixels to array dark current does not decrease like $T^{3/2}\exp(-Eg/2kT)$ as predicted and higher than expected dark current is measured at -40°C. These localized spikes may be due to defects in the silicon substrate, residual impurities in the silicon, or implant damage which is not completely annealed. Subsequent processing improvements are expected to significantly reduce these localized dark current sites to the low levels seen in the smaller arrays.

The backside illuminated CCD should be characterized by highly uniform responsivity since optical radiation is focused on an etched silicon surface. However, membrane thickness non uniformities often result in bands of higher (or lower) sensitivity. Uniformity of response, as measured by sampling each pixel with a multichannel analyzer and defined as the standard deviation divided by the mean, has been limited to about 8%. Variations in the backside accumulation process used at the membrane surface also lead to non uniformities in response, particularly at shorter wavelengths. Devices with 70% quantum efficiency at 4000 A have been fabricated but at present an average value is in the range 10 - 20%. High QE devices often show some variation in responsivity as the temperature is decreased from 24°C to -40°C which is generally not observed in the lower QE devices. Surface passivation with AR coatings of SiO have been applied to the membrane surface and appear to stabilize device response against long term variations. It is expected that improved etching techniques together with passivation will eventually result in response uniformity of 5% or better.

CONCLUSIONS

High performance, backside illuminated CCD arrays have been demonstrated in a configuration sufficiently large to have application in a spacecraft environment. Operation at low data rate and -40°C appear to be compatible with the thinned CCD technology. Further improvement in array performance is predicted and improved packaging techniques, particularly aimed at increasing stability of the thin membrane, will be implemented to allow eventual application in the spacecraft camera system.

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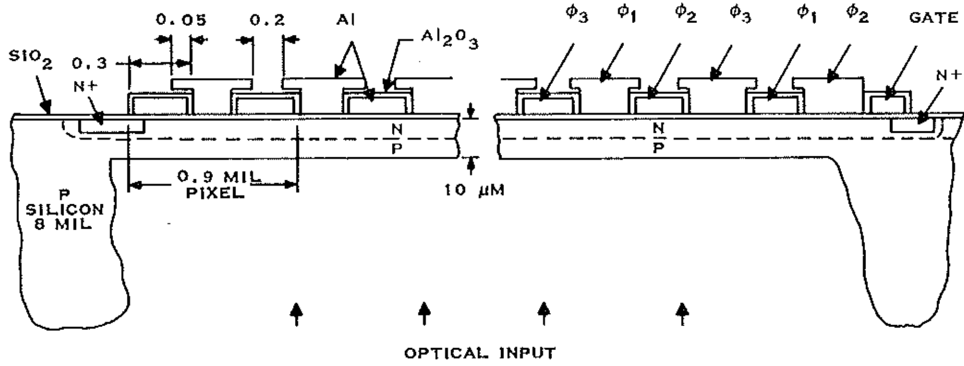

Fig. 1. Schematic of backside illuminated, double level metal CCD.

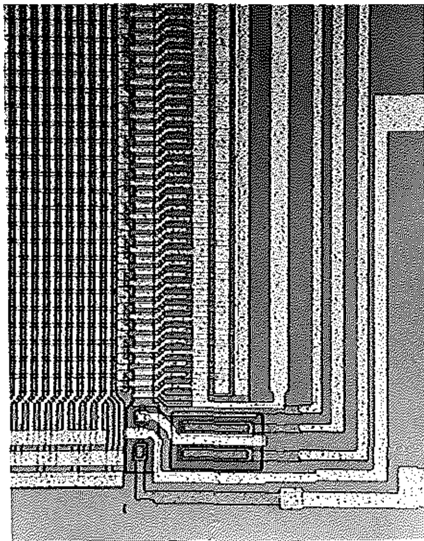

Fig. 2. Photomicrograph of one corner of the 400 x 400 array showing both serial and parallel busing from one side. The output amplifier is a reset switch and source follower.

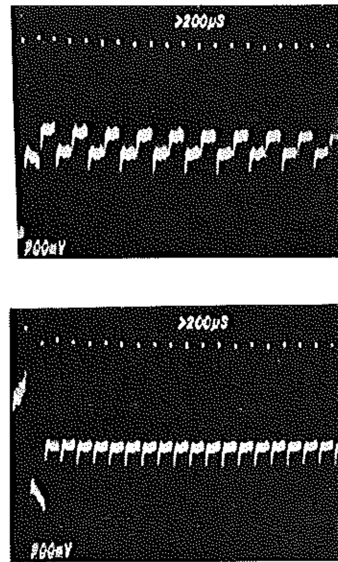

Fig. 3. Line video output from CCD using ϕ_1 parallel for integration (a) and $\phi_2 + \phi_3$ for integration (b).

Fig. 4. Imagery of the IEEE Standard taken with a 400 x 400 at 24°C and 1 MHz data rate corresponding to a frame time of 163 msec.