INFRARED IMAGING WITH MONOLITHIC, CCD-ADDRESSED SCHOTTKY-BARRIER DETECTOR ARRAYS: THEORETICAL AND EXPERIMENTAL RESULTS*

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ABSTRACT. The theoretical basis for infrared imaging in the 3 to 5 μm spectral band with CCD addressed silicon, Schottky-barrier mosaics is presented. A unique approach is used which allows readout of majority carrier signals with depletion mode CCD's. Photo-response, contrast, and noise relationships for this type of all solid-state sensor are derived. It is seen that the use of the Schottky-barrier, internal-photoemission process, which is independent of lifetime and doping variations in the silicon wafer, leads to at least a factor of 100 improvement in infrared photoresponse uniformity. This advance permits for the first time the development of infrared cameras that are not limited by fixed pattern noise. Systems considerations such as cooling requirements, noise mechanisms, and cutoff wavelengths, are related to signal contrast and noise-equivalent-temperature (N.E.ΔT.). A charge-coupled imager sensitive to infrared light as far out as 3.5 μm has been fabricated and operated. It consists of a linear array of 64 Pd:p-Si Schottky-barrier detectors adjacent to a three-phase charge-coupled shift register. A single transmission gate, when pulsed on, coupled each detector to its associated shift register gate, thus reverse-biasing the detectors. The charges transferred to the shift register are then read out sequentially to produce the video signal. It is demonstrated that in this mode of operation, the IR-CCD is particularly immune to non-uniformities in substrate doping and in MOSFET pinch-off voltage. Visible images were sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1\ \mu m < \lambda < 3.5\ \mu m$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their responses to changes in their separate integration times. All IR measurements were made at 77°K. Uniformity was within a few percent, and objects at 110°C could be detected. A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip. Operation in this mode was also demonstrated.

INTRODUCTION

The realization of a viable infrared television camera with electronic scanning would represent a major advance in thermal imaging technology. Applications would range from military reconnaissance and weapons delivery systems to high resolution, real-time thermography systems for earth resource management and medical diagnostics. We will describe recent results of a device effort directed towards the development of silicon monolithic focal planes that are suitable for an IRTV.

The design of an IRTV camera for thermal imaging is complicated by signal conditions which include the presence of high photon flux densities from the thermal background and low scene contrast. Cameras use frame integration to achieve high sensitivity; therefore, an IRTV must have very wide dynamic range to accommodate background flux integration without signal saturation. Further, in the presence of high background flux densities, point to point variations of photoresponse, give rise to fixed pattern noise which obscures low contrast detail. We are attempting to develop a diode array

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focal plane that has sufficient dynamic range to accommodate the infrared background in the 3 to 5 μm spectral range and sufficient spatial uniformity to give good thermal imagery. The focal plane consists of ordered arrays of Schottky internal photoemission diodes operated in staring-mode which are multiplexed by an integral surface channel CCD. The focal plane is fabricated using standard silicon microcircuit technology.

SCHOTTKY INTERNAL PHOTOEMISSION

It has been suggested that the Schottky internal photoemission process is inherently more uniform than conventional photodetection processes and that this process could be exploited in the development of IR thermal imaging retinas.[2] The internal photoemission process is shown in Fig. 1. The metal photocathode of a Schottky barrier is illuminated through the silicon semiconductor substrate resulting in photoemission of charge into the semiconductor from the metal. Photoemission occurs in a spectral band determined by the silicon transmission edge at 1.1 μm and the internal photoemission threshold wavelength, λ_c, given by

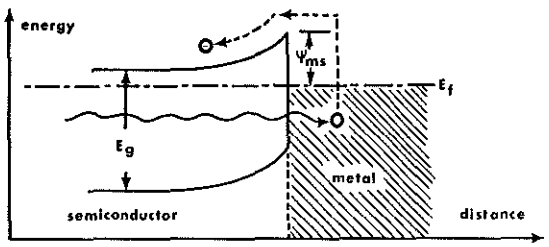

Fig. 1. Band diagram of Schottky-barrier detector.

$$\lambda_c(\mu m) = \frac{1.24}{\psi_{ms}(eV)} \qquad (1)$$

where ψ_{ms} is the Schottky barrier potential. Within the above spectral range, the photoemission quantum efficiency, η, is given by

$$\eta(\nu) = C_1 \frac{(h\nu - \psi_{ms})^2}{h\nu} \qquad (2)$$

provided that the metallic photo-absorption process is energy independent. In Eq. 2, $h\nu$ is the photon energy and C_1 an efficiency coefficient that is dominated by properties of the metal.[3,4] Archer and Yep[5] have shown that the value of ψ_{ms} is independent of the substrate doping density over large ranges of impurity concentration. The only significant variation of ψ_{ms} with semiconductor properties is that due to the conductivity type where

$$\psi_{msn} + \psi_{msp} = E_g \qquad (3)$$

Thus, the quantum efficiency of an internal emission photodiode is expected to be insensitive to normal variations in semiconductor properties. Further, it should be noted that this process emits majority carriers into a substrate that is operating at high enough temperatures to have full extrinsic ionization; two factors which combine to eliminate most of the causes of spatial non-uniformities in the photoresponse of other detectors. Variations of minority carrier lifetime, diffusion length and impurity compensation can be neglected. The key remaining causes of spatial non-uniformity will be variations of sensor cell geometry, Schottky barrier formation metallurgy, multiplex losses and dark current. Dark current variations can be minimized by cooling to the point where dark signals are negligible. We note that the dark current density is given by

$$J_d = A_r T_d^2 \exp\left(\frac{-\psi_{ms}}{kT_d}\right) \qquad (4)$$

where k is Boltzmann's constant and A_r is Richardson's constant (20A cm^{-2} $°K^{-2}$ for p-Si) and T_d is the detector temperature. Dark currents become neglibible at 80°K for $\lambda_c \leq 5$ μm.

Shepherd, et al[6] have shown experimentally that both continuous and reticulated Schottky surfaces have the expected improvements in spatial uniformity, but their work does not include the effects of spatial variation of multiplex losses.

THERMAL IMAGING

Since quantum efficiencies of internal photoemission diodes are low, staring-mode operation is used to achieve good sensitivity. In staring-mode an infrared scene is projected onto the Schottky array and the resulting signal is accumulated for a frame time, t_s. At the end of the frame, the array is multiplexed cell by cell and

the resulting charge pulse train provides a video signal of the IR image. We will now calculate the magnitude of these charge pulses and the resulting sensitivity of the Schottky arrays.

Consider a Schottky focal plane mounted in a cold chamber that is exposed to a uniform thermal background at temperature, T_b, through an aperture of f-number, F. In the short wavelength limit, where $h\nu >> kT_b$ the photon flux incident on the focal plane in the frequency interval, $d\nu$, is given by

$$N(T_b,\nu)d\nu = \frac{\pi\nu^2}{2c^2F^2}\exp\left(\frac{-h\nu}{kT_b}\right)d\nu \qquad (5)$$

where c is the velocity of light and h is Planck's constant. The number of electrons collected per frame by a cell of area A is given by

$$N_b = At_s\int_{\psi_{ms}}^{\infty}\eta(\nu)N(T_\nu,\nu)d\nu \qquad (6)$$

$$N_b = \frac{\pi At_s C_1 k^4 T_b^4}{c^2F^2h^3}\left(\frac{\psi_{ms}}{kT_b}+3\right)\exp\left(\frac{-\psi_{ms}}{kT_b}\right) \qquad (7)$$

The resulting signal contrast, γ, is given by

$$\gamma = \frac{dN_b}{dT_b}\,N_b^{-1} \qquad (8)$$

For a Schottky retina that has a barrier height ψ_{ms} the contrast is given by

$$\gamma = \frac{1}{T_b}\,\frac{\left(\frac{\psi_{ms}}{kT_b}+3\right)^2+3}{\left(\frac{\psi_{ms}}{kT_b}+3\right)} \qquad (9)$$

For a 15°C background, γ varies from 6.9%/°K for threshold at 3 μm to 4.3%/°K for threshold at 5.5 μm. Thus, a system uniformity better than 0.4% would not prevent the resolution of 0.1°K details.

In order to calculate the response of a Schottky retina to a thermal signal we note that most metals have values of $C_1 \simeq 0.1$ $(eV)^{-1}$. Later we will consider a CCD addressed retina that has Pd_2Si Schottky contacts of area 2.8×10^{-5} cm^2. The Pd_2Si retina has a photoemissive threshold at $\lambda_c = 3.54$ μm. Other retinas under design cut-off at 4.5 μm and 5.5 μm. The cell response of these retinas to a 15°C background is given in Table 1.

Table 1. Thermal Background Photoresponse of Schottky Diodes

λ_c(μm)	$N_b(T_b)$	$\gamma N_b(T_b)$	$N_b(T_b+10°)$	$N_b(T_b+100°)$
3.54	2.0×10^4	1.2×10^3	3.6×10^4	2.0×10^6
4.5	3.4×10^5	1.7×10^4	5.5×10^5	1.6×10^7
5.5	2.2×10^6	9.5×10^4	3.3×10^6	saturated

T_b = 15°C, A = 2.8×10^{-5} cm, t_s = 30 ms, F = 1, and C_1 = 0.1 eV^{-1}.

A detail in an infrared scene will be detected as a low contrast signal superposed on the background signal, N_b. Consider an object which is at a temperature ΔT above T_b, and which has an image that subtends a sensor cell. The cell which views the object will have an accumulated charge N_j where

$$N_j = N_b + \frac{dN_b}{dT}\Delta T \qquad (10)$$

The signal of interest is

$$N_s = N_j - N_b = \frac{dN_b}{dT}\Delta T = \gamma N_b\,\Delta T \qquad (11)$$

Note that γN_b given in Table 1 represents the number of additional charges counted per cell from an object 1°C above background temperature. The signal-to-noise ratio of our measurement will be

$$\frac{N_s}{\overline{N}_t} = \frac{\gamma N_b \Delta T}{\overline{N}_t} \qquad (12)$$

Where $\overline{N}_t$ is the total rms noise of the detector, its multiplexer and its associated amplifiers. The noise equivalent temperature is then given by setting Eq. 12 to unity.

$$(NE\Delta T) = \frac{\overline{N}_t}{\gamma N_b} \qquad (13)$$

To find $\overline{N}_t$ we follow Carnes and Kosonocky[7] with the following differences:

1. On focal-plane thermal noise corresponds to 80°K rather than 300°K.

2. Operation is at high infrared backgrounds where photo-electron shot noise can be significant, and where, for low contrast targets, $N_j \simeq N_b$.

TABLE 2. IR SCHOTTKY CCD NOISE SOURCES AND NOISE EQUIVALENT TEMPERATURES[a]

SOURCE	$\overline{N}$	λ_c = 3.54 μm	λ_c = 4.5 μm	λ_c = 5.5 μm
Photo-electron Shot Noise	$\sqrt{N_b}$	1.4×10^2	5.8×10^2	1.5×10^3
Background Charge, Incomplete Transfer Noise[b]	$\sqrt{2\varepsilon N_g N_1}$	1.6×10^3	1.7×10^3	2.1×10^3
Fast Interstate Trapping Noise[c]	$\sqrt{1.4 N_g (kT/q) N_{ss} A_g}$	1.6×10^3	1.6×10^3	1.6×10^3
Floating Diffusion Reset Noise	$200\sqrt{C_{pf}}$	200	200	200
Combination of Above Noise Sources	$\overline{N_t}$	2.3×10^3	2.4×10^3	3.0×10^3
NEΔT From Above Sources	$\overline{N}_t/\gamma N_b$	1.9°K	0.15°K	0.04°K
NEΔT Including Above Sources and 1% Nonuniformity		1.9°K	0.20°K	0.23°K

a) Terms defined in Ref. 7.

b) εN_g (transfer loss per gate times number of gates) was taken from Ref. 8.

c) N_{ss} was taken as 4×10^{10} cm^{-2} eV^{-1}.

Because of the large background signal, an electrical bias charge (fat-zero) is not needed. Assuming that the first well has 0.25 pf capacitance and the floating diffusion and MOSFET gate have 1 pf capacitance, we find the results given in Table 2. These results indicate that a Schottky focal plane with a floating diffusion and MOSFET output can have very good sensitivity.

IR-CCD DESIGN

There are several approaches to the design of infrared, charge-coupled imagers. One is the fabrication of charge-coupled shift registers on materials having the desired intrinsic response.[9] Such materials include InAs, InSb, and HgCdTe. Infrared radiation would be absorbed in the wafer, generating minority carriers which would then be transported just as in silicon devices. A second approach is the fabrication of charge-coupled shift registers on silicon wafers with separate infrared detectors prepared on the wafer. Schottky barriers are a natural choice though photoconductive films and heterojunction detectors are other possibilities.[8] A third approach is the use of extrinsic silicon.[10]

Our approach to the design of infrared-sensitive, charge-coupled imagers has been to use well-known technologies, namely charge-coupled shift registers and Schottky-barrier detectors fabricated on silicon wafers. This requires that the majority-carrier signals from the detector be converted to minority-carrier packets for transport by the shift registers. Methods for accomplishing this were reported by Shepherd and Yang,[2] and by Williams and Kosonocky.[11] The latter method, which we adopted for this work, is simpler, and has the advantage that the large background signal from a thermal scene need not be transferred to the shift registers. While this technique does not, by itself, compensate for nonuniformities in the detector array, it does make better use of the shift register's dynamic range and thereby makes possible the use of frame comparison techniques. To test these ideas, we fabricated 64 x 1 linear arrays of Schottky-barrier detectors coupled with three-phase, charge-coupled shift registers. The structure used for coupling the Schottky barrier detectors to the charge-coupled shift register is shown in Fig. 2. A row of Schottky-barrier metallizations is seen in the center of the chip. The center area

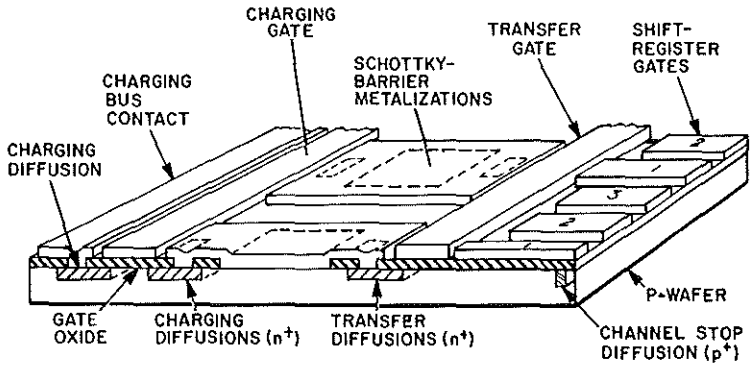

Fig. 2. Layout of IR-CCD.

of each metallization contacts the p-wafer forming the infrared-sensitive area. Each metallization also contacts individual charging and transfer diffusions. The transfer gate overlaps the transfer diffusions, and can couple them individually to the phase-1 gates of the shift register. The phase-1 gates are wider than the other shift register gates for just this reason. The charging gate on the left of the detectors overlaps the individual charging diffusions and can couple them all at once to the charging bus diffusion. A channel stop diffusion at the right terminates the shift-register channel as shown in the illustration. The shift-register gates are connected to three phase buses to the right of the channel (not shown in Fig. 2) Strips of channel stop, also not shown in the illustrations, are included between the detectors to prevent coupling.

The structure shown can be operated in two different modes: the high contrast mode or *vidicon mode*, and the *thermal imaging mode* or *skimming mode*. A device designed for use in the high contrast mode does not require the charging gate or the charging diffusions. If these structures were included in the device, the charging gate can simply be biased negatively and ignored. The three-phase clock voltages are applied to the shift-register gates. At some time in the cycle, when the phase-1 shift register gates are on and the other two phases are off, a positive pulse is applied to the transfer gate making the potential under that gate V_A as in Fig. 3b. The floating transfer diffusion will settle at a potential equal to V_A. All excess charge flows across the transfer gate channel into the deeper CCD potential well. After the transfer pulse ends, the shift register clocks out the charge packets. The next time, and each subsequent time, the transfer pulse is applied, the detectors are reset to the same potential, V_A, and the charges removed are stored in the phase-1 wells. These charges represent the photocurrent and dark current that accumulated at the detectors during the integration time, and make up the video signal when read out. This mode of operation is somewhat different from that used in interline devices with photogates where all minority carriers are removed from the detectors during the transfer time. It is more closely related to the mode of operation of a vidicon, since the detectors are reset to the same potential each frame, with the charge removed to do this making up the video signal. Hence, the designation: *vidicon mode*. An imager designed for use in this mode should have detectors whose charge storage capacity is about the same as a shift-register well since the entire detector signal plus dark current must be carried out by the shift register. For thermal images with only a few percent contrast, however, the dynamic range of the shift register would be better utilized if only the small fraction of charge containing the signal modulation were transferred out by the CCD and the large constant background charge containing no information were removed by an auxiliary drain. This can be accomplished with the help of the charging bus and the charging gate shown in Figs. 2 and 3. A large potential V_B is applied to the charging bus (Fig. 3B) which acts as an auxiliary drain for the constant background charge. A clock pulse is applied to the

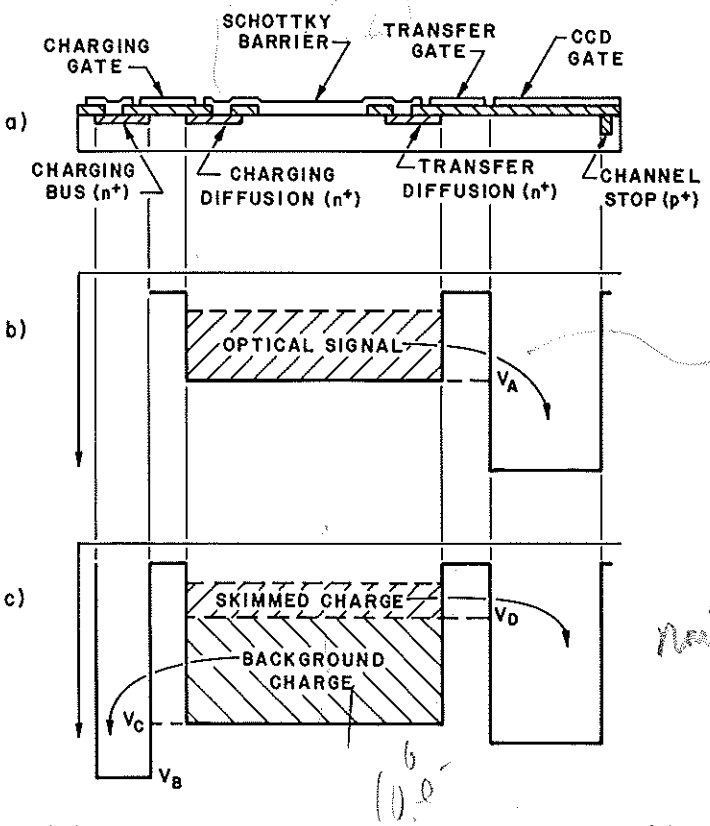

Fig. 3. Electron potential energy profile of IR-CCD during operation. (a) Cross-section of device. (b) Potential profile during operation in the vidicon mode. (c) Potential profile during operation in the thermal imaging mode. Certain details were omitted for clarity.

charging gate once per frame, setting the surface potential under it to V_C. This in turn sets the charging diffusions, Schottky-barrier gates and transfer diffusions to V_C, since all excess electrons stored on these conductors will spill over the charging gate channel into the charging bus and be returned to the substrate. Thus the initial level of the Schottky barrier is set by the charging gate pulse amplitude, not by the transfer gate pulse amplitude as in the vidicon mode described earlier. At the end of the integration period a small pulse is applied to the transfer gate which causes its surface potential to go to V_D (see Fig. 3c). Now only the charge above V_D will drain into the CCD potential well and be read out. Remaining behind is the constant background charge. This background charge is removed shortly thereafter when the charging pulse comes on and sets the Schottky barrier to V_C. It is assumed that the light falling on the detectors is sufficient to discharge each of them below V_D. In actual operation, V_C would be adjusted to ensure this condition.

DESIGN AND FABRICATION

The shift register was a 64 bit, 3-phase, linear CCD having a single level of metallization with 2.5 μm gaps. The gates are 12.5 μm long in the directions of charge transfer, making the bit spacing 45μ. The channel is 125 μm wide, and is confined by a channel stop diffusion. The Schottky-barrier contact holes are rectangles 125 μm by 22.5 μm and are spaced on 45 μm centers along the CCD register so that each detector can load into a phase-1 CCD gate when the transfer gate is clocked. There is a source diffusion with loading gates at one end of the shift register and a reset-table floating diffusion connected to an

on-chip MOS transistor at the other end. The fabrication procedure is as follows. A $10^{15}/cm^3$ doped (100) silicon wafer is subjected to a p-type diffusion and an n-type diffusion, each defined by a thermal oxide left after a photolithographic step. The gate oxide is grown, and contact holes are opened. Palladium is then evaporated onto the wafer in a vacuum system that received special care to avoid sodium contamination. While the palladium is being evaporated, the wafer is heated, causing palladium silicide to be formed in a chemical reaction. The wafer is then removed from the evaporator, and the remaining metallic palladium is etched off. It is returned to a vacuum system, where it receives a film of aluminum to be defined photolithographically. Thinning was not necessary because silicon is transparent to infrared light beyond 1.1 μm. Fig. 4 shows photomicrographs of the two ends of a completed device on a wafer containing about 50 chips. The vertical white rectangles in a row along the top (1) are the Schottky barrier metallizations, each overlapping the contact holes to the substrate and to the setting and transfer diffusions. The setting gate (2) and the transfer gate (3) control the channels to the setting diffusion (contacted by 4) and the phase-1 gates (5), respectively. The bonding pad for the phase-1 bus-bar (5) cannot be seen because it is near the center of the CCD. Phases 2 (6 and 7) and 3 (8 and 9) are double-end connected because they require a diffused crossunder which is more resistive than a metallization. Two separate gates are provided at the beginning (10 and 11) of the shift register and at the end (12 and 13). A source diffusion (contacted by 14) is provided to permit electrical input to the shift register while a floating diffusion with a reset gate (15) and drain (16) is provided at the output. The floating diffusion is connected to an on-chip MOS transistor whose source and drain diffusions are brought out to pads 17 and 18. Contact to the substrate is made at pads 19 and 20, each of which contacts a channel-stop diffusion.

A circuit diagram of the IR-CCD chip is shown in Fig. 5. The extra gates G_2 and G_3, which were included to make possible other input and output schemes, are connected in sequence with the three phases, while G_4 receives a small positive bias, and the reset gate is pulsed. For operation with electrical input, the transfer gate receives a negative bias, isolating the shift register from the detectors while the three-phase, overlapping clock waveforms run continuously, and a burst of electrical pulses is applied to G_1. At the clock rate of 250 KHz used in this work, the minimum transfer loss of 5×10^{-4} per transfer was achieved with a bias current (fat zero) of 0.3 μA.

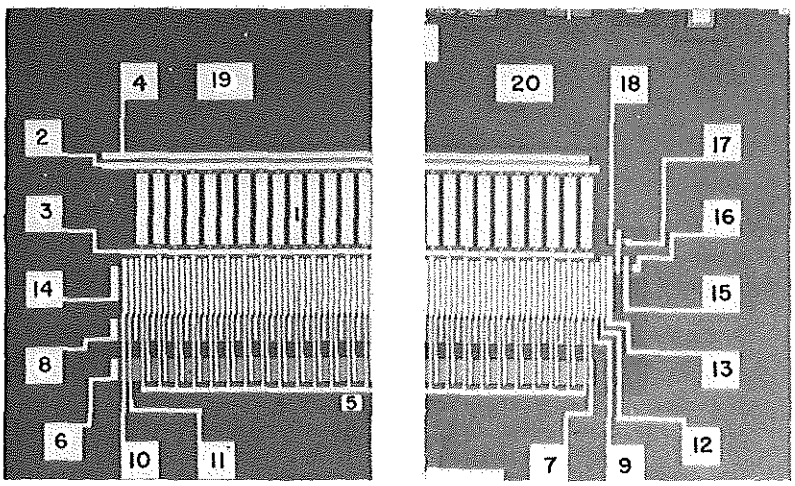

Fig. 4. Photomicrographs of the two ends of the CCD chip.

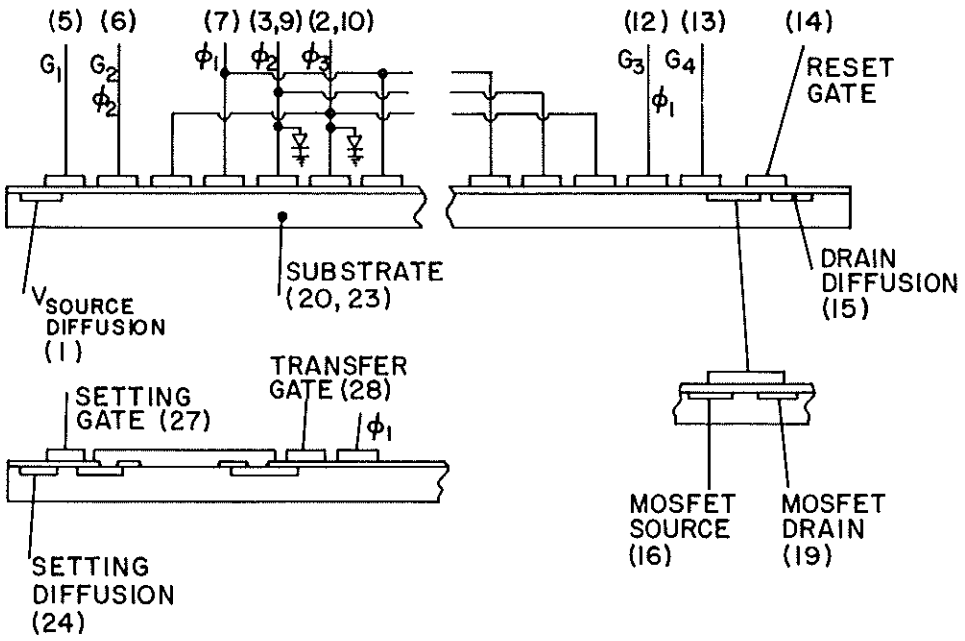

Fig. 5. Circuit diagram of the IR-CCD chip. The diodes indicate diffused busses.

DETECTION OF INFRARED IMAGES (VIDICON MODE)

For infrared imaging, the IR-CCD chip was operated in a quartz optical dewar containing liquid nitrogen. A weak tungsten lamp illuminated an adjustable slit that was imaged on the IR-CCD chip with a germanium lens. The lens also served to block light of wavelength less than 1.7 μm. The charging gate was biased negatively to pinch off that channel. The integration time for infrared detection is the time between transfer pulses. The shift register runs continuously during the integration, with the first 64 bits after the transfer pulse ends comprising the video signal; only during the transfer pulse does the shift register not run. Hence, the transfer pulse width is the integration time for light detection by the shift register. Any doubt whether the video signal was caused by absorption at the shift register or absorption at the Schottky barriers can be resolved by varying the two integration times independently. Fig. 6 shows the video signal for imaging with a narrow slit and a wide slit in different locations. The signal with the narrow slit was 2 bits. Making the slit still smaller did not improve the resolution beyond this. The limitation was probably in the focusing as the shift register had sufficiently good transfer efficiency to deliver a single recognizable bit. For this chip, a transfer pulse as high as 15 V could be used without significant dark current. The optical system was focused using the video signal of a narrow slit as a guide. The slit could then be moved laterally to scan the signal across the oscilloscope screen. A photograph of the video signals with the narrow slit in four positions is shown in Fig. 7. A soldering iron tip, invisible to the human eye, easily saturated the video signal. A hotplate at 110°C could be detected with a 30-ms integration time.

It should be noted that, unlike some visible charge-coupled imagers, this IR-CCD is immune to smear and blooming. Smear occurs when imaging is performed by the shift register, and an unusually bright spot creates a significant number of carriers in a shift-register well during the short time between two consecutive clock pulses. Since our chip will not be allowed to image at the shift register, this mechanism does not apply. This is true of all CCD's of the "interline" type. Blooming

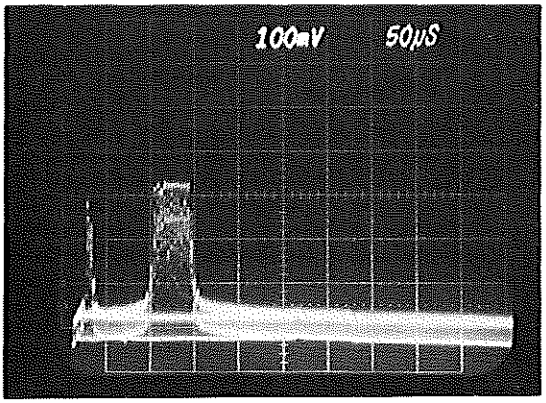

Fig. 6. Video signal for infrared imaging with a narrow slit and a wide slit. The first trace was taken with the slit smaller than 0.1 mm; the second trace was taken with the slit repositioned and set to 1.0 mm.

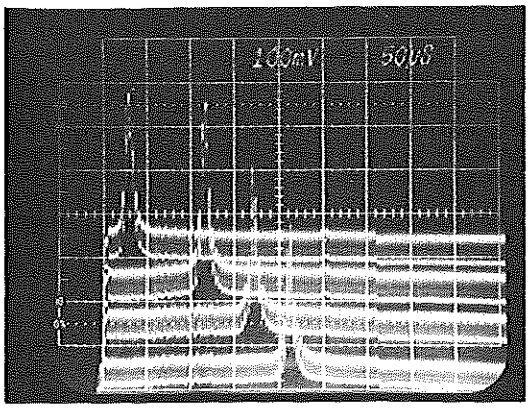

Fig. 7. Video signal corresponding to a narrow slit in four positions.

occurs when a bright spot causes a well to become overfilled with minority carriers which then transfer to adjacent wells. Again this is not possible at our shift register because we do not permit imaging there. A charge-coupled imager with separate p-n junction detectors or photogate detectors could conceivably bloom but Schottky barriers are majority-carrier devices. No minority carriers are even generated, so there is no blooming mechanism.

DEVICE UNIFORMITY

Although Schottky-barrier detectors offer the advantage of uniformity good enough for thermal imaging, this advantage would be lost if nonuniformities were introduced by the transfer process. We must, therefore, consider the consequences of the charge-coupled imager. Possible nonuniformities include those associated with substrate doping, oxide thickness, oxide charge, and accuracy of definition in the photolithographic process. A variation in doping across the array will not have any significant effect on Schottky barrier detector responsivity but will result in a variation of detector capacitance. If the device is operated in the vidicon mode, (with the detectors recharged by the shift-register wells) small differences in detector capacitances should not show up in the video signal. Of course, if dark current were a factor, doping variation would result in dark-current variation. Variations in oxide thickness or oxide charge would cause variation of the surface potential under the transfer gate, and thus would result in a variation of the level to which the detectors are set. Still, in the vidicon mode of operation, each detector is reset to its same potential at the end of each frame. The charge removed is independent of the capacitance and of the transfer level so long as the detectors are not discharged to zero. Thus, in the vidicon mode, the transfer process should not introduce any additional nonuniformities. The uniformity with which the contact holes can be defined and etched will clearly affect the uniformity of response. However, uniformity measurements on similar arrays at Air Force Cambridge Research Laboratories suggest that this will not be a problem.[6]

The uniformity obtained experimentally in the vidicon mode is shown in Fig. 8. The video signal, measured downward, is shown for seven levels of approximately uniform, germanium-filtered, tungsten illumination. Local nonuniformities of a few percent can be seen on the signals with small illumination. Slow variations across the signal are most likely due to grading of illumination. Much larger variations can be seen at high levels of illumination as some of the detectors are discharged to zero.

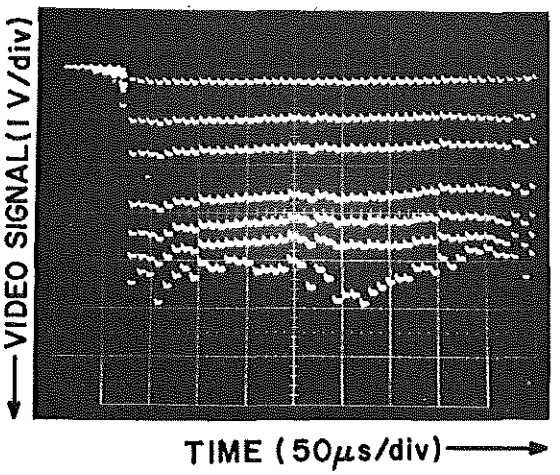

Fig. 8. Response of a typical IR-CCD in the vidicon mode to several levels of approximately uniform infrared illumination.

OPERATION OF THE BACKGROUND-SUPPRESSION (SKIMMING) MODE

In the background-suppression (skimming) mode of operation the initial Schottky barrier potential is set at the beginning of the integration period by the surface potential under the charging gate. The charge which is transferred into the CCD is determined by the surface potential under the transfer gate which is turned on at the end of the integration period when phase-1 is high, as in Fig. 3c. The voltage on the transfer gate is set so that just the "top" of the optical signal containing the signal modulation is skimmed off. The uniform background charge remains behind and is drained into the charging bus when the charging gate is turned on at the start the next integration period. In order for the skimming technique to be beneficial, the charge storage capacity of each detector must be several times that of a shift register gate. If the shift register can hold the entire detector signal, there is no reason to have it do otherwise. Indeed the skimming mode might be expected to introduce non-uniformities in the video signal because of variations in the threshold voltages of the transfer gate and the charging gate. In the vidicon mode these differences are not observed because the same gate (the transfer gate) is used to initially set the Schottky barrier potential and to remove the charge. Variations in detector capacitance can be expected to show up in the skimmed video signal as well, even in the absence of threshold variations. The devices were operated in the background suppression mode with scenes consisting of bright slits and a uniform background. For fixed optical input, increasing the potential applied to the charging gate did reduce the video signal, eventually removing the slit peaks as expected. However, since the storage capacity of the detectors in our device was smaller than the shift register well capacity, the true value of this technique could not be demonstrated. The operation in this mode was displayed more clearly with the charging circuit used to load charge in the dark. In these measurements, the charging bus was used to set the charging level with the charging gate used as a transmission gate. The relative magnitudes of the charging and transfer levels were reversed compared to Fig. 3. Here, with no illumination, that circuit is being used to create a signal. The lower the charging bus potential the more charge is loaded. Fig. 9 shows three different output signals using this mode of operation for three different charging bus potentials. The non-uniformities displayed here result from differences in the threshold voltages and detector capacitances, and contrast vividly with the uniformity displayed in Fig. 8 for the same device. Thus, while the skimming mode has been demonstrated, much better control of device uniformity will be required for practical use in this mode.

CONCLUSION

Schottky-barrier detector arrays were shown to have the uniformity required for thermal imaging with sufficient sensitivity for use in the staring mode. Calculations indicate that thermal imaging is possible in the 3 to 5 μm region with noise-equivalent-temperature of a fraction of a degree K. A charge-coupled imaging array using palladium-silicide Schottky-barrier detectors has been designed, fabricated, and tested. Thermal scenes as low in temperature as 110°C were imaged. It was shown theoretically that in the vidicon mode of operation, non-uniformities in the transfer process and in detector capacitance do not degrade the video signal, and good uniformity was indeed obtained in this mode. A scheme for removing

the background signal from the detectors before loading into the CCD was incorporated into the design of the chip, and operation in this mode was also demonstrated. This imager, though made with a single level of metallization with gaps, had reasonably good transfer efficiency and is immune to smearing and blooming.

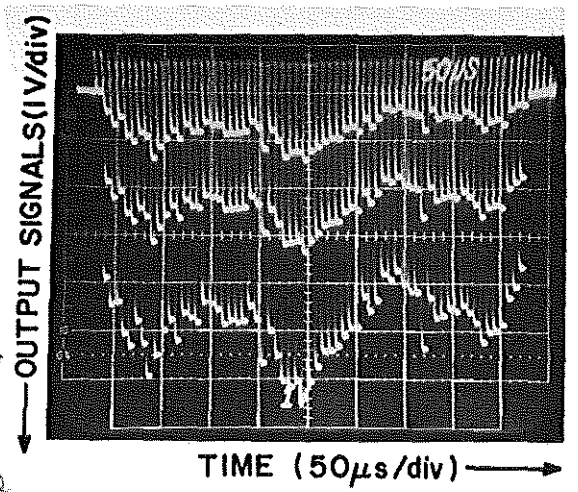

Fig. 9. Output signals from shift register with charge loaded into the unilluminated detectors from the setting diffusion. The largest output signal corresponds to the lowest setting potential. The transfer level was the same for all three cases. The device was the same one used for Fig. 8.

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