108 element, 30 frames/sec 50% duty cycle.
Video B.W. ≈ 28KHz.

10:43 – 10:58 presentation.

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*A CCD MULTIPLEXER WITH FORTY AC COUPLED INPUTS

S. P. Emmons and T. F. Cheek, Jr.
Texas Instruments Incorporated
Dallas, Texas 75222

J. T. Hall, P. W. Van Atta and R. Balcerak
Night Vision Laboratory
Fort Belvoir, VA 22060

ABSTRACT The performance of a buried channel CCD multiplexer with forty floating diffusion inputs [1, 2] is described. Features include: (1) Single-stage, low noise preamplifiers fabricated on the CCD chip and interfaced with each input at a nominal power of 25 μW per channel; (2) ac coupling between preamps and CCD on the monolith with low frequency response adequate for slow scan FLIR applications; (3) CCD input bias maintained by periodic reset (dc restore) with measured sag rate of 166 μV in 8.3 msec.; (4) anti-aliasing characteristics of the combined preamp-CCD input measured to be excellent and adequate for FLIR applications.

Overall ac dynamic range of 50 dB was measured. Ac coupling suppressed by 20 dB dc input variations such as would result in a direct coupled system from average background temperature changes, detector bias non-uniformities, and cold finger temperature fluctuations. Frequency response data on ac coupling circuitry is presented. Channel-to-channel crosstalk due to CCD CTE was measured to be less than -40dB at the 4 MHz output data rate.

I. INTRODUCTION

Charge coupled devices (CCD's) have been recognized as a potential means of performing signal processing functions in HgCdTe FLIR systems, for example: multiplexing, delay-and-add, data storage, and scan conversion. In recent months, increasing interest has been directed toward integration onto the same monolith of, not only the CCD's and their driver electronics, but also the interface circuitry between the HgCdTe detectors and the inputs to the CCDs. Total integration of the interface circuitry would make placement of the signal processing electronics on the focal plane an option available to the system designer.

A number of requirements on the CCD and its interface circuitry in an 0.1 eV HgCdTe system result from characteristics common to many IR detector-array systems.

(1) The detector noise bandwidth exceeds the required video bandwidth, a condition that can produce undesirable aliasing of high frequency noise in a sample-data system.

(2) The dynamic range requirements at the detectors (focal plane) is severe in 8 to 14 μm systems because of ambient background variations, detector non-uniformities, and "cold-finger" temperature fluctuations, in addition to the variations in irradiance associated with the viewed scene. Non-uniform response to the background also represents coherent or "fixed pattern" noise at the detector array which is large relative to "signal" because of the low contrast in real scenes.

(3) The charge transfer inefficiency (CTI) of a CCD is a potential source of image MTF degradation, an effect which in a multiplexer system is referred to as channel-to-channel crosstalk.

Techniques to circumvent the first two problems outside the detector/dewar are relatively straightforward; for example: RC filtering and ac coupling. However, the large coupling capacitors, necessary for low frequency response as well as for band-limiting of detector noise, are not

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compatible with either monolithic integration or physical placement within the dewar. The device described in this paper is a 40 input buried channel multiplexer designed specifically for compatibility with slow scan FLIR applications. It incorporates input circuitry which, together with its low CTI, represents viable solutions to the three problems listed above.

II. MULTIPLEXER DESIGN

A. Buried Channel CCD for Basic Shift Register

The basic functional design of the 40 input multiplexer is illustrated in block diagram form in Figure 1. The nucleus of the multiplexer is a 40-stage four-phase poly-Si/Al shift register fabricated by conventional ion-implant buried-channel processing. Simultaneous parallel inputs are made to each stage via 40 floating diffusion inputs [1, 2] each of which is preceded by a single stage MOSFET preamp which is ac coupled to the control gate of the floating diffusion input. A more detailed schematic is shown in Figure 2. The floating diffusion inputs and preamplifiers were masked from the ion implant to maintain surface channel characteristics.

The interchannel crosstalk due to charge transfer inefficiency, ICR, is defined as the ratio of the amount of charge that is lost into the primary packet by other charge packets to that of the primary charge packet when measured at the output. Since inputs are made to every stage, the interchannel crosstalk can be written as

$$ICR = k\varepsilon + \frac{[k\varepsilon]^2}{2!}$$

where the first term is due to the charge packet initially at position k - 1 and the second term is due to the charge packet initially at position k - 2. Epsilon, ε, here denotes the fractional loss per stage and is equal to the loss per transfer, CTI, times the number of phases.

B. The Floating Diffusion Input as an Anti-Aliasing Filter

The structure of the floating diffusion (FD) input is shown in Figure 3. In simple terms, the technique involves first setting the intermediate node to a voltage dependent on the signal voltage applied to the first transfer electrode, then setting it to a second level dependent on a reference pulse applied to the second transfer electrode. The second process is accomplished through transfer of charge into the receiving CCD well; as such, the charge introduced is derived from the difference in the two preset levels multiplied by the capacitance of the floating node and is insensitive to threshold voltage (V_T) to the extent that V_T is the same under the closely spaced electrodes.[4] The noise characteristics of this input are known to be approximately described by kTC.[2, 5]

The first process in the two step sampling operation of the floating diffusion input is essentially the "fill-and-spill" or "potential equilibration" [1, 6, 7, 8] procedure applied to a diffusion instead of a CCD or MIS node. This process is initiated by pulsing the input diode negatively (for an N channel CCD) to introduce excess charge onto the diffused node and then returning it to a high positive value to extract charge from the node while the channel current is controlled by the signal voltage applied to the input gate (Vg_1). The process is terminated by the pulsing of the second gate, which, for a multiplexer, is the serial-parallel transfer electrode. It can be shown that for noise, the time interval associated with the first process constitutes an effective integration time, τ, and the input acts to band limit the noise.[9, 10] Details of this analysis are contained in another paper at this conference listed here as reference [10]. The band-limiting effect approaches the sinX/X of an ideal integrator where $X = \pi T_c/\tau$ and T_c is the reciprocal of the input data rate.

C. Monolithic AC Coupled Preamplifier for Background Suppression

Because of the impracticality of introducing large discrete coupling capacitors into the dewar, focal plane processing of HgCdTe photoconductor signal is usually associated with a direct-coupled system. The severe dynamic range requirements on the CCD and any interface circuitry due to background radiation, together with the "fixed pattern" noise, were identified in Section I. Because of the very high impedance associated with the gate of a monolithic MOSFET, however, it becomes feasible to achieve acceptable low-frequency

time constants allowing ac coupling on-chip. A proposed structure, shown in Figure 4, relies on periodic reset techniques to maintain bias stability. System considerations for the reset are similiar to those associated with dc restore techniques in FLIR systems. One might set the dc bias level prior to each sweep of the IR scan mirror and then allow ac variations about this dc level; therefore, it is desirable for this level to change less than, say, several gray shades; for the 30 frame-per-second 2:1 interlace FLIR with nominal gain between detector and this point of 1500, the required sag is 300 μV in 8.3 msec assuming 50% scan efficiency. From a design standpoint, a capacitor value of 2 pF is required based on a diode leakage current of 10 nA/cm^2 and a typical source drain diffusion area of 4 x 10^{-6} cm^2. This value is the total capacitance to ground of the input node; that is, C is C_{couple} (Fig 4) in parallel with the FD input gate capacity, the MOS reset drain capacity and the stray capacity. We selected $C_{couple} \simeq 2$ pF and had planned to hold other capacities ≤ 0.2 pF to avoid attenuation in a capacitive voltage divider.

In the final design, a preamplifier with a design gain of six preceded the coupling capacitor. An overall gain of at least four between preamp input and FD input gate was desired after the divider attenuation mentioned in the preceding paragraph. The preamplifiers were of a single stage MOSFET design, as shown in Figure 2, where the W/L ratio of the drain load MOSFET was planned to be 1/6 that of the active input MOSFET.

III. EXPERIMENTAL RESULTS

Provisions were made by metal mask variation to separate the multiplexer with its 40 FD inputs from the ac coupled preamps for independent evaluation of the multiplexer. Characteristics of the preamplifiers and ac coupling were inferred by comparing the combined operation with that of the multiplexer by itself.

Table I
Buried-Channel Multiplexer
With Floating Diffusion Inputs

CTE (@ 4 MHz)	0.99996
Crosstalk (Worst-case)	-44 dB
Output Capacitance	0.24 pF
Source Follower Gain	0.5
Overall Gain	1
Noise (100 kHz input rate)	
Output Spot Noise	1.85μV/$\sqrt{Hz}$
Output Wideband Noise (50 kHz)	0.41 mV
Maximum Output Swing (P-P)	0.15 V
Dynamic Range	51 dB
Low Frequency Noise Corner	500 Hz
Equivalent Input Spot Noise	1.85μV/$\sqrt{Hz}$
Wideband Input Noise (50 kHz)	410μV

A. Buried Channel Multiplexer With Forty Floating Diffusion Inputs Only

Data presented in Table I summarizes the results obtained on the device of Figure 2 without the ac coupled preamplifiers; inputs were directly to the first gates of the FD inputs.

The CTE was measured to be at least 0.99996 at 4 MHz output data rate (which corresponds to an input data rate of 100 kHz) with a corresponding -44 dB crosstalk measured for the input farthest from the output end. The design goal of 40 dB isolation was achieved.

The output capacitance was measured to be 0.24 pF. The source follower output associated with the serial output (see Fig 2) showed a gain of 0.5. This loss value was attributed to the small value of load resistor (10K) necessary to achieve 4 MHz operation. The overall small signal voltage gain of unity, obtained by comparing the demultiplexer output rms voltage of a given channel with the rms value applied to the corresponding FD input, combined with the measured source follower gain and output capacitance, allowed calculation of an equivalent input capacitance of 0.48 pF.

Noise data were taken. An output spot noise (spectral intensity) of 1.85 μV/$\sqrt{Hz}$ was obtained for a typical demultiplexed channel (demux sample rate equal to 100kHz) in the "white" region of the spectrum from which an rms wideband value (over the

Nyquist bandwidth) was calculated to be 0.41 mV.

A saw tooth waveform was applied to a typical channel and compared to its demultiplex output as depicted in Figure 5. The maximum peak to peak undistorted output voltage was determined to be approximately 0.15 volts from which a dynamic range of 51 dB was calculated. The system requirement was 40 dB.

By observation of the output spot noise, the low frequency (1/f) noise corner was determined to be approximately 500 Hz.

Table II
Buried-Channel Multiplexer With Preamps AC Coupled Using DC Bias Reset

Overall Gain	2.0
Noise (100 kHz Input Rate)	
Output Spot Noise	$2.0\mu V/\sqrt{Hz}$
Output Wideband Noise (50 kHz)	0.46 mV
Maximum Output Swing (P-P)	0.15 V
Dynamic Range	50 dB
Low Frequency Noise Corner	1000 Hz
Equivalent Input Spot Noise	$1.0\mu V/\sqrt{Hz}$
Wideband Input Noise (50 kHz)	220μV
Input dc Dynamic Range	76 dB

B. Buried Channel Multiplexer With Preamps and Periodic Reset

The data of Table II characterize the buried channel device of Table I with the addition of ac coupled preamps. The preamps, coupling capacitors, and bias reset circuitry were also protected from the ion implant and therefore have surface channel characteristics.

Comparison of Tables I and II suggests that the nominal gain of the preamps, as attenuated by a possible capacitive voltage divider effect at the ac coupled node, was two.

Since output "white" noise and maximum undistorted output swing were essentially unchanged, it can be concluded that the combination of ac coupled preamplifier and bias reset circuitry made negligible contribution to the noise in the "white" spectral region. Data taken on MOSFETs of similar geometry or similar bias conditions are consistent with this conclusion and further suggest that the slightly higher low frequency corner listed in Table II was not due to the preamp.

An extra term, Input DC Dynamic Range, has been added to Table II. It is defined as the ratio of the maximum change in DC voltage applied to the input to the preamplifier (while maintaining undistorted small-signal ac response) divided by the equivalent input wideband noise voltage.

The value of 76 dB was determined by superimposing a small sawtooth signal on a variable input dc level and recording the range over which the output waveform was essentially undistorted and the gain was substantially constant. A very important result is that the input dc dynamic range is approximately 20 dB larger than the output ac dynamic range. Another stage of preamplification with bias reset should increase input dc dynamic range even further. This "dc dynamic range" is a measure of the suppression of background effects due to the ac coupling. It is limited only the maximum dc response of the preamplifier.

The total current drain on the preamp supply $V_{DD\ in}$ was measured to be 100μA, or 2.5μA per channel, indicating a power dissipation of 25 μW per channel.

C. Low Frequency Characteristics of AC Coupling With Bias Reset

The ac coupling with its bias reset MOSFET circuit is illustrated schematically in Figure 4 and in Figure 2 in relationship to the 40 input multiplexer. While the data for Tables I and II were being taken, the test circuitry was adjusted so as to apply a pulse (ØR) to the gate of the bias reset transistors every 8.3 msec. As pointed out in Section II.C, 8.3 msec corresponds to the nominal read-in time for an entire horizontal line of parallel-scan FLIR video. During this bias reset interval, the ac components of the input signals were grounded using the set up of Figure 6 to simulate the condition of the detectors viewing a uniform background.

Using this technique one would predict that the low frequency gain suppression effects of a periodic series clamp would not be evident. Without input clamping as in Fig 6 the output signal became chopped up near the

reset rate and quickly went to zero for frequencies below the reset rate.

Using the 8.3 msec restore rate the frequency response curve of Figure 7 was obtained. The rolloff at 0.2 Hz was only -1.6 dB. The high frequency data was a smooth rolloff in sinX/X fashion to zero at 100 kHz and was limited by the sample and hold. A more detailed study is contained in reference [10] presented at this conference.

An experiment was deviced to measure the sag rate directly. With the 8.3 msec reset interval the sag on the envelope of the output waveform and on the demultiplexed output was impreceptable. By increasing the interval between the bias resets to values much larger than normally required the sag rate became discernable. A typical demultiplexed waveform is shown in Figure 8. The sag rate was consistent and appeared linear in several repetitions of the experiment. An output sag rate as low as 0.02 V/sec was measured on one device. Since the slope of the sag was linear, denoting a leakage current or an RC decay with a time constant much longer than 1.3 seconds it is appropriate to interpolate the sag in an 8.3 msec interval as only 166 μV. Even at these low restore rates a 2 Hz signal could be processed riding on the linear sag.

D. Anti-Aliasing Characteristics of the Combined Floating Diffusion-Preamplifier Circuitry

Preliminary experiments were conducted to evaluate the bandlimiting nature of the floating diffusion input in combination with the ac coupled preamplifiers. Data indicated effective bandlimiting of otherwise unbandlimited input noise with negligible resulting aliasing.[10]

IV. CONCLUSIONS

The performance of the 40 input multiplexer was adequate for many slow scan FLIR applications. The use of monolithic ac coupling with dc bias reset maintains good low frequency response below 2Hz. This reset, when synchronized to detector signals from a uniform background, will allow system dc restoration on a frame basis. This effectively increases dynamic range by 20 dB by eliminating dc input variations from average background temperature changes, detector bias non-uniformities, and cold finger temperature fluctuations.

Channel to channel crosstalk was maintained less than -40 dB at 4 MHz data rate by the high CTE of buried channel design without the use of isolation inputs.

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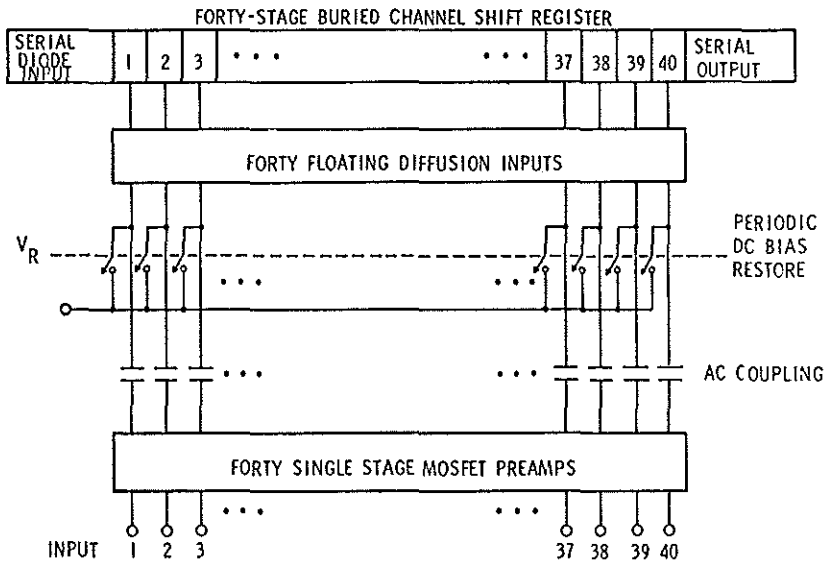


FIGURE 1. BLOCK DIAGRAM OF 40 INPUT MULTIPLEXER WITH PREAMPLIFIERS

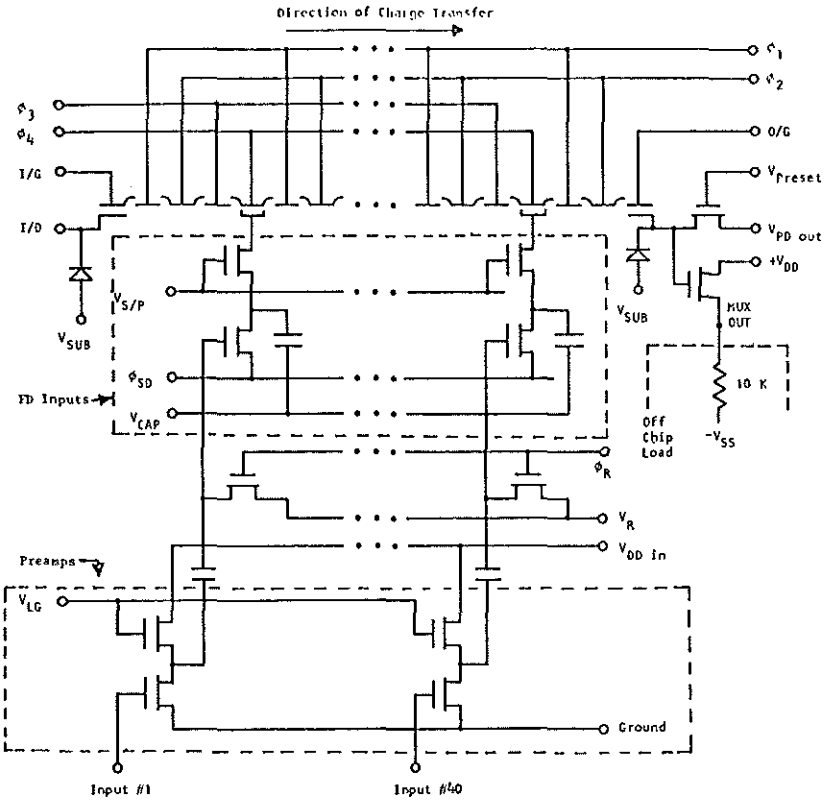


Figure 2 Schematic of Chip With Preamps, Bias Reset, and FD Input

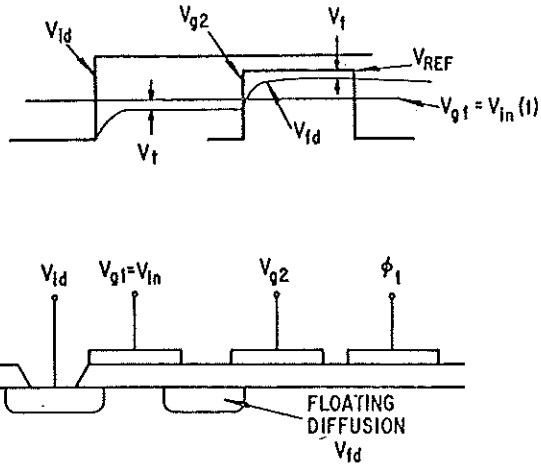


Figure 3 Floating Diffusion Input Structure Consisting of Input Diode (Connected to V_{id}), First Transfer Electrode (Connected to V_{g1}), Second Transfer electrode (Connected to V_{g2}), Floating Diffusion (Between the Two Transfer Electrodes), and ϕ_1 Electrode. The waveforms required to operate the floating diffusion are shown.

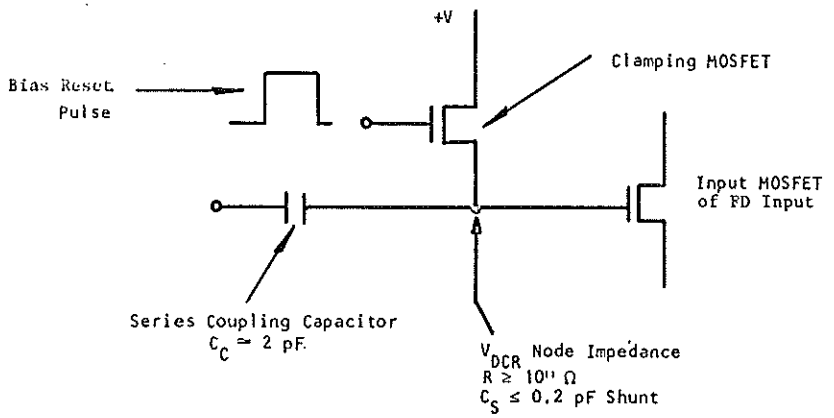
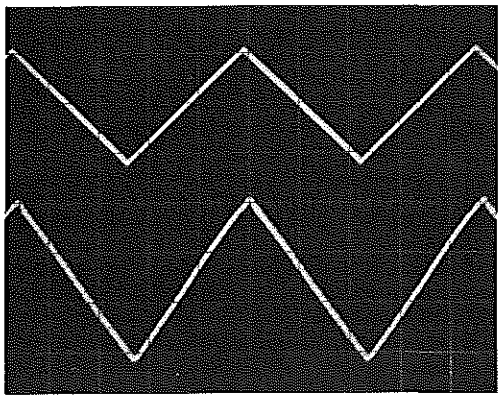


Figure 4 Schematic of AC Coupled Monolithic Node With DC Bias Reset



Input Waveform

Demultiplexed
Output Waveform

0.1 μsec/cm

Figure 5 Typical Waveforms Used To Determine Maximum Undistorted Output Swing of Multiplexer

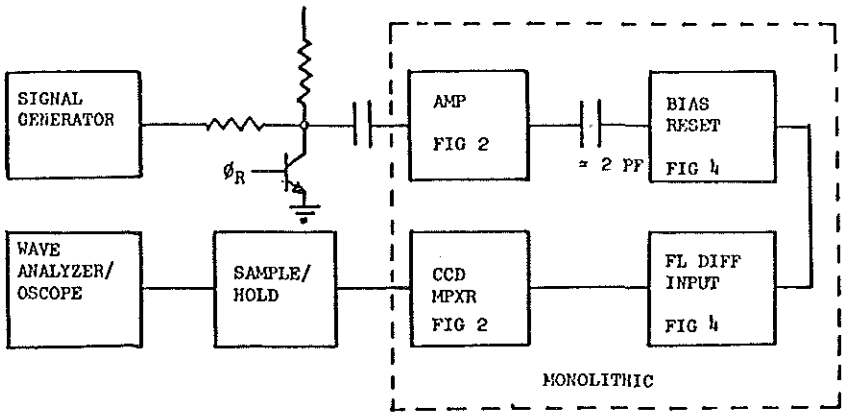


Figure 6 Block Diagram of Test Setup Showing Input Signal Clamping

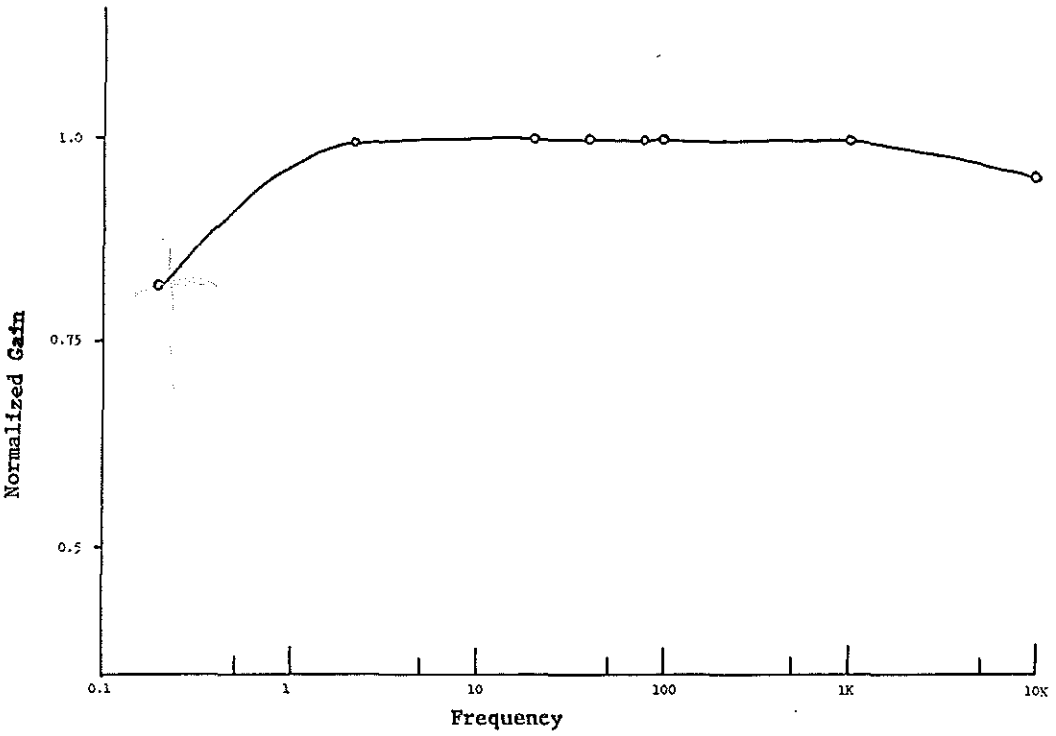


Figure 7 Frequency Response of AC Coupled Multiplexer With Bias Reset Every 8.3 msec

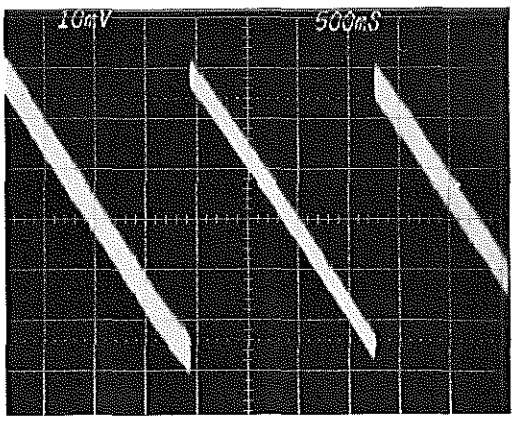


Figure 8 Demultiplexed Output Showing Sag Between Bias Resets

University of Iowa data
not available.