A CCD ANALOG MEMORY SYSTEM FOR SLOW-SCAN CONVERSION OF STANDARD TV VIDEO

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ABSTRACT

A novel approach for accomplishing the frame rate reduction of standard TV video has been demonstrated with commercially available charge-coupled devices (CCD). The basic design concept has been verified using two 128 x 128 element CCDs, but the technique described may be easily expanded to meet increased resolution requirements.

The system input is EIA compatible, composite video. After extraction of vertical and horizontal sync pulses, portions of the remaining video are clocked into CCD analog shift registers at standard video line rates. At the end of an input field, the video is clocked out at a reduced rate that results in a fast-to-slow scan conversion. Sync pulses at the slow data rate are then added to the low frequency output signal to create composite video as the final output.

The logic control for the slow scan system is as elegant as it is simple. In breadboard form, only 130 cm^2 of TTL components are required for the fast-to-slow conversion. Implementation details are presented as well as test results obtained on the breadboard system which transforms the standard EIA composite waveform at 30 frames per second to an output of 5 frames per second.

INTRODUCTION

The abounding number of CCD imagers that have appeared on the market in recent years have become competition for more conventional vacuum tube imagers, e.g., vidicons, orthicons, etc. The goal of the CCD manufacturers would seem to be that of obsoleting its predecessors. Although this indeed may occur in the not too distant future, the momentum achieved by the vacuum tube counterparts will not be curbed over night. It is therefore the goal of some workers in the field to seek out new applications for CCDs, not with the intent of replacing other imagers, but rather to find new ways of using this relatively new device. In the topic to be covered by this paper, the CCD is used along with a conventional vidicon to provide unique as well as useful results.

More specifically, it is the intent of this offering to present a scheme by which portions (or all) of an EIA compatible video frame can be put into a standard imaging type CCD and then clocked out at a reduced rate to achieve an effective bandwidth reduction. The usefulness of such a device is limited only by one's imagination. Data link applications for military use, picture phones, and video records played on a standard phonograph are but a few of the possible applications.

The implication here is not that scan converters are new. The important point is that the CCD with its volume, weight, and power characteristics, makes an ideal candidate for the main component of a modular scan converter, requiring nothing from the input video but the composite signal itself.

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The first phase of the scan converter operation, that of converting the composite TV signal to CCD format and filling the analog shift register, is significant because of its other applications. This subtopic will be covered briefly.

DEVICE DESCRIPTION

Although the concepts covered here are equally valid for any CCD equipped with an electrical input capability, the actual hardware implemented in conjunction with this paper was centered around two 128 x 128 element frame-transfer devices manufactured by Fairchild Semiconductor. A complete description of this device is given elsewhere (Ref. 1), but a few of its more relevant features are presented here. The input function is accomplished using the low noise "fill-and-spill" method (Ref. 2) to a 128 element horizontal input register. SPS (serial-parallel-serial) organization leads to a single-line output register which receives charge from the area array via an output transfer gate. A low noise threshold floating gate amplifier (Ref. 3) is located at the end of the output register to interface the CCD with the off-chip video processing electronics. This device has an average dark-current density of 10nA/cm^2 and a charge-transfer efficiency of .9995. The noise equivalent signal from the FGA is advertised to be less than 100 electrons/pixel at a clock frequency of 1 MHZ. The device has provisions for clocking the input and output registers separately.

SYSTEM DESCRIPTION

U. S. television systems generally conform to the Electronic Industries Association (EIA) standard RS-170 (Ref. 4) with regard to composite picture format. Although the details of the timing format are not important to the scan converter concept, knowledge of the line and field time of 63.5 μs and 16.7 ms, respectively, are basic to the understanding of the block diagram shown in Figure 1. Also, fundamental to the operation of the system is the existence of horizontal and vertical sync pulses within the video, i.e., composite video.

The approach used to demonstrate the feasibility of this concept was to use two 128 x 128 element CCDs to read-in every twelfth field of incoming video and read the video out during the remaining eleven fields. The resulting field rate is reduced from sixty to five per second.

Referring to Figure 1, the input video is exposed simultaneously to a sync separator and low-pass filter. The latter serves to limit the video bandwidth to a value slightly below the input sample rate to reduce aliasing effects in the output. The vertical sync pulse from the input video is divided by twelve to establish the basic reduction factor. The horizontal sync pulse is used as the clock for the vertical registers of the CCDs during the input phase. This sync pulse is also used to turn on and off a 2.5 MHZ gated oscillator which forms the CCD horizontal input clock. Alternately, a phase-lock-loop could provide this function, but a gated oscillator designed to start in the proper phase and at the correct frequency can be implemented with much fewer components. Since the 128 x 128 device requires an input sample clock that is in phase with but more narrow than the horizontal clock pulse, a monostable multivibrator is used as shown.

The 200KHz oscillator provides the horizontal output clock, its frequency being determined by the requirement to clock out one line of video in approximately 700 microseconds. After 150 of these clock pulses have been counted, an output horizontal sync pulse is derived which disables the oscillator.

It can be seen then, that the horizontal registers, being independent parts, are operated only during read-in or read-out phases. The vertical clock, on the other hand, must be operated during both phases, with only a change in rate from input to output. Using two CCDs, each responsible for handling one-half of a field, further complicates matters. The diagram shows how these problems are handled in this hardware implementation. A switch operated from the divide-by-twelve counter determines whether fast or slow vertical clock pulses are required. The two series counters, divide-by-128 and divide-by-two, enable the proper CCD for the half-field being processed, and determine when both CCDs are full (or empty).

The outputs of the two CCDs are multiplexed, amplified, and peak-detected to reduce clock noise in the output. The final step in the process is to add the vertical and horizontal sync pulses to the output video to produce the composite signal.

ADAPTABILITY TO SPECIFIC REQUIREMENTS

The breadboard model used in conjunction with this paper was constructed to show concept feasibility, and not as part of a specific requirement. However, it can now be seen that this basic idea can be applied to meet various specific resolution requirements by clocking a desired portion of the input video into the CCD or combination of CCDs. For instance, the 4.5MHz band width normally required by conventional television systems can be maintained by using either several "small" CCDs or one CCD with 480 columns and approximately 490 rows. Alternately, where specific portions of a scene are involved, a single "small" CCD could be clocked at a 9 MHz rate for that period of time which corresponds to the subscene. Another possibility would be to scan the full camera's field-of-view with a small CCD looking for specific targets while maintaining full resolution. Implementation of any of these schemes would be straight forward, involving at most an additional 100 cubic cm of additional volume.

TEST RESULTS

Figure 2 shows portions of photographs taken from monitors arranged before and after the scan converter. The slow scan monitor is, of course, a special piece of equipment. For these tests, a Sony model CT 500 monitor was modified to accept the slow composite video. The input video was displayed on a Sony model CVM 112 monitor, and the camera used was a Sony model AVC 3400, a 1.69 cm antimony trisulfide vidicon.

Figure 2A and 2B demonstrate the resolution degradation associated with using 128 discrete bins to represent a normal TV line. This is not surprising since sampling theory assigns an upper limit equivalent bandwidth of 1.25MHz (one-half of the input horizontal clock frequency) for this particular implementation. Contrast transfer function (CTF) measurements were taken that offer a more quantitative means of comparison (see figure 3).

The photographs, 2C and 2D, showing the gray-shade reproduction capability of the scan converter are not really representative of what can be seen when examining an oscilloscope pattern of the two videos, which clearly indicate ten gray-shades out of the scan converter. It is believed that the monitors used were not capable of displaying the full dynamic range capability of the camera or the scan converter.

The third set of photographs, 2E and 2F, demonstrate the apparent degradation that is encountered when viewing a typical scene.

Although no effort was made to limit volume or power consumed, all hardware for the breadboard scan converter required only 600 cm^3, which could be easily packaged in a cube 8.5 cm on a side. Power consumption on the breadboard approached 10 watts, but this number could be easily halved simply by using MOS logic instead of TTL.

OTHER APPLICATIONS

The prospect of clocking video from a standard TV camera into a CCD storage device opens up other avenues for investigation. One example is that of a moving target indicator. A CCD camera and matching shift registers have been used together as a means of detecting motion in a scene (Ref. 5). The principle of operation involves holding a frame of video in a CCD memory, and comparing that video, on a pixel-by-pixel basis, with real-time video from the imager. With the ability to transfer the vidicon video to CCD format, MTI (Moving Target Indicator) capability could be easily integrated into an existing TV system as a modular add-on. Permanent scene storage, also covered in Reference 5, is another example of using a CCD camera and CCD analog storage device that could be adapted to continuous-read-out imagers by the means described earlier in this paper.

SUMMARY AND CONCLUSIONS

A method of storing a portion of EIA compatible TV video using CCDs for temporary analog storage has been demonstrated. Implementation details that have been presented indicate only very simple circuitry is required to add a modular, easily expandable memory unit to standard CCTV (Closed Circuit Television). Test results have been obtained on an operating prototype unit. These results indicate the successful operation of a slow scan conversion system to convert standard CCTV video from 30 frames/second to 5 frames/second. Results also indicate that an efficient MTI system can be incorporated into a standard CCTV operation.

REFERENCES

1. Hunt, J., and Sandowski, H., "Diverse Electronic Imaging Applications for CCD Line Image Sensors," Proceedings of the 1975 Conference on the Application of CCDs, San Diego, Ca., October 1975; Reference also unpublished Fairchild Data Sheet.

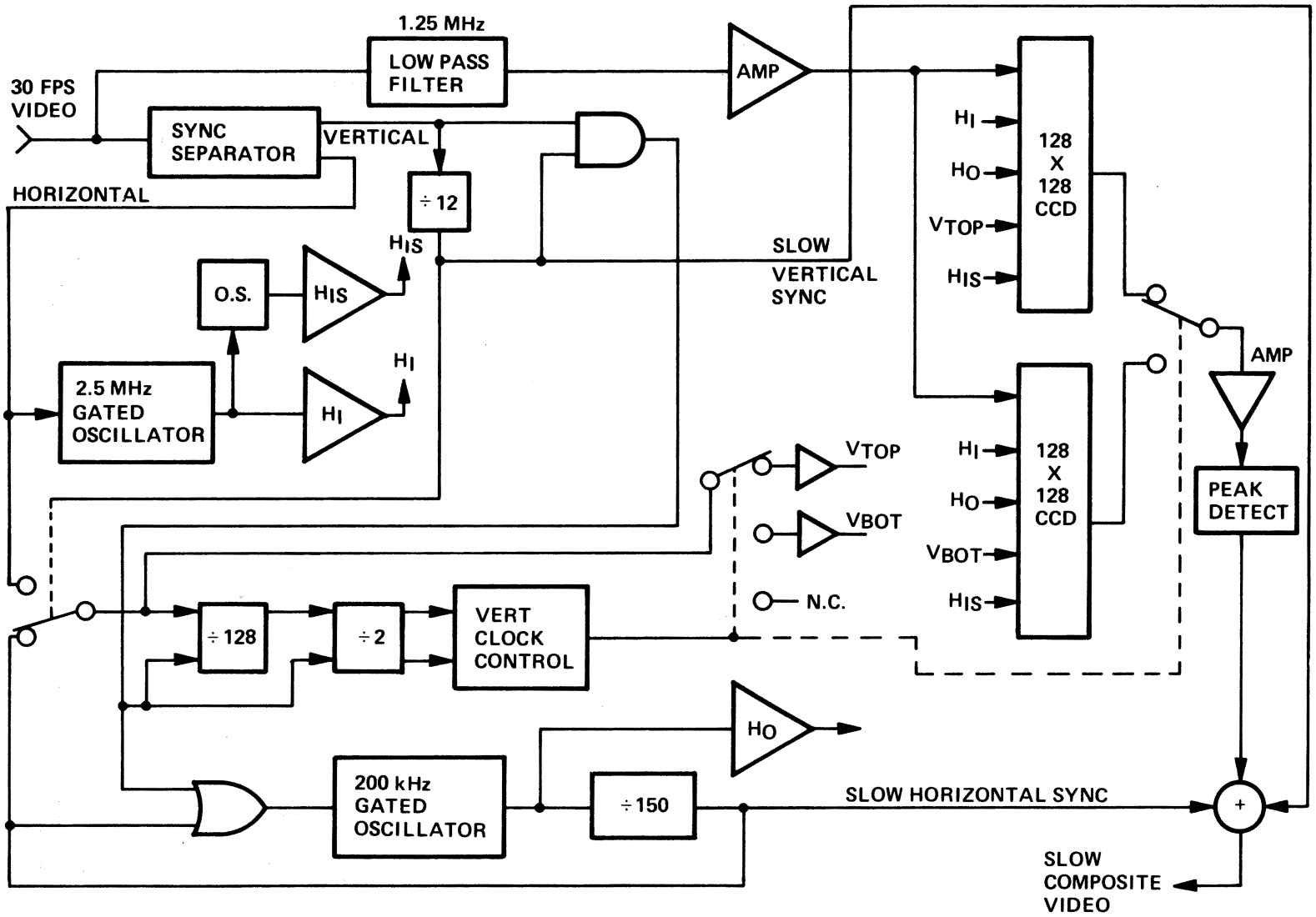
2. Sequin, Carlo H., and Tompsett, Michael F., Charge Transfer Devices (1975), Academic Press, Inc.

3. Wen, David D., "Design and Operation of a Floating Gate Amplifier," IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

4. RS-170 (Revision TR-135) November 1957, Electronic Industries Association, Standards for TV Video.

5. Buchanan, S.P., and Clark, R.R., "Signal Processing Capabilities of a 100 x 100 CCD Array", Proceedings of the International Conference on the Applications of Charge-Coupled Devices, p. 209; October 29-31, 1975.

FIGURE 1. BLOCK DIAGRAM



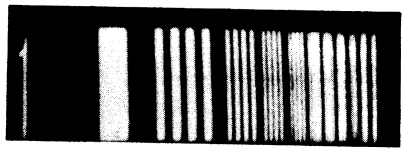


Figure 2A. Bar Pattern Input

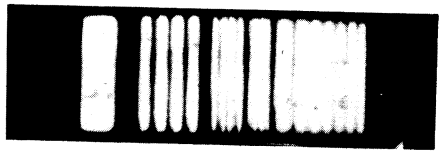


Figure 2B. Bar Pattern Output

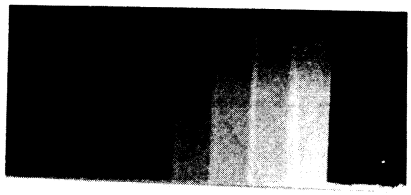


Figure 2C. Grey Scale Input

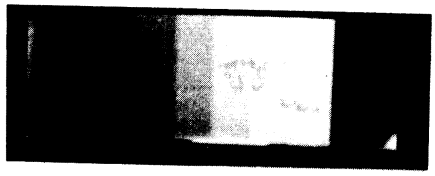


Figure 2D. Grey Scale Output

Figure 2E. Scene Input

Figure 2F. Scene Output

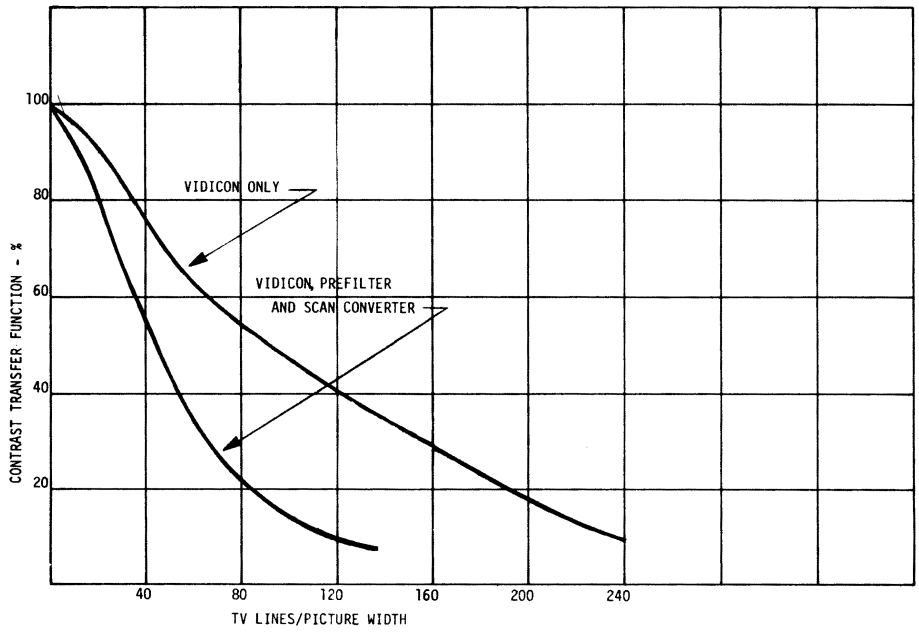


FIGURE 3. SYSTEM CTF MEASUREMENTS