AN MOS AMPLIFIER FOR CCD APPLICATIONS

N. Weste* and J. Mavor**

ABSTRACT

A key development in CCD integrated circuits is the incorporation of on-chip peripheral circuitry for signal conditioning, summing and sample-and-hold. This is conveniently realised using monolithic MOS transistors to form the gain block, preferably in the configuration of a differential-input, operational amplifier. In this paper, details of MOS amplifiers are given which have been specifically designed for CCD integration of signal processing applications. Details are also given of a chopper-stabilisation circuit to improve the usually poor temperature drift characteristics of MOS stages. The current and expected future performance of these amplifiers is presented in the CCD context. The application of these amplifiers in CCD sub-systems is reviewed with particular reference to feedback linearisation and the implementation of on-chip, active filter banks.

INTRODUCTION

In order that CCD signal processing circuits might gain a wide acceptance, they have to be easy to use and convenient to implement in larger systems. This necessarily means that the clock driving circuits, and more importantly the various level shifting, gain and sample and hold amplifiers, should be incorporated on chip (refs.1,2). At the present time most of the latter functions are performed by off-chip discrete circuitry; usually using bipolar operational amplifiers. It seems attractive, therefore, to implement operational amplifiers on the CCD chip itself. To minimise the complexity of the process, and thus maximise the yield, it is desirable to design these amplifiers using the same technology as the CCD itself. Although MOS transistors have relatively low gain, it is possible to achieve a useful gain-bandwidth product in carefully designed amplifiers. In critical applications DC drift may be minimised by using a chopper-stabilisation technique using the CCD clocks.

This paper presents the results of work carried out on the design and evaluation of CCD process compatible amplifiers which have been designed to be used in conjunction with CCD subsystems. The results show that DC stability, noise and frequency response criteria may be satisfied, for applications below 10 MHz. Provided that the configurations in which the amplifiers are used are not dependent on large open-loop gains, then the gain of these amplifiers has been found to be sufficient.

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DESIGN

Target Specification

The first amplifier designed was a PMOS amplifier that had a target specification that would enable the amplifier to be used for most on-chip tasks. These were as follows:

GAIN	200 - 1000
BANDWIDTH (OPEN LOOP)	0.5 → 1 MHz
POWER DISSIPATION	50 mW
S/N RATIO	>60 dB
CHIP AREA	<400000 sq. microns (630 μ x 630 μ)
OUTPUT IMPEDANCE	5 KΩ
OUTPUT SWING (20 V VDD)	10 V p-p
CMRR	>60 dB

PMOS Amplifier Design

The amplifier was designed for a conventional <111>, 3-15 Ω cm, P-channel digital process with threshold voltages about -2 V. The circuit diagram of the PMOS amplifier appears in Figure 1(a). It consists of two cascaded differential stages which in turn drive a source follower level shifter. This source follower drives a gain block consisting of three inverters and a source follower buffer, which provides a low impedance output driver. Two bias points set the tail currents in the differential pairs. These bias points are set externally, but on-chip biassing is quite feasible.

The PMOS amplifier was designed with a dominant pole which could be adjusted by an external capacitor, depending on the application. If desired this could be achieved on chip by a redesign of the relevant stages. In addition to the desired dominant pole, a zero was evident due to the interaction of the finite diffusion connection resistance from the compensation point to the pad, and the compensation capacitance.

The noise in the amplifier is dominated by the input stage and may be minimised by optimising the input driver transistors. Large W/L devices minimise the 1/f noise and the area of the input transistors is optimum when it equals the source capacitance. The W/L of the input transistors in this design was 25 and the input capacitance approximately 12 pF. In addition, maximising the L dimension reduces channel conductance modulation which affects common mode performance (ref.4).

NMOS Amplifier Design

Based on the results of the PMOS design an amplifier was designed on a <100>, thin oxide, n-channel process having a threshold voltage of around -1 V. (ref.3). The circuit of this amplifier appears in Figure 1(b).

In essence it is similar to the PMOS design, but the number of stages has been reduced and the gain of each stage increased. Only one bias point is needed but two substrate voltages are needed. At only one point is there an inverter driving another inverter, which provides an obvious compensation point.

Because the amplifier was designed on the Plessey "shadow etch" process it was possible to design a transistor which minimised the gate-drain overlap which, due to the Miller effect, dominates the frequency response of these amplifiers. This was achieved by placing a guard plate over the drain diffusion and placing the control gate next to this. In high gain stages this reduces the input capacitance of the stage by a factor of 2 - 5.

AMPLIFIER PERFORMANCE

PMOS Amplifier

The performance of the prototype PMOS amplifier is summarised in Table I.

TABLE I - PMOS AMPLIFIER (OPEN LOOP)

PARAMETER	
VDD	-20 V
GAIN	52 dB
BANDWIDTH (C_L = 120 pF R_L = 1 MΩ)	500 kHz
POWER DISS	20 mW
S/N RATIO 1 kHz	60 dB
CHIP AREA	302000 sq.μ (550 μ x 550 μ)
OUTPUT IMPEDANCE	3 KΩ
OUTPUT SWING	-2 V to +7 V
CMRR	74 dB
DRIFT (no compensation)	2 mV/^{o}C
DRIFT (compensation)	1 mV (10^{o}C → 70^{o}C)
SLEW RATE	0.5 V/μs
INPUT CAPACITANCE	12 pF

This shows that the desired gain has been achieved at the required bandwidth. Figure 2(a) shows the gain and phase response. The notable differences when compared to a bipolar operational amplifier are the open loop gain, drift and the output impedance. In addition, the threshold drop across the output stages limit the output voltage swing to about half the supply rail. The rms noise measured at unity gain for a 500 kHz bandwidth was 5 mV and this exhibited a 1/f type characteristic. Figure 2(b) shows this noise plotted against frequency.

NMOS Amplifier

Preliminary results for the NMOS amplifier are shown in Table II.

TABLE II - NMOS AMPLIFIER (OPEN LOOP)

PARAMETER	
VDD	15 V
GAIN	50 dB
BANDWIDTH C_L = 10 pF R_L = 10 MΩ	5 MHz
POWER DISSIPATION	100 mW
CHIP AREA	360000 sq.μ^2 (60 μ x 60 μ)
OUTPUT IMPEDANCE	500 Ω
OUTPUT SWING	-5 to +2 volts
SLEW RATE	2 V/μs

These show that the open loop bandwidth has been increased by a factor of 10, slew rate increased and the output impedance decreased at the expense of power dissipation.

STABILISATION

Operation

As was noted previously, the dc drift and associated noise is reasonably high for MOST amplifiers resulting from the 1/f type characteristic of the noise associated with MOST's. Two approaches may be used to reduce the noise. The first is to use the amplifiers in unity gain configurations, and rely on the open loop gain of the amplifiers to reduce the noise to an acceptable level. A second method involves the use of a stabilisation technique used originally for vacuum tube amplifiers, but more recently applied by Fry (ref.4) to MOST amplifiers. This chopper-stabilisation technique uses the available CCD clocks to reduce the drift virtually to zero without incurring large support circuitry overheads. The circuit used in this set of experiments is shown in Figure 3(a), although other possibilities exist.

With reference to Figure 3(a) the operation of the circuit is as follows. At the beginning of the stabilisation period, the non-inverting input of the amplifier is clamped via MOST switch T4 to common. The inverting input is clamped via capacitor C_{STORE} and switch T3 to common. At the same time full negative feedback is applied via switch T5 resulting in a non-inverting unity gain amplifier. In this configuration C_{STORE} charges to the offset voltage produced by the amplifier. Following this stabilisation period T3 and T4 are opened and T1, T2 closed, the amplifier reverting to its original configuration, with C_{STORE} subtracting the offset.

As CCD's operate in a sampled data mode, the periods where data is not sampled may be used to stabilise the amplifier. Figure 3(b) shows the stabilised output signal and a detailed photograph of the clamping period.

Figure 3(c) shows the improvement effected by using this stabilisation method.

Theory

In the analysis of the chopper stabilisation a band-limited input signal is considered. The stabilisation technique results in an output spectrum which may be considered to consist of two components - the signal and a noise contribution. The full analysis is presented in Appendix 1 resulting in a signal component given by:

$$Vo(t) = A\ v(t)\ p(t)$$

where,

$v(t)$ = input signal to stabilised amplifier

$p(t)$ = CCD clock stabilising waveform

$Vo(t)$ = output signal of stabilised amplifier

A = open loop gain of amplifier

and,
$$p(t) = \frac{L}{T} \sum_{-\infty}^{\infty} \text{sinc}\ (\frac{nL}{T})\ e^{+jn2\pi t/T}$$

where,

T = CCD clock period = $1/f_o$

L = stabilisation period ($= \frac{T}{3}$ for 3Φ CCD)

Plotted in the frequency domain this output signal is shown in Appendix 1. The DC gain is proportional to the L/T ratio which is 1/3 for a 3-phase CCD and ½ for a 2-phase CCD.

The noise component in the output is given by,

$$Gn(f) = \sum An(f)\ Gx\ (f - nfo)$$

where,

$Gn(f)$ = net output noise spectrum of stabilised amplifier,

$Gx(f)$ = power spectrum of internally generated noise, and

$An(f)$ = coefficients defined in Appendix 1.

From Appendix 1 it may be seen that Ao is multiplied by Gx(f) which in the case of the MOST amplifiers is dominated by 1/f noise. Thus it may be seen that any internally generated 1/f noise is virtually suppressed by the stabilisation procedure. The coefficient A_1 is multiplied by Gx(f - fo) which is effectively the thermal noise of the amplifier around the clock frequency. For MOST transistors this will be quite low. The net result of using a stabilised MOST amplifier in the CCD case is therefore only a slight increase in noise.

Use of Stabilisation

A few points need to be made in relation to the use of the amplifiers. A conceivable use would be in low-pass prefilters to prevent aliasing distortion at the input of a CCD (ref.5). However, the output of a stabilised amplifier filter would contain signal components about multiples of the CCD clock frequency and hence could not be used to prevent aliasing distortion. Thus for low pass filtering applications the amplifiers have to be used in a unity gain mode. Alternatively, a low stabilisation frequency (10 Hz) could be used such as Fry (ref.3), employing an L/T ratio of say 999/1000. Sample-and-hold operations have to be achieved in

a similar manner. In view of the experience gained with these amplifiers the former approach seems the most practical.

APPLICATION OF AMPLIFIERS

Low-Pass Filters

The PMOS amplifiers were used in a second-order low-pass Butterworth filter, which has a designed 3 dB point of 5 kHz. This filter was compared with a filter which used a 741 type operational amplifier. Figure 4 shows the responses of the various filters including a simulated results using SPICE 2 (ref.6). Note that the PMOS amplifier filter used smaller capacitor values to minimise the phase shift introduced, due to the finite output impedance of this amplifier. When the capacitors are too large a net phase shift occurs, which changes the polarity of the feedback thus causing an increase in the response at high frequencies. However, with small capacitor values (as would be implemented on-chip) this effect is minimised. The NMOS amplifier shows this effect to an even smaller extent due to its lower output impedance. The amplifiers operated with a gain of approximately 1.4 which applies sufficient negative feedback to reduce the noise to about 5 mV rms.

Another observed difference between the bipolar amplifier and the PMOS amplifier filters was a slight difference in pass-band gain.

Summing Amplifier

A circuit which represents a typical CCD signal processing sub-system is shown in Figure 5(a). This circuit is a form of Hilbert transformer, which derives two sine waves in quadrature over a range of frequencies. In a more developed form it could form the basis for SSB generation and detection and for quadraphonic demodulation. However, as a representative model of a wide range of other CCD analogue systems, it shows operational amplifiers used as summing amplifiers and sample-and-hold amplifiers. The calculation of the tap weights (and description of a similar circuit) is described elsewhere (ref.7).

The system shown in Figure 5(a) was constructed and tested using internally compensated bipolar operational amplifiers and the PMOS amplifiers. Figure 5(b) shows the impulse response of the phase shifter using the MOST amplifiers (the slight discrepancies in weighted levels are due to misalignment errors in the fabrication of the CCD). Figure 5(c) shows the two generated sine waves, which are shifted by approximately 90^{o}. The finite gain of the PMOS amplifiers resulted in a slight amplitude drop in the output compared to the bipolar case. The bipolar amplifiers have also a higher output drive capability. Despite these observations the operation of both systems - bipolar and PMOS - was substantially similar.

Linearisation

A useful application for these MOST amplifiers would be for the linearisation of the CCD transfer function (ref.8). In this configuration, the quantity of charge injected into the CCD is non-destructively sensed, and this signal used as feedback to control the charge being injected via a differential amplifier. An open loop gain of 100 is sufficient for many applications of this technique.

CONCLUSIONS

It has been shown that it is possible to implement MOS amplifiers that will perform most of the signal conditioning functions on the same chip as the CCD itself. In particular, low pass filters have been realized which could be used for on-chip pre-filtering and comparable performance to bipolar low pass filters has been achieved.

Drift may be reduced to a negligible level by using a chopper stabilisation technique which adds a minimum of amplifier generated noise to the processed signal.

It has been shown that an increase in frequency performance may be achieved by using an NMOS process and this may be further enhanced with specially designed transistors. Using a circuit analysis program (SPICE 2) it is possible to estimate the performance of an optimised amplifier which indicates gains of the order of 1000 and unity gain bandwidths of 30 MHz, combined with power dissipations of 50 mW.

With amplifiers similar to that described, the level of integration in CCD analogue systems may be increased substantially while maintaining the simplicity of the CCD process. Thus the component count, and hence cost, of a complex signal processing system may be kept to a minimum.

ACKNOWLEDGEMENTS

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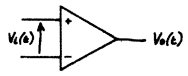
APPENDIX 1

Stabilisation

1. Model the amplifier as follows



Vo(t) = AVi(t) + x(t)

where A = amplifier gain

Vi(t) = signal input = $V^+ - V^-$

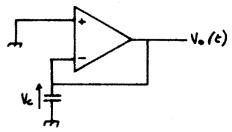
x(t) = amplifier noise = DC offset + drift + $^1/f$ noise + white noise

Vo(t) = output voltage

Assume during clock phase Φ1

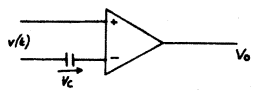
Vo = Vc = A (-Vo) + x(t)

$\therefore$ Vo(t) = $\frac{x(t)}{1 + A}$



During clock phase Φ2

Vo(t) = A (v(t) - Vc) + x(t)



Now let p(t) = 1 during Φ2

p(t) = 0 during Φ1

where p(t) = CCD clock sequence

Hence

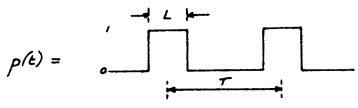
$$Vo(t) = [A (v(t) - Vc) + x(t)]p(t) + \left[\frac{x(t)}{1 + A}\right] (1 - p(t)) \quad (1$$

where Vc = $\frac{x(t')}{1 + A}$ t' is the beginning time of pulse p(t).

2. Signal Component

From (1)

Vo(t) = A v(t) p(t)



For pulse waveform p(t)

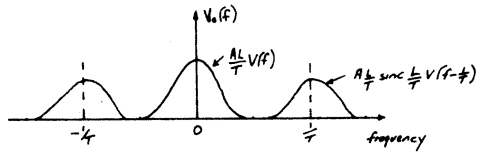
$$p(t) = \frac{L}{T} \sum_{-\infty}^{\infty} \text{sinc } \frac{(nL)}{T} e^{jn2\pi t/T}$$

$$= \sum_{-\infty}^{\infty} C_n e^{jn2\pi fot}$$

where $C_n = {}^{L}/_{T} \text{ sinc } \frac{(nL)}{T}$

fo = $^1/T$

which may be represented by



Thus for $\frac{L}{T} = \frac{1}{3}$ the DC gain is $\frac{A}{3}$ and the "gain" at $\frac{1}{T} = \frac{2A}{3\pi}$

3. Noise Component

From (1)

$$n(t) = \left[-\frac{A}{1+A}\, x(t') + x(t) \right] p(t) + \frac{x(t)}{1+A} [1 - p(t)]$$

$$= x(t)\, q(t) - w(t) \qquad (2)$$

where $q(t) = \frac{1}{1+A} + \frac{A}{1+A}\, p(t)$

$$w(t) = \frac{A}{1+A}\, x(t')\, p(t)$$

Consider a component $e^{j2\pi ft}$ of $x(t)$.

Thus

(a) $\frac{x(t)}{1+A} = \varepsilon e^{j2\pi ft}$ where $\varepsilon = \frac{1}{1+A}$

(b) $(1 - \varepsilon)\, x(t)\, p(t) = (1 - \varepsilon)\, e^{j2\pi ft} \sum C_n e^{jn2\pi fot}$

(c) $(1 - \varepsilon)\, x(t')\, p(t) = (1 - \varepsilon) * [x(t) * \text{combfunction}]$ passed through a filter with $h(t) =$

Thus $x(t) * \text{combfunction} = \frac{1}{T} e^{j2\pi ft} \sum e^{jn\pi\frac{L}{T}} e^{jn2\pi fot}$

and $x(t')\, p(t) = \frac{1}{T} e^{j2\pi ft} \sum H(f + nfo)\, e^{jn\pi\frac{L}{T}} e^{jn\pi fot}$

where $H(f) = \frac{1 - e^{-j2\pi fL}}{j2\pi f} = L\, \text{sinc}\,(Lf)\, e^{-j\pi fL}$

hence from (2)

$$n(t) = \sum a_n e^{j2\pi(f + n\, fo)t}$$

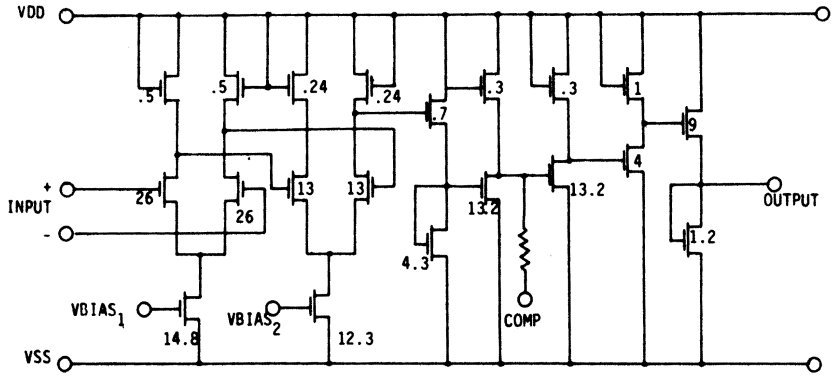


Figure 1(a). PMOS Amplifier ($^{W}/_{L}$ values shown)
(UA7501)

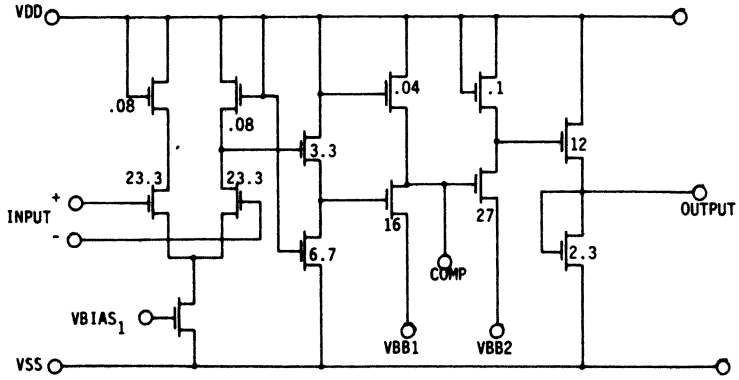


Figure 1(b). NMOS Amplifier
(M550A-N)

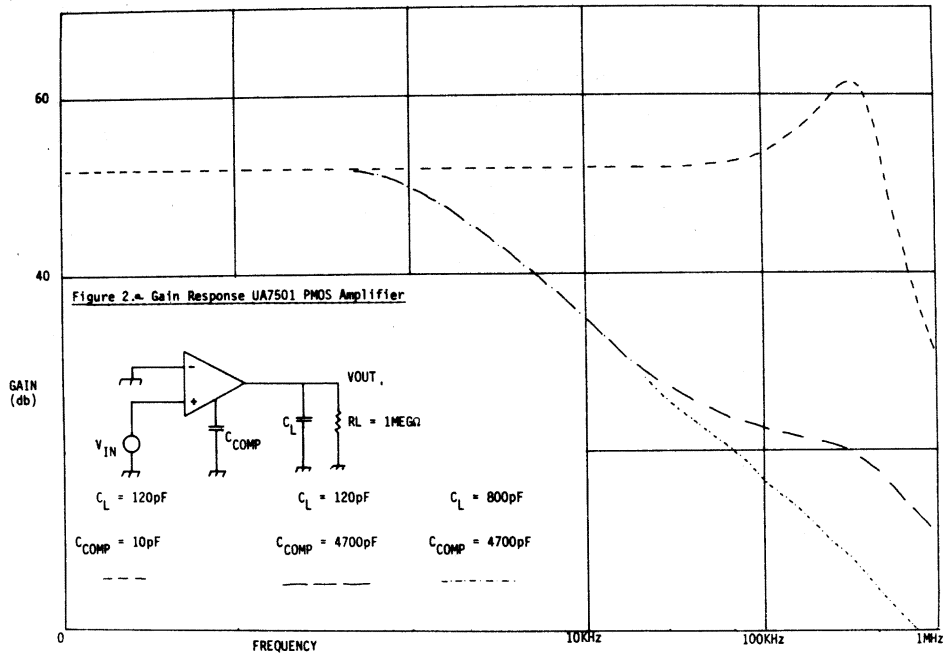


Figure 2.a. Gain Response UA7501 PMOS Amplifier

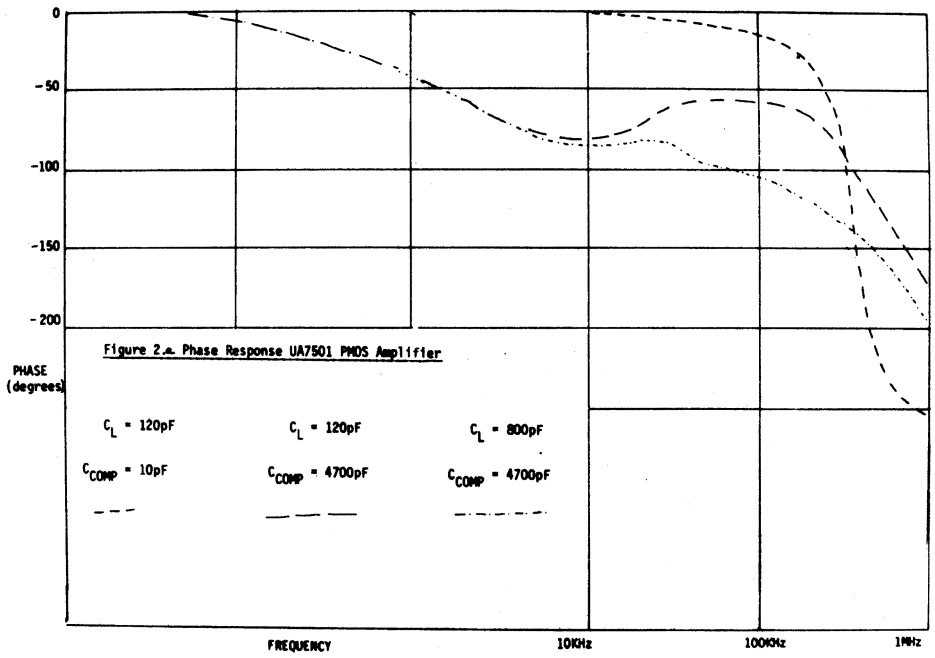


Figure 2.a. Phase Response UA7501 PMOS Amplifier

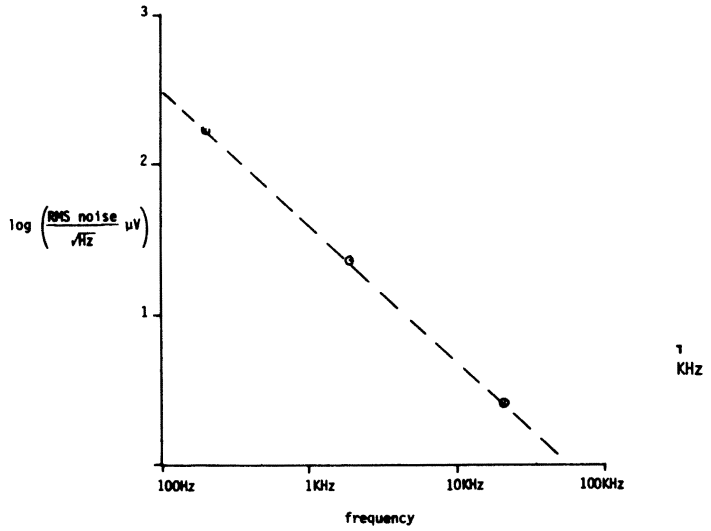


Figure 2(b). Noise Characteristic of PMOS Amplifier

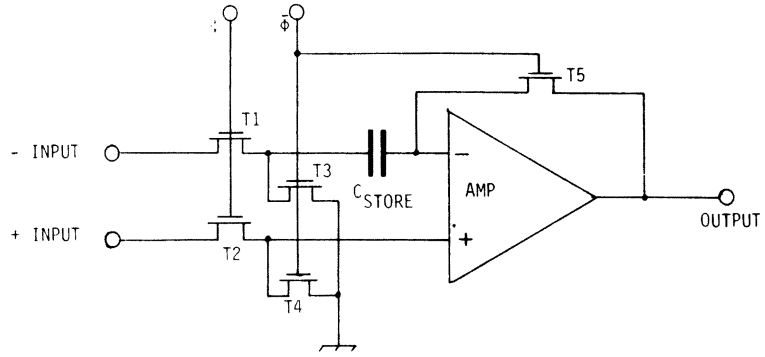


Figure 3(a). Switching Stabilisation Circuit
φ is one phase of the CCD clock.

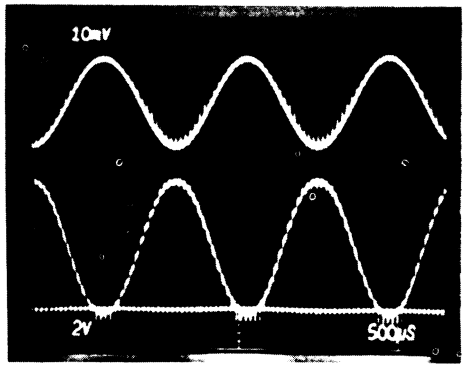
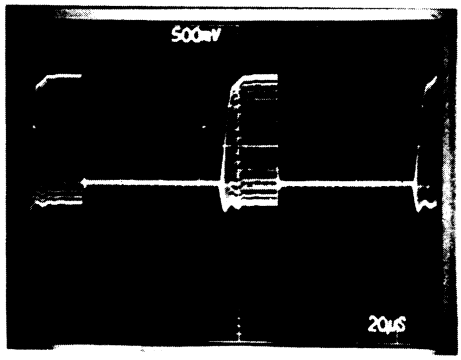


Figure 3(b). Stabilisation Waveforms

Photograph showing input to stabilised amplifier (upper-trace) and output (lower trace).

$\frac{L}{T} = \frac{2}{3}$



Photograph showing detailed portion of stabilisation output waveform $\frac{L}{T} = \frac{1}{3}$

Step response of amplifier may be seen on the leading edge of signal period waveform.

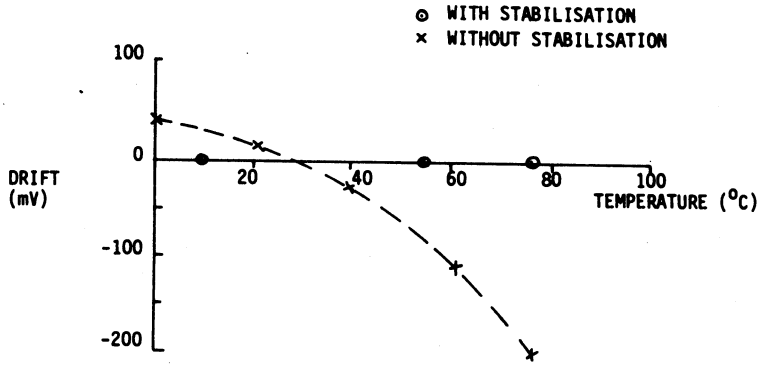


Figure 3(c). Improvement of Drift with Stabilisation

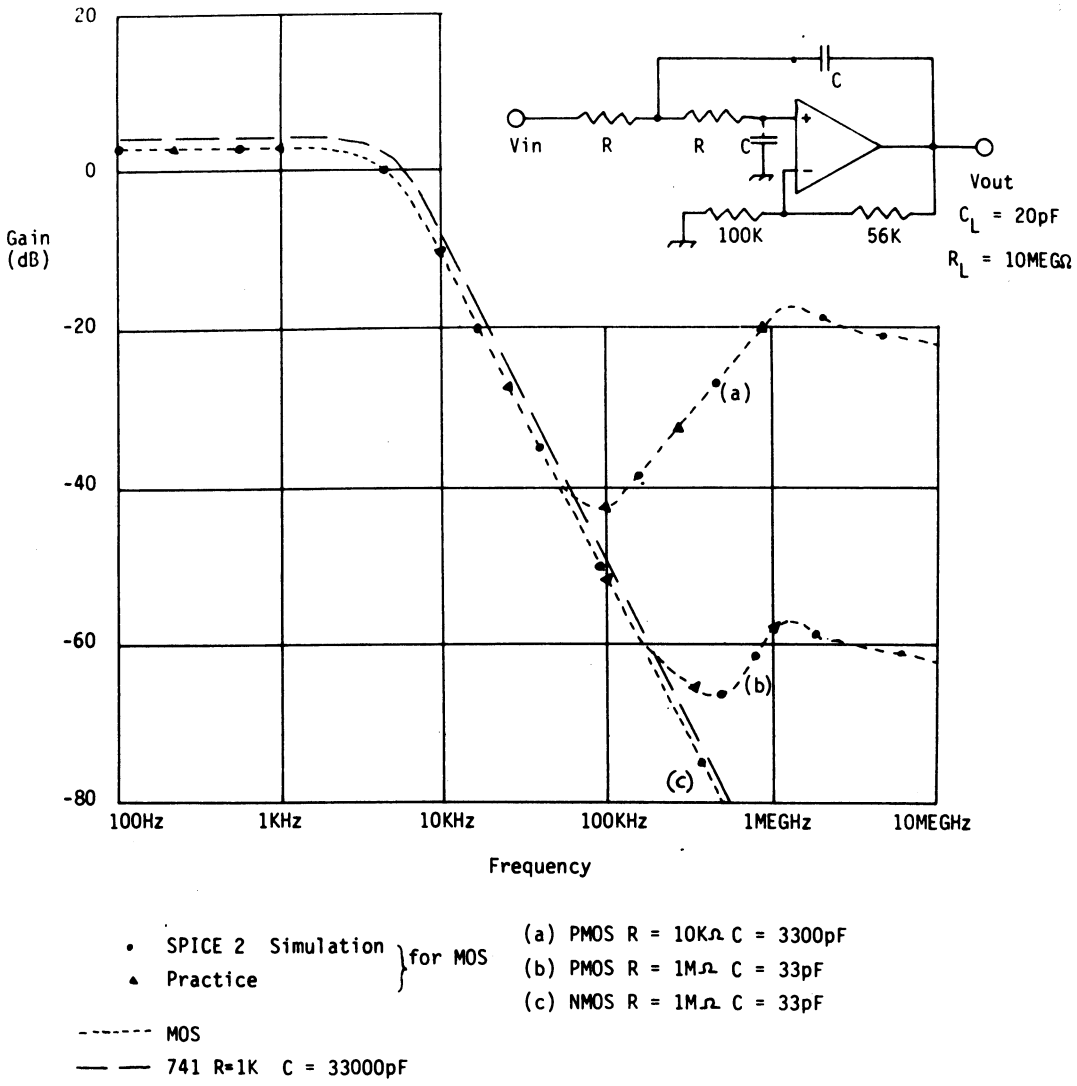
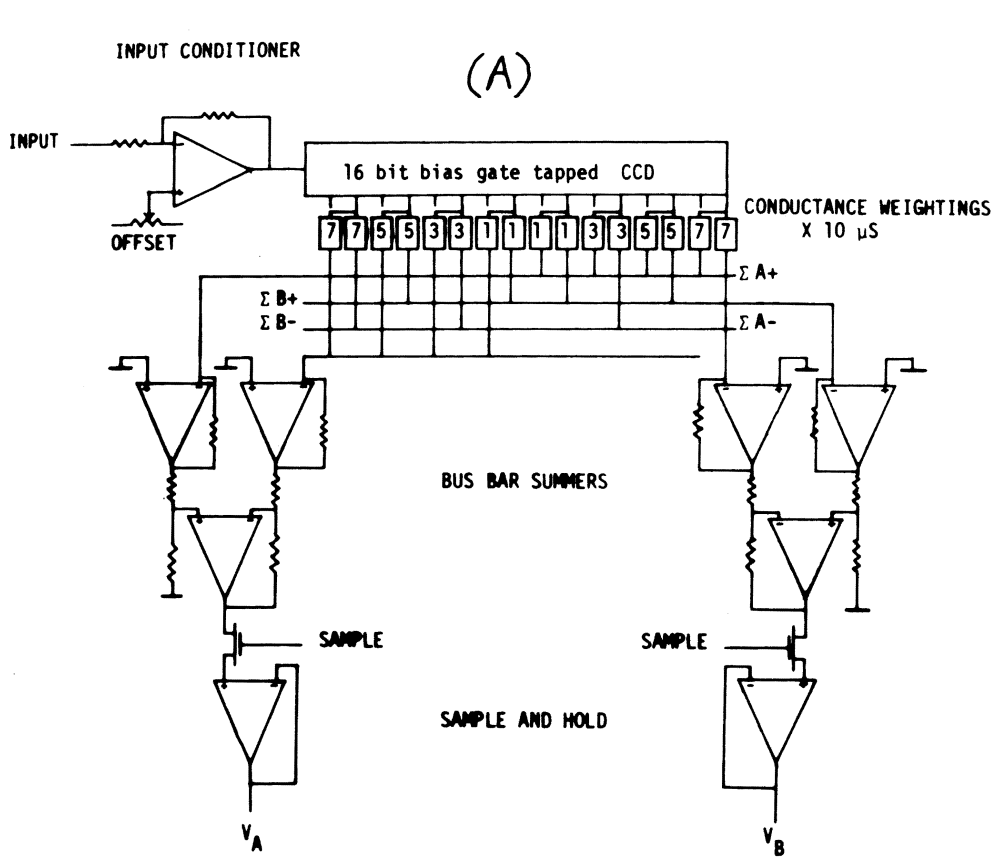
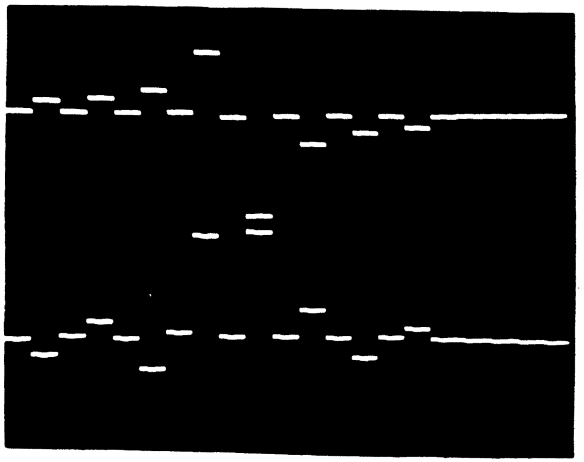
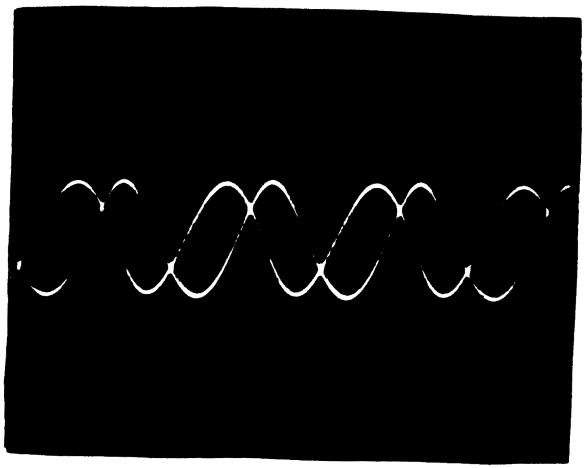


Figure 4. Butterworth Low Pass Filter Results





(B)



(C)

FIG.5. CCD SUB-SYSTEM

(A) TWO QUADRATURE SINEWAVES GENERATED AT V_A AND V_B

(B) IMPULSE RESPONSE OF CIRCUIT (A)

(C) RESULT OF APPLYING SINEWAVE AT INPUT

Scales: 1 V/cm vertical; 50 µs/cm horizontal