A TIME DELAY AND INTEGRATION CCD FOR A SERIAL SCANNED IR IMAGER

G F Vanstone*, J G Harp*, J M Keen*, D V McCaughan* and D B Webb*

ABSTRACT

Commencing with a description of a concept for an IR serial scanned imager we shall outline the function of TDI signal processing. The system requirements impose certain specifications on the TDI processor and we describe the potential advantages of a CCD solution when compared to other techniques.

The reasoning behind the design is outlined, together with details of the design and technology used. A report of the evaluation of N and P surface channels versions of the TDI CCD includes results on harmonic distortion, integration linearity, crosstalk, speed limitations etc.

INTRODUCTION

The function of TDI signal processing is essentially that signals arising from parallel channels are integrated into a common serial signal path by means of a series of differential time delays as shown in figure 1. This technique can be used to coherently integrate the same signal arising from a number of different sensors as in the case of IR or low light imaging (refs 1 and 2) and sonar array processing (ref 3). It can also be used, in place of a tapped delay line, to perform a transversal filtering function (ref 3).

IR SYSTEM CONCEPT

The requirement for a TDI processor stemmed from the need to develop a thermal imager with a display which was not only low in cost but free from fixed pattern noise. The adoption of a television compatible display format satisfied the former requirement. The most satisfactory method of obtaining a uniform display is achieved by utilising a sequential scanning technique. A schematic diagram of such a thermal imaging system is depicted in figure 2.

For sequential scanning the detector elements of a linear array scan one after the other in a serial fashion across the scene. Two axis scanning is employed so each detector scans the entire field of view resulting in wide video bandwidths. Sequentially scanning a linear detector array results in a set of video signals which are similar but staggered in the time domain. To remove this time stagger and linearly sum the resultant signals corresponding to the same resolution element in the scene a time delay and integrate circuit function must be performed. Since the noise contributions of each detector are uncorrelated the total noise is obtained via an r.m.s. summation. The time delay and integration process will therefore afford a maximum improvement of $(n)^{\frac{1}{2}}$ in the signal to noise ratio of the entire array of n detectors over that of an individual detector. Furthermore it is the time delay and integration function that yields the improvement in display uniformity and can

* Royal Signals & Radar Establishment, Malvern, Worcs, UK.

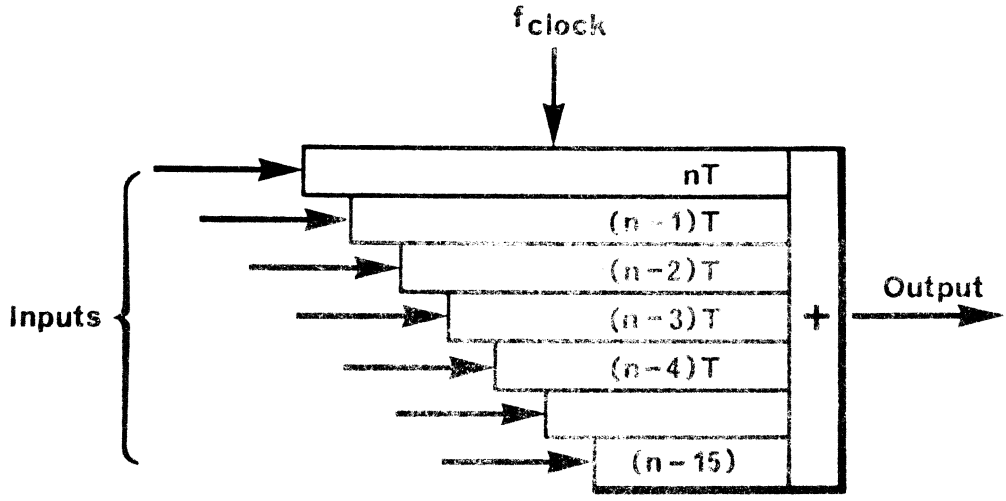


Fig. 1 TDI Concept

result in reduced detector uniformity requirements as well as a high degree of immunity from detector element and/or detector preamplifier failures.

Thermal imaging systems will employ multidetector arrays both to enhance their temperature resolution and to enable the mechanical scanning mechanisms match television line scan efficiencies in scanning the required angular field of view. In the case depicted in figure 2 two serial detector arrays are employed.

Figure 2B illustrates the manner in which the information which is gathered simultaneously from two lines in the infrared scene is serially presented to the television display. With the aid of a delay line the video information from the second infra red scene line is delayed by one television line period and presented for display in the dead time of the mechanical scanner.

The performance required from the circuit undertaking the time delay and integration function within the thermal imaging system is depicted in the table presented in Table 1.

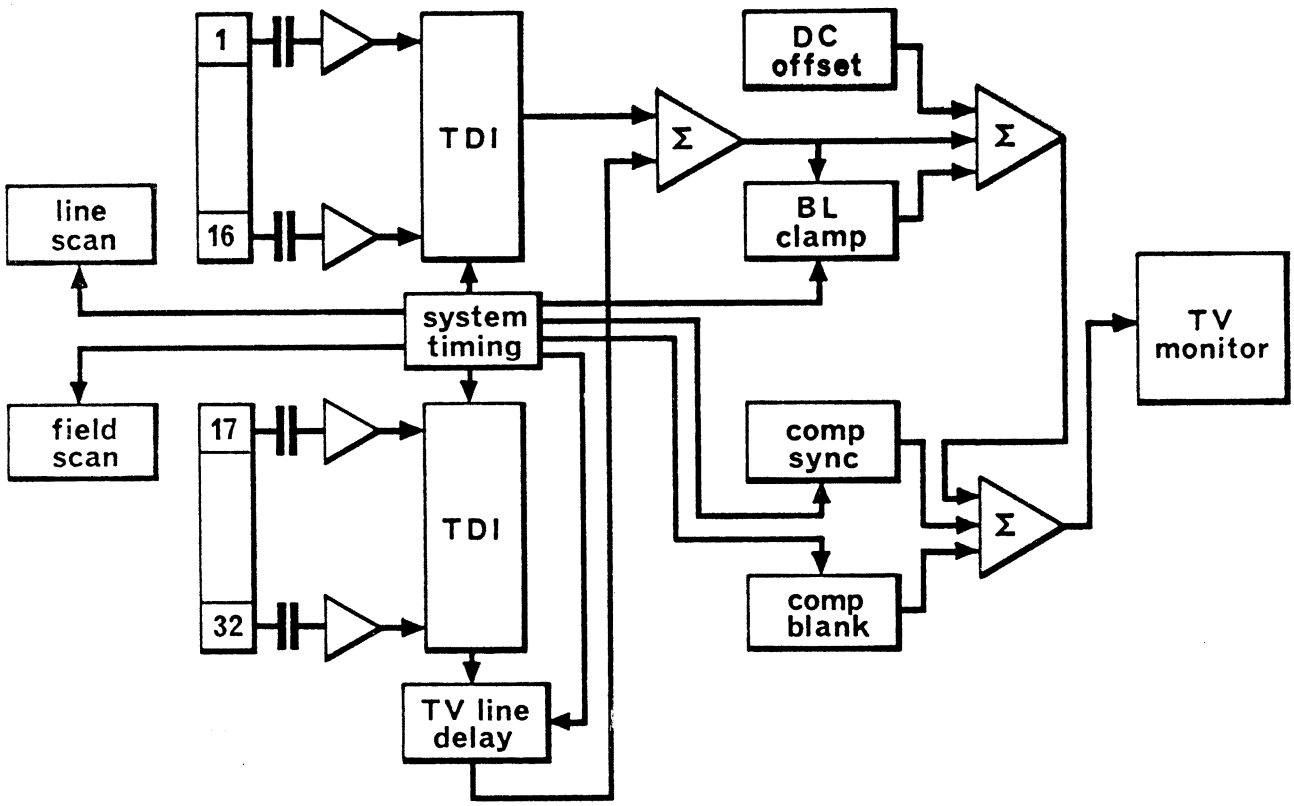
COMPETITIVE TECHNOLOGIES

In implementing the TDI processor two other technologies were considered as competitors to the CCD solution, an approach using digital devices and one based on L-C delay lines.

The digital approach although feasible and based on known technology is large and expensive. Sixteen 8-10 Bit A/D converters are required together with a quantity of shift registers and addition circuitry. It is estimated that such a processor would have a cost and power consumption of 100 times that of the CCD approach and a size factor of 7-8 times larger.

A processor based on L-C delay lines is more competitive. This potentially could be cheaper, smaller and less power consuming than the CCD processor. However unlike shift registers the delays are not exact, they depend on manufacturing tolerances which can give typical errors of $\pm 3 \times 10^{-8}$ s in 10^{-6} s delay and this will lead to an unacceptable signal to noise degradation. In addition L-C processors are designed to operate

(A) System block diagram



(B) Temporal relationship between I/P data O/P data

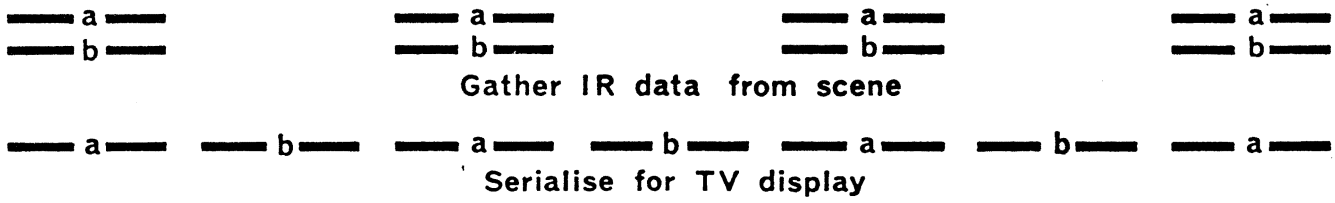


Fig. 2 Sequentially scanned imaging system

PARAMETER	VALUES MIN	TYP	MAX	COMMENTS
Parallel Data Inputs		16		
Package		40 pin DIL		Ceramic
Signal Bandwidth	2.0	2.75		MHZ 313 Line TV format
Dynamic Range	40	60		dB Greater desirable
Maximum input signal amplitude		2.0		Volts peak/peak available from pre-amplifier
Through gain		1.0		Ratio input/output signal
Linearity		1%		
Total harmonic distortion		2%		
Output impedance			1k	Lower desirable, typical load capacitance 10 pf
Minimum acceptable operational temperature range	0		+70°C	
Desirable Operational temperature range	-55°C		+125°C	

TABLE 1 TDI PERFORMANCE REQUIREMENTS

with fixed delays. Changes in the IR mirror scan rate cannot be compensated for. Synchronised processing of this type is however possible with the CCD approach.

CCD DESIGN

The initial choice to be made in designing the TDI device is whether to adopt the multi-delay line approach shown schematically in Fig 1 or to use a multi-input single delay line with the maximum input being restricted to $\frac{1}{n}$ th full well capacity. If we implement the addition within the delay lines rather than at the end, then the former approach can be looked on as a multi-input single delay line but with the electrode size increasing to maintain a constant charge per unit area.

The disadvantage of the 'uniform' electrode structure is that it has a poor input signal to noise ratio because of the restriction on maximum input signal. In addition the low charge per unit area levels can lead to increased charge transfer inefficiencies in the early stages of the TDI processor.

With the 'tapered' structure the major problems are the rapidly increasing chip area as n becomes large (> 20) and also the difficulty of designing an amplifier to cope with the large charge packet. For this particular case with n = 16 it was possible to design a fully tapered structure but for larger devices some compromise between the two extremes would have to be used.

A floating diffusion coupled to an MOS source follower circuit was used at the output. In order to keep the voltage swing on the output node low and to give sufficient drive capability, the output transistor has to be large. An inter-digitated design was used with a channel width/length (Z/L) of 167 and a channel width of 1500 micrometres. The on-chip load transistor had a Z/L of 83 giving a gain of 0.65 for a 16 V power rail. The N-channel version of this amplifier should be capable of driving into a 10 pF load at 14 MHz data rate. A dummy output amplifier was included to permit differential operation to reduce the effect of clock and reset breakthrough. The reset transistor had a gate width of 300 micrometres and a Z/L of 14.

A photomicrograph of the tapered CCD structure together with its output amplifier is shown in Fig 5.

To meet the system linearity requirement it was felt that an input technique based upon surface potential equilibration (ref 4) was needed, this technique is sometimes called 'fill' and 'spill'. A common input diode rail was used with separate input gates to carry the parallel signals. Where the input rails cross the input diode track a grounded screen was interposed between the two levels, the object was to minimize input crosstalk and any pick up from the 'spill' pulses applied to the input diode.

In order to realise the full $\sqrt{n}$ signal to noise improvement the processor has to be limited by the noise presented to the CCD input rather than the CCD noise itself. The theoretically estimated noise levels for the CCD are given in Table 2. These are derived using the equations presented by Carnes and Kosonocky (ref 5). For the specified input voltage swing of 2 V peak-to-peak, the integrated charge packet at the output would be 1.2×10^7 electrons. This would mean that the signal/rms noise should be approximately 80 dB. So that 80 dB would represent the best signal/noise performance of the TDI processor and inputs with a signal/noise > 68 dB would not achieve the full 12 dB processing gain of the integrator.

NOISE SOURCE	NOISE ELECTRONS (rms)
Input noise (single input)	28
Interface state trapping noise	604
Floating Diffusion Reset	1088
MOSFET noise	113
Transfer noise	80
TOTAL (rms)	1257

TABLE 2 CALCULATED CCD NOISE LEVELS

The effect of charge transfer inefficiency can be evaluated by treating the processor as a series of parallel delay lines with addition at the output. It has been shown that (ref 6) using the Z transform notation the output after a single transfer can be represented by $Q_o = Q_i \left(\frac{\alpha}{Z-\varepsilon}\right)$ where the delay time t at one electrode is given by $Z = e^{i\omega t}$.

The charge transfer inefficiency is ε and $\varepsilon = 1-\alpha$ if no charge loss is assumed. For a p phase device with n stages

$$Q_o = Q_i \left(\frac{\alpha}{Z-\varepsilon}\right)^{pn}$$

In the TDI we have a series of parallel delay lines of length n to 1. The impulse response of such device has to be calculated using a staggered input where unit delays are applied to the impulse before entering successive inputs so that synchronous integration occurs within the device.

Then the impulse response of the TDI is given by

$$\frac{Q_o}{Q_i} = \left(\frac{\alpha}{Z-\varepsilon}\right)^{np} + \left[\left(\frac{\alpha}{Z-\varepsilon}\right)^{(n-1)} Z^{-p}\right] .$$

$$+ \left[\left(\frac{\alpha}{Z-\varepsilon}\right)^{(n-2)p} Z^{-2p}\right]$$

$$+ - - - - - - - - - -$$

$$\left[\left(\frac{\alpha}{Z-\varepsilon}\right)^{p} Z^{-(n-1)p}\right]$$

$$\frac{Q_o}{Q_i} = \sum_{k=1}^{n} \left(\frac{\alpha}{Z-\varepsilon}\right)^{kp} Z^{-(n-k)p}$$

The amplitude is given by

$$\left|\frac{Q_o}{Q_i}\right|^2 = \frac{a^{np}\{1 + a^{-np} - 2a^{-np/2} \operatorname{Cos}[np(\theta + \omega t)]\}}{1 + a^{-p} - 2a^{-p/2} \operatorname{Cos}[p(\theta + \omega t)]}$$

where $$a = \frac{\alpha^2}{1 + \varepsilon - 2\varepsilon \cos \theta}$$

$$\theta = \tan^{-1}\left(-\frac{\operatorname{Sin} \omega t}{\operatorname{Cos} \omega t - \varepsilon}\right)$$

Using this relationship it can be calculated that for the 16 stage TDI the drop in MTF at half the clock frequency is 1% and 5% for ε values of 10^{-4} and 10^{-3} respectively. For comparison in a 256 stage device the values are 7% and 50%. The MTF roll-off is less than that experienced by a 256 stage linear delay line because the MTF is normalised to the output signal which is integrated from a series of delay lines ranging from 1 to 256 stages.

From this it can be concluded that transfer inefficiency has less effect in a TDI than a linear line of the same length and in a 16 stage device the MTF degradation should be negligible.

CCD TECHNOLOGY

Devices were made using both P and N surface channel technologies. The gate structure is formed using two levels of polysilicon and one level of aluminium. The gate oxide is etched back between polysilicon deposition steps because no nitride layer is used. Burnt hydrogen oxides including HCl are used for all P-channel masking layers. Dry gate oxides are used and only the layer under the aluminium has a short phosphorus glass step included. P channel starting material is 8-10 ohm-cm and N channel 2-4 ohm-cm, all <100> orientation. Typical Q_{ss} values are 1-1.5 x 10^{11} cm^{-2} and N_{ss} 1-2 x 10^{10} cm^{-2} eV^{-1}. The main differences between the P and N channel processes are in the masking oxides (dry HCl for N-channel), the order of diffusions (diodes before channel stops) and in the etch-back treatment of the gate oxides (changed for N-channel to reduce the total process furnace time).

DEVICE EVALUATION

Measurements were carried out on N and P channel devices using a clock amplitude of 20 V and a clock frequency of 3.3 MHz. The surface potential equilibrium (ref 5) or 'fill and spill' input technique was used throughout.

TRANSFER CHARACTERISTICS

The transfer characteristics shown in fig 3 were obtained by plotting output voltage as a function of the dc input voltage applied to all the gates. Both characteristics show the expected increase in signal at low voltages when the input is operating in a dynamic mode. After the output has reached its peak it then decreases with increasing input in the way expected of a 'fill and spill' input using a single input gate.

The difference between the N and P channel characteristics can partially be explained by the use of a +5 V substrate bias with P channel devices. This was used to ensure that the surface remained depleted even when the clock voltage was returned to zero.

As an initial measurement of the temperature stability of the device the P channel transfer characteristic was also determined whilst the device and its peripherals were placed in an ambient temperature of 82°C. No shifts in the characteristic were seen but the peak value did diminish by approximately 15%.

MAXIMUM OPERATING FREQUENCY

The maximum operating frequency of the P channel device was found to be limited by the time taken to reset the output node to its reference level. This was measured to be 100 ns which restricted the maximum sample rate to approximately 4 MHz.

The corresponding time for the n channel device was < 20 ns indicating that sample rates in excess of 14 MHz should be possible. Limits set by peripherals have so far restricted the evaluation of the device to sample rates up to 10 MHz.

INPUT CROSS-TALK

Two forms of input cross-talk were considered (a) the interference between input signals on different gates (b) the breakthrough of the

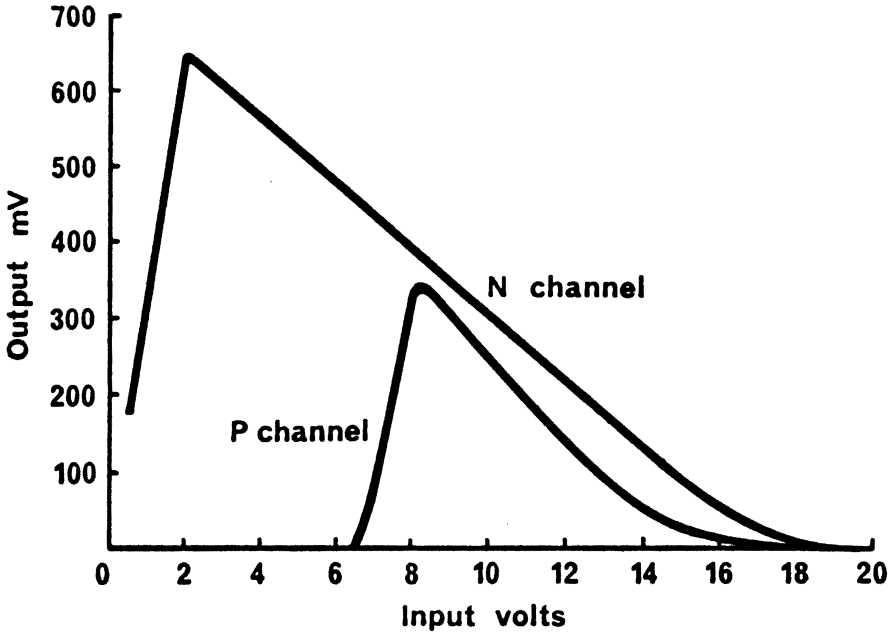


Fig. 3 Transfer characteristics

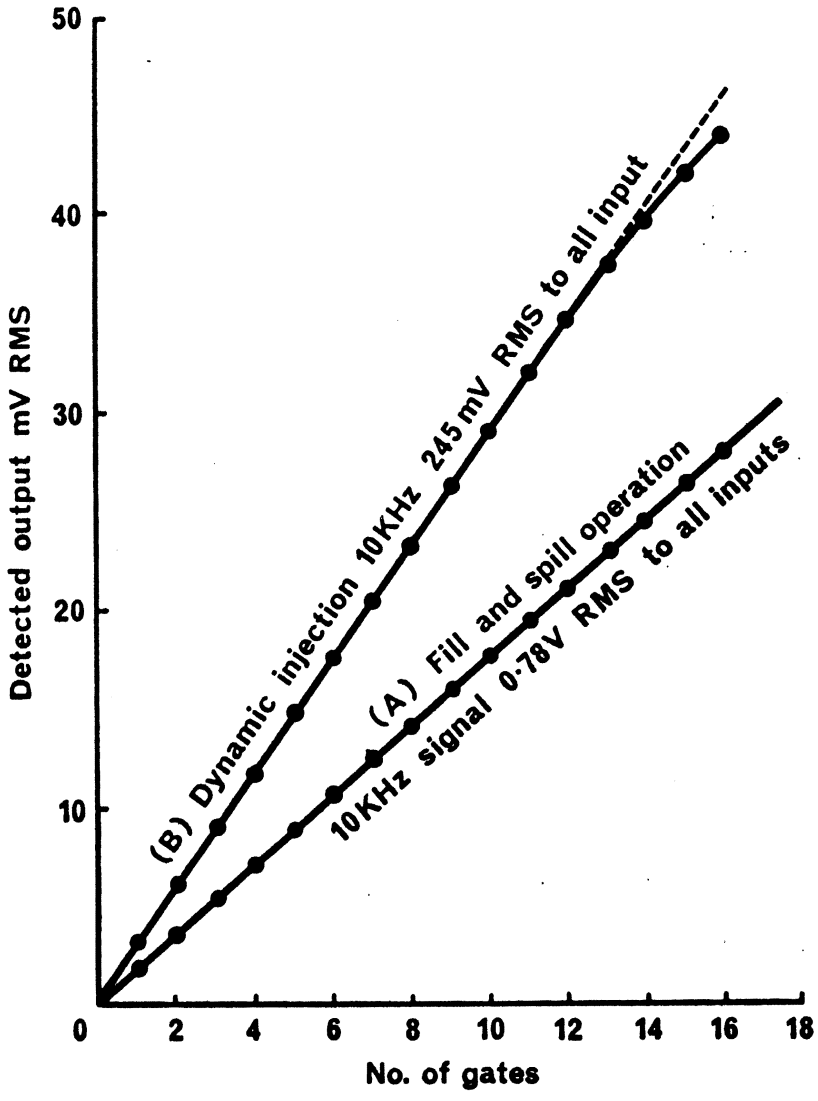


Fig. 4 TDI Linearity

falling edge of the input diode pulse on to the input gate line.

Input signal interference was measured by applying an input of 2 V at 1 KHz on to 15 of the input gates and using a spectrum analyser to determine the amplitude of any cross-talk on to the remaining input gate. Under these conditions the level of cross-talk was 75 dbs down on the input signal.

The breakthrough of the 'fill and spill' pulse was found to be reduced by up to 50% by the operation of the shield gate. However even in this case a 20 V pulse resulted in 100 mV of breakthrough. Care has to be taken to ensure that this breakthrough does not influence the final 'spill' level under the input gate.

SIGNAL LINEARITY

Using a sample rate of 3.3 MHz an input sine wave of 1.5 KHz was applied to all input gates. At the output the amplitude of the fundamental frequency was compared with the second and third harmonics using a spectrum analyser.

For the P channel devices the non-linearity was of the order of 0.1% for a 2 V signal and 1% for a 4 V signal. With signals of up to 12 V into N channel devices the non-linearity remained below 0.01%.

INTEGRATION LINEARITY

To assess the integration linearity of the TDI device, tapped delay lines were used to produce 16 input signals at 10 KHz frequency and with a time stagger of 300 ns between successive inputs. The amplitudes of the input signals were normalised using operational amplifiers. After eliminating the common mode breakthrough by using the on-chip differential amplifier the 10 KHz signal was detected using a wave analyser.

Fig 4 illustrates the way in which the output amplitude increased as the number of input signals being integrated was increased. The straight line characteristic is an indication of the uniformity of the CCD input process along the device and the efficiency of the addition technique.

DYNAMIC RANGE

To measure the dynamic range of the CCD a 1 KHz sine wave was fed to all input gates and its amplitude increased until the second harmonic distortion was 30 db down on the fundamental. The dynamic range was then measured as the difference between the amplitudes of the fundamental and the peak noise level. It was found to be the order of 60 dbs.

Noise generated from outside sources, the measurement instruments, clocks, power supplies etc was found to be dominating the CCD noise. Further work is underway to eliminate these interfering sources so that the true signal/noise of the CCD can be evaluated.

TDI OPERATION

To demonstrate the improved signal to noise of waveforms subjected to TDI processing an input was used consisting of a noise superimposed on a square wave. This signal was fed to all the input gates simultaneously. Fig 6 shows how the signal to noise improves as the number of inputs contributing to the integration increases from 1 to 16.

SUMMARY

The CCD implementation of a TDI processor is likely to be an important device type, useful for a number of applications. We have described its use in a serial scanned IR imaging system. Details of some of the design factors considered have been outlined and these indicate that for a 16 input device it should be possible to achieve a high dynamic range (~ 80 db) with good linearity and high frequency operation (> 10 MHz).

Evaluation of this device confirmed these predictions although limitations in the measurement technique prevented the full dynamic range from being determined. The very good integration linearity indicates that such devices could also be useful alternatives to tapped delay lines for adaptive transversal filters.

ACKNOWLEDGEMENTS

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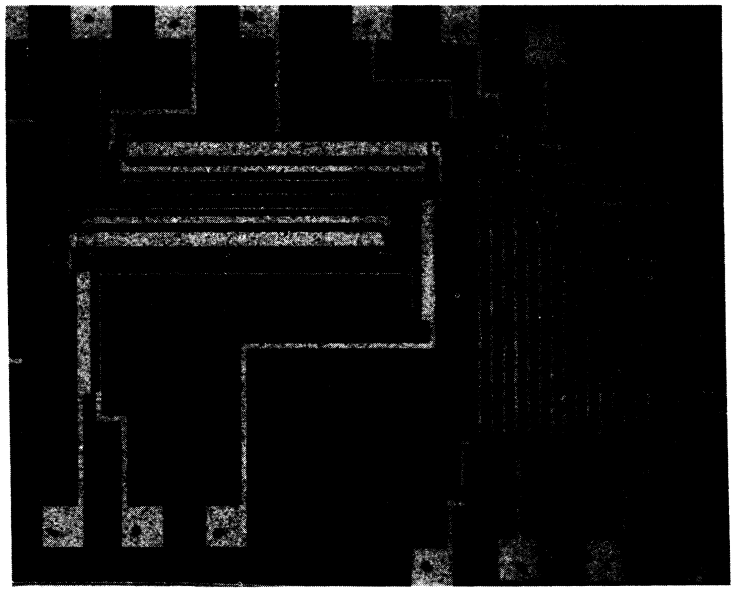

FIG 5. CCD AND OUTPUT AMPLIFIER

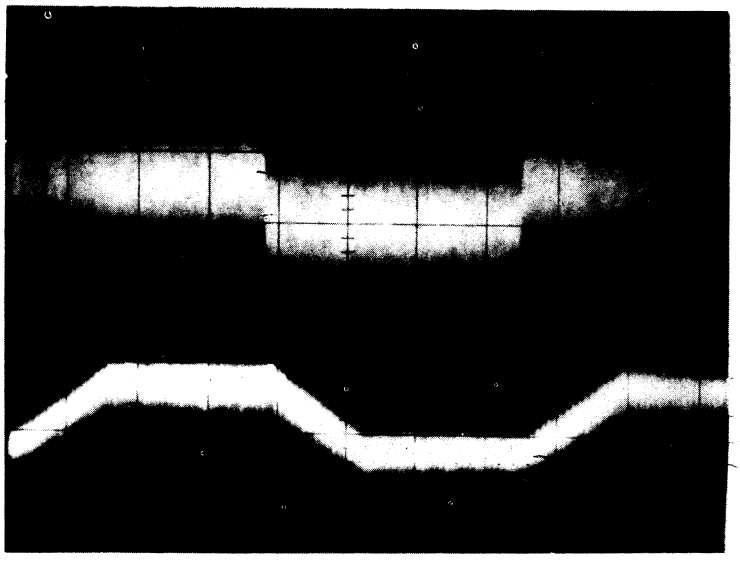

FIG 6. TDI SIGNAL TO NOISE IMPROVEMENT