A CAPACITIVELY-METERED INPUT CIRCUIT FOR LINEAR OPERATION OF CCD's

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ABSTRACT

Investigations of CCD input mechanisms based on the use of the input diode, input gate and ϕ_1 potential well as the source, gate and drain of a MOSFET respectively have led to a new type of charge input mechanism. The charge input level is set by controlling the voltage change across a capacitor. At one extreme the voltage is controlled by a reset limit provided by an external d.c. voltage and at the other extreme it is set by the cut-off of current flow through the effective MOSFET circuit. In turn the latter is controlled in a linear manner by the signal voltage applied to the input gate.

Second and third harmonic distortion levels over 80% of the device dynamic range are as good as or better than those from fill and spill input techniques on the same devices.

INTRODUCTION

A common way of overcoming input circuit non-linearity in CCD's (ref. 1) is to use the "fill and spill" technique (ref. 2). However, residual non-linearities are caused by imperfections of potential profiles in the CCD and the fill and spill technique usually requires large input-signal amplitudes which may be inconvenient.

Here, we suggest an alternative input technique which overcomes the non-linearity by capacitively metering the input signal charge to the CCD so that the voltage to charge transduction is carried out by a constant capacitor.

THE CAPACITIVELY-METERED INPUT TECHNIQUE

The input circuit is illustrated in Fig. 1. The cycle of events is entered after the input diode voltage has been reset to V_o by the diode D_1 when the gating signal on the upper side of the capacitor C was taken to a high positive voltage, Fig. 2.

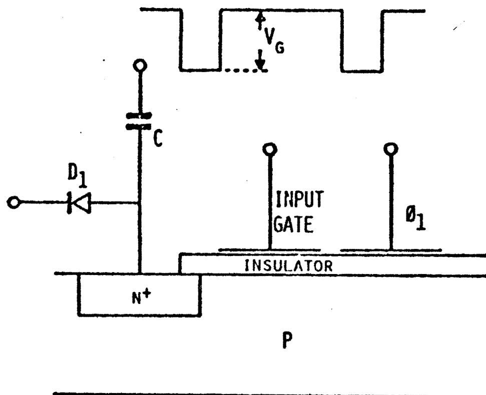

FIG. 1.
A SIMPLE DIAGRAM OF THE CCD INPUT CIRCUITRY

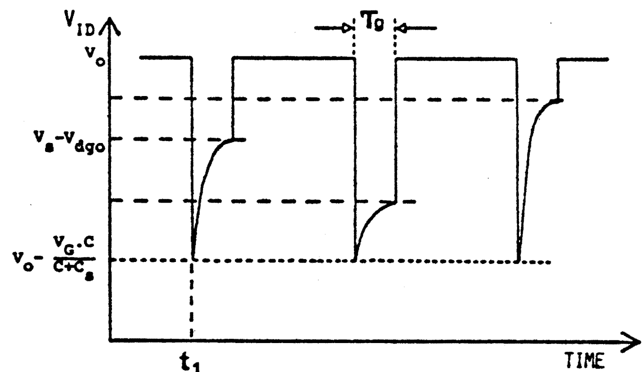

FIG. 2.
VOLTAGE WAVEFORM AT INPUT DIODE FOR THREE DIFFERENT INPUT GATE VOLTAGES (v_s)

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V_s is the input signal voltage and V_{dgo} is the gate/diode threshold voltage. At time t_1 the gating voltage falls so that charge flows from the input diode under the gate and into the CCD. t_1 and the following events must lie within a ϕ_1 clock period. The charge flow originates in the capacitor C so that the input diode voltage rises until the input "FET" ceases to conduct. This cut-off point is determined by V_{dgo} so that the voltage excursion across the capacitor is essentially terminated by V_s. The injected charge is:-

$$q_s = (C + C_s)\left[V_s - V_{dgo} - V_o + \frac{V_G.C}{(C + C_s)}\right] \qquad ...(1)$$

C_s is the stray capacity between the input diode and ground and includes the capacity of D_1 and the input diode.

OPERATIONAL FEATURES
(a) CAPACITIVE NON-LINEARITIES

From eqn. 1 there will be a linear relationship between q_s and V_s providing all terms in the square bracket are either constant or linearly proportional to V_s and providing C_s is a constant or its variation under all conditions is much less than C. In the latter case C is made significantly larger than C_s to avoid the capacitive non-linearities associated with the reverse-biased D_1 and input diode. However, an increase of input diode reverse voltage during the period following t_1 corresponds to a decrease of the reverse bias across D_1 so that their non-linearities can be designed to cancel at the working point (the value of V_s corresponding to zero signal).

V_{dgo} can also cause non-linearity owing to its dependence on $V_s(t)$. Fig. 3 shows a typical relationship (for CD100 devices) between current and voltage at the input diode with input-gate voltage as a parameter. V_{dgo} (defined at an asymptotically low input current of typically 1nA) is found to depend on V_s. The origin of this non-linearity is the voltage across the oxide layer underneath the input-gate. Cut-off conditions are defined by relative potentials in the conducting channel of the FET so that an increase of input diode voltage requires a corresponding increase of (in our case) surface potential at cut-off. In turn a greater gate potential increase is required to provide this change of surface potential owing to the potential change absorbed by

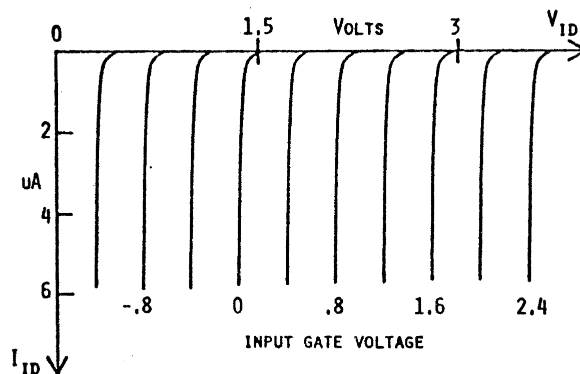


FIG. 3.

RELATIONSHIP BETWEEN INPUT DIODE CURRENT AND INPUT DIODE VOLTAGE FOR VARIOUS VALUES OF INPUT GATE VOLTAGE. VOLTAGES ARE W.R.T. SUBSTRATE.

the oxide. Quantitatively, V_{dgo} contains a constant term V_{dgT} plus a term, ΔV_s, which is dependent on V_s where:-

$$\Delta V_s = V_s \cdot \frac{C_{tot}}{C_{ox}} \qquad ...(2)$$

C_{tot} is the series combination of the oxide capacity, C_{ox}, and the semiconductor depletion layer capacity, C_{dep}. C_{ox} is typically 40×10^{-5} F_1m^{-2} and C_{dep} is typically $\sim 2 \times 10^{-5}$ F_1m^{-2}, so that:-

$$C_{tot} \simeq C_{dep} \simeq \frac{K}{(V_s + V_T)^{\frac{1}{2}}} \qquad ...(3)$$

V_T is a constant caused by fixed interface charge and is typically ~ 4 volts in our n-channel devices. The approximations in eqn. 3 are not necessary to evaluate eqn. 2 but are introduced to indicate the order of non-linearity caused by ΔV_s. Substituting eqns. 2 and 3 into 1:-

$$q_s = (C + C_s) \cdot \left[V_s \left(1 - \frac{C_{tot}}{C_{ox}}\right) - V_{dgT} - V_o \right] + V_G C \qquad ...(4)$$

i.e. $$q_s = (C + C_s) \cdot \left[V_s \left(1 - \frac{K}{(V_s + V_T)^{\frac{1}{2}} \cdot C_{ox}}\right) - V_{dgT} - V_o \right] + V_G C \qquad ...(5)$$

For the numerical values given above the maximum possible non-linearity is less than 5% and will be even smaller owing to the finite dynamic range of V_s. If q_{sat} is the maximum signal charge per cell in the CCD the maximum value of the signal charge in V_s, δV_{smax} is given by:-

$$\delta V_{smax} = \frac{q_{sat}}{(C + C_s)} \qquad ...(6)$$

for $q_{sat} = 1pC$ and $C + C_s = 1pF$ $\delta V_{smax} = 1V$. This peak signal voltage is significantly smaller than that usually required for the fill and spill input technique and is more convenient for many applications.

Typically our measurements of $\left(1 - \frac{K}{(V_s + V_T)^{\frac{1}{2}} C_{ox}}\right)$ from $\frac{\Delta V_{ID}}{\Delta V_s}$ (see Fig. 3) lie in the range 0.90 to 0.95 but the variation for any defined working point is less than 0.01 with $\delta V_{smax} \simeq 1V$ or less. Further assessment of non-linearity will be given later from sine wave distortion measurements.

(b) INEFFICIENCY OF CHARGE TRANSFER IN THE INPUT CIRCUIT

Unfortunately, as is well known to bucket-brigade designers, the charge transfer rate from C through the input circuit of the CCD becomes slower as the cut-off point is approached (ref. 3). If the total charge to be transferred into the CCD during the gating period, τ_g, is q_{so} there is a residual charge, q_{sr}, which is not transferred. We take the simple FET relationship between drain current, i_d, and gate to source voltage,

V_{gs} as (ref. 4):-

$$i_d = \gamma \cdot (V_{gs} - V_T)^2 \qquad \ldots(7)$$

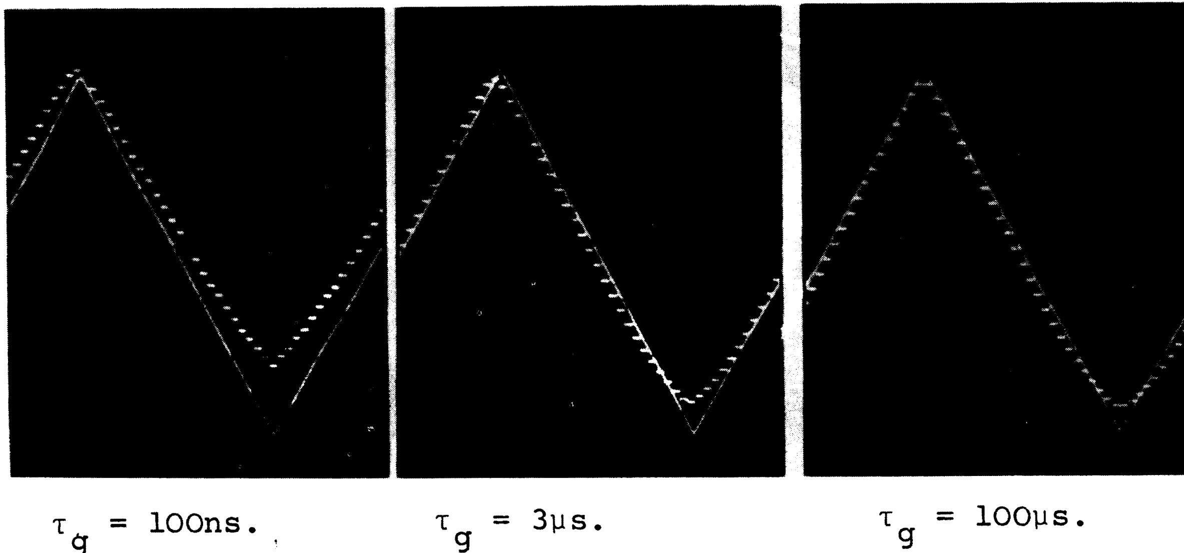
γ is a constant and V_T is the threshold voltage. Using eqn. 7 it can be shown that:-

$$\frac{q_{sr}}{q_{so}} = \frac{1}{1 + \frac{\gamma \cdot q_{so}}{C^2} \cdot \tau_g} \qquad \ldots(8)$$

For the useful practical situation where $q_{sr} << q_{so}$:-

$$q_{sr} \simeq \frac{C^2}{\gamma \tau_g} \qquad \ldots(9)$$

and is independent of q_{so}, so that non-linearity is not introduced.



τ_g = 100ns. τ_g = 3µs. τ_g = 100µs.

Fig. 4. Distortion of a 30 Hz. triangular wave. Clock 3kHz.

In order that q_{sr} is always much less than q_{so} it is essential, as in the use of bucket-brigade devices, to add a fat-zero of about 20% of the saturation charge to all desired signals so that q_{sr} only appears as a simple d.c. offset independent of input signal. When this is not done the results illustrated in Fig. 4 are obtained. Distortion of the triangular wave and its dependence on τ_g at small signal levels can be clearly seen. Even though this residual charge transfer inefficiency is a serious limiting factor for bucket-brigade devices with large numbers of transfer elements it is not particularly troublesome for our single transfer input stage.

(c) EXPERIMENTAL SINE-WAVE DISTORTION MEASUREMENTS

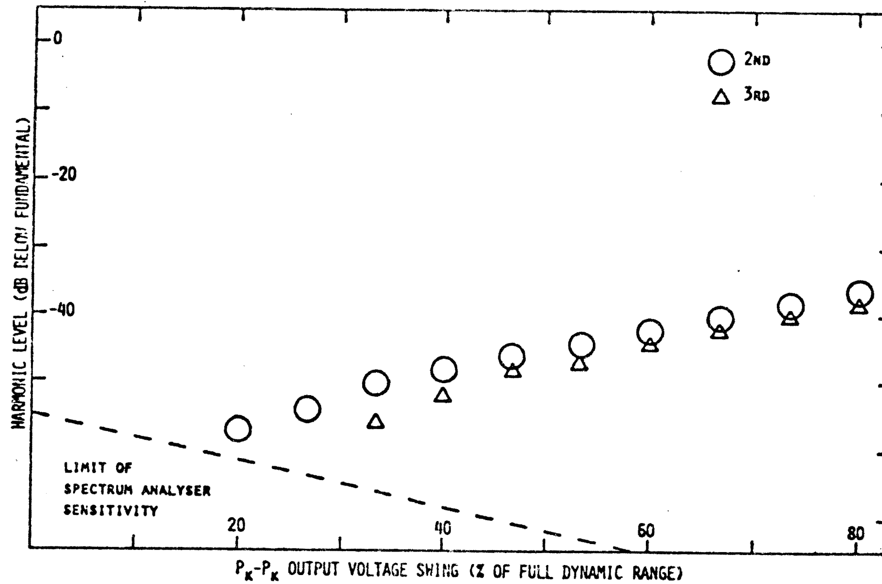


FIG. 5.

Fig. 5 shows the harmonic distortion generated by the passage of a sine-wave through the device as a function of output signal amplitudes. It has a fat-zero of just over half the device dynamic range. Fig. 6 has a fixed signal amplitude of about 14% of the device dynamic range and the d.c. level upon which the signal sits increases in increments of 14% of dynamic range. Fig. 6 shows clearly the effect of residual charge, q_{sr}, on the low level second harmonic component of distortion (see overleaf).

IMPROVED DEVICE DESIGN

Owing to our restricted facilities we have had to conduct experiments with off-chip components. The sources of capacitive non-linearity would be much reduced by combining C with D1 and the input diode in an on-chip realization. Ideally D1 and the input diode would then be realized with their p-type regions diffused into p+ regions and operated at reverse voltages that caused the depletion layer to punch through to the p+ region.

The depletion layer width during the charge-injection period would then be unaffected by potential changes. Similar design of the semiconductor under the input gate would largely remove the residual non-linearity in eqns. 3 and 5.

Another consequence of integration would be the reduction of stray capacity so that the maximum signal voltage excursion described in eqn. 6 could be increased or designed to suit any particular application. The smaller stray capacity and design value of C would require smaller charge transfer with a larger voltage so that non-linearity arising from residual charge in eqn. 9 would be reduced. A fuller use of the dynamic range may then be expected owing to the need for a smaller fat-zero which would probably only be limited by requirements for transfer within the bulk of the CCD.

CONCLUSION

In conclusion we have shown that the turn-off characteristics of the CCD's input FET can be used to control the charge input to a CCD by the feed-back effect of a capacitor. The linearity of this input mode is as

good as conventional "fill and spill" techniques used with the same devices and requires input signals of the order of volts rather than the ten volts or so required by the "fill and spill" method. With fully integrated device design considerable improvements over the results shown here may be expected.

The smaller input-voltage dynamic range required for the capacitively-metered technique appears to provide a further advantage over the fill and spill input technique. We have experienced frequency dependent linearity problems at low frequencies owing to changes of the amount of "fixed" charge at the oxide/semiconductor interface with signal level in the latter technique (ref. 5). No significant similar effects were found for the much lower input-gate-voltage excursions of the capacitively-metered technique.

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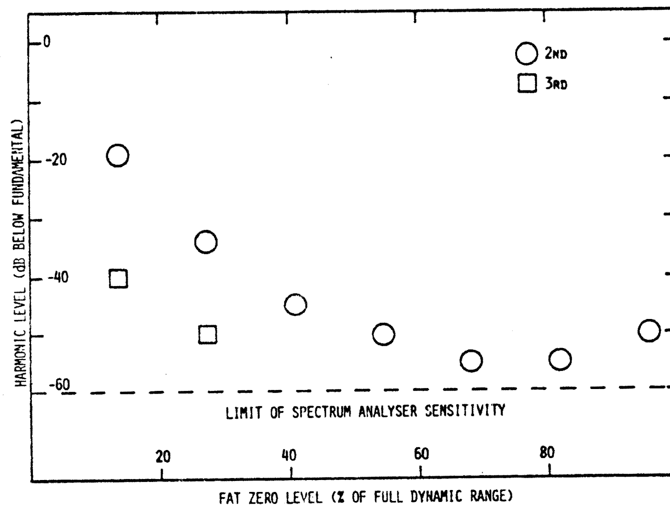

FIG. 6.