# A CCD ANALOG AND DIGITAL CORRELATOR

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## ABSTRACT

The present state-of-the-art in CCD Signal Processing falls short of the requirements for simultaneous high throughput and high accuracy in a single, relatively inexpensive component. Such a component could increase the performance and efficiency of some radar, sonar, communication, frequency domain beamforming and image transform tasks requiring linear filtering, convolution, cross-correlation or Fourier Transform calculations. Recent work has shown that whenever analog accuracy is acceptable, the analog CCD transversal filter or correlator can be used as a modular building block for the implementation of these computations with high intrinsic speed, a high degree of parallelism and minimal control overhead. The algorithm used for the computation is that of the Chirp-Z Transform (CZT) which is ideally suited to CCD implementation. To maintain both the speed and accuracy, the most desirable and straightforward approach is to use the concept of parallelism and simplicity of control of the CZT and modify the analog transversal filter used in the temporal transform to obtain a digital equivalent.

The discussion of the capabilities and limitations of present system implementations will naturally introduce a new device architecture whose desired properties reduce present constraints. The design of an integrated, high speed, highly parallel "digital" cross-correlator where the charge coupling concept is also used to implement the multipliers will be described. The analysis of experimental data on the multiplier has validated the high accuracy squaring required for the multiplier. The mathematical algorithms used in this work will be presented and will show how digital accuracy can be achieved in an analog sampling device. A CCD correlator with a code storage capability of 32 samples will be discussed for a technological assessment of this new approach to high speed, high accuracy signal processors.

## INTRODUCTION

Recent work has shown how a large portion of the computational task for many signal processing problems can be implemented via crossconvolution or crosscorrelation. [1] Tasks requiring matched filtering, passive localization, and signal preemphasis may be performed directly as a crosscorrelation or crossconvolution. Other linear transforms required for spectral analysis, data compression, and beamforming may be reduced to crosscorrelation or crossconvolutions via algorithms such as the chirp-z transform and the prime transform. Whenever analog accuracy is acceptable, the analog CCD transversal filter or correlator can be used as a modular building block capable of performing many demanding signal processing computations with a high degree of parallelism and minimal control overhead.

In order to be able to address as wide a class of signal processing problems as possible, it is desirable to have a processing structure in which increased accuracy may be obtained by simply combining identical modules. The module which will be described in this paper is an analog CCD correlator with digital input and output. The correlator architecture is selected for its high degree of parallel computation and simple serial data flow. Provision of digital input and output permits modules to be combined for increased accuracy using residue or radix arithmetic.

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## ANALOG CORRELATOR

The basic block diagram of an analog crosscorrelator is shown schematically in Figure 1. In this diagram the convolution/correlation of two discrete signals s and r is expressed as

$$(s * r)(n) = \sum_{n=0}^{N-1} s_n r_{m-n} \quad \text{(convolution)} \tag{1}$$

is seen as the formation of the sum of products of the shifted sequence $s_n$ with the reversal of the sequence $r_n$. For compact, low power implementation of this programmable transversal filter or crosscorrelator structure, the action of two CCD delay lines shifting and storing the signal [s(n)] and reference [r(n)] samples is combined with the non-destructive sensing and tapping circuitry which feeds into an analog multiplier. Figure 2 illustrates the techniques

1. for injecting charges proportional to the voltage sequences s(n) and r(n),
2. for non-destructively sensing and tapping each sample s(n) and r(n),
3. for forming the summation s(n) + r(n),
4. and finally for squaring s(n), r(n), and [s(n) + r(n)] in simple, floating gate amplifiers. These MOSFET amplifiers operating in the saturation region have outputs proportional to $s^2$ (n), $r^2$ (n), and $[s(n) + r(n)]^2$ which are then fed into a differential amplifier (D.A.) to produce s(n)r(n) from the identity.

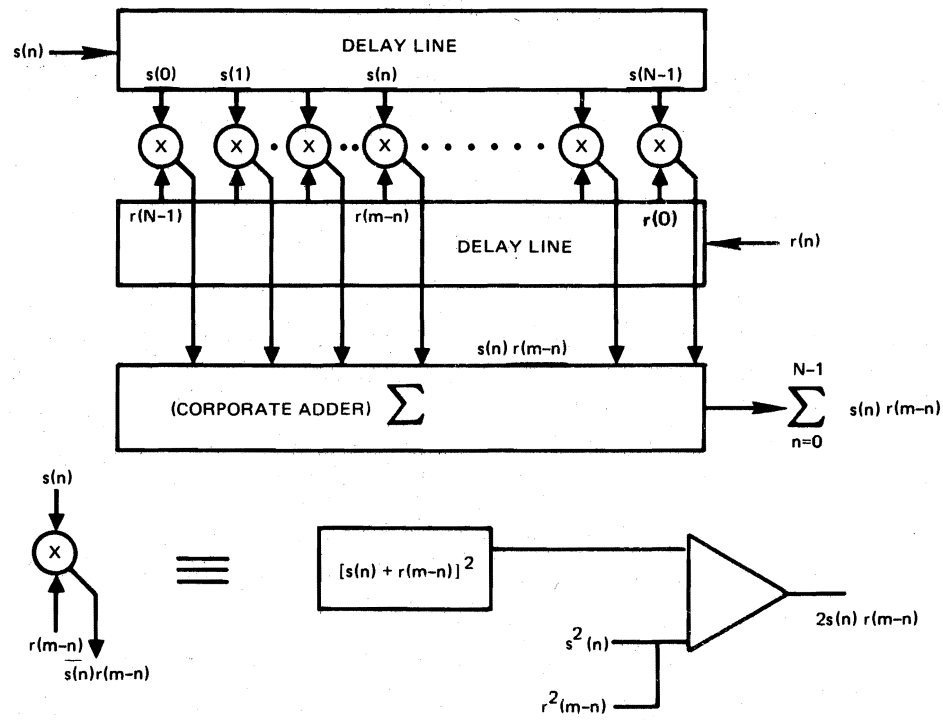
$$s(n)r(n) = \frac{1}{2}\left\{[s(n) + r(n)]^2 - [s(n)^2 + r(n)^2]\right\} \tag{2}$$

The performance of the basic operations 1, 2, 3, and 4 above is the basis for real-time convolution of signals. The functions 3 and 4 are performed in what is labelled "multiplier" in the block diagram of Figure 1. A one-quadrant multiplier (i.e., both s(n) and r(n) are positive quantities) or a one-cell crossconvolver is shown in the photomicrograph of Figure 3. A 32-sample programmable filter would simply consist of 32 serial juxtapositions of such cells. Additional circuitry could also be included, such as adders to sum the outputs of several taps (i.e., squaring devices) in order to reduce the pin count and allow the use of available packages. The circuit implementation of Eq (2) destroys the inherent simplicity and flexibility of the concept since the requirement for the provision "on-chip" of $s(n)^2$ and $r(n)^2$ at each tap is satisfied only if two identical tapped delay lines are added – one for each signal s(n) and r(n).

To alleviate this "layout" difficulty, the alternative mathematical identity

$$s(n)r(n) = \frac{1}{4}\left\{[s(n) + r(n)]^2 - [s(n) - r(n)]^2\right\} \tag{3}$$

is considered. A change of sign for r(n) is, however, present in the second squared term. The capability for handling positive and negative values for s(n) and r(n) is an important aspect to the design of a multipurpose analog correlator regardless of whether Eq (2) or (3) is implemented. The building block in Figure 4 represents the implementation of Eq (3) for this purpose while Figure 2 illustrates the hardware implementation of Eq (2).




A. ANALOG CONVOLVER/PROGRAMMABLE FILTER

B. MULTIPLIER OPERATION PERFORMED BY A SQUARING DEVICE AND A DIFFERENTIAL AMPLIFIER

Figure 1.

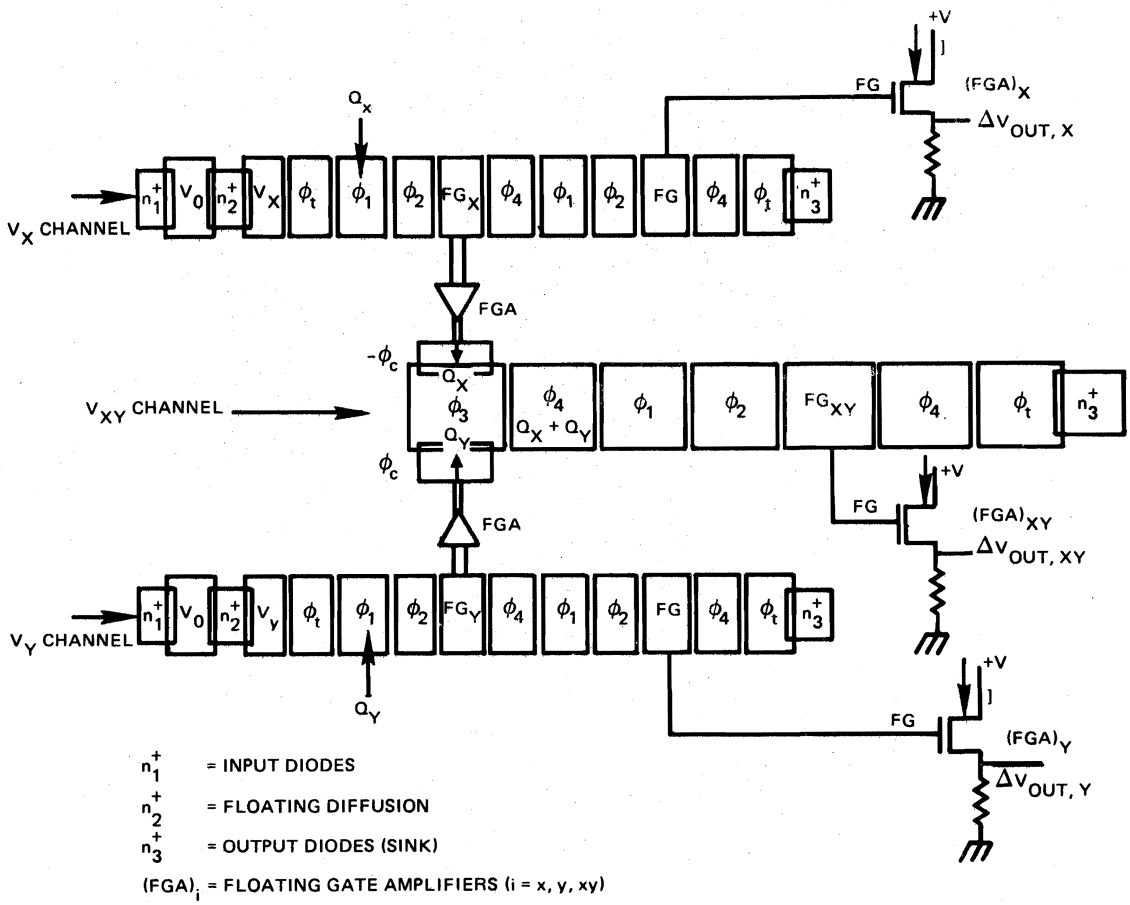



Figure 2.

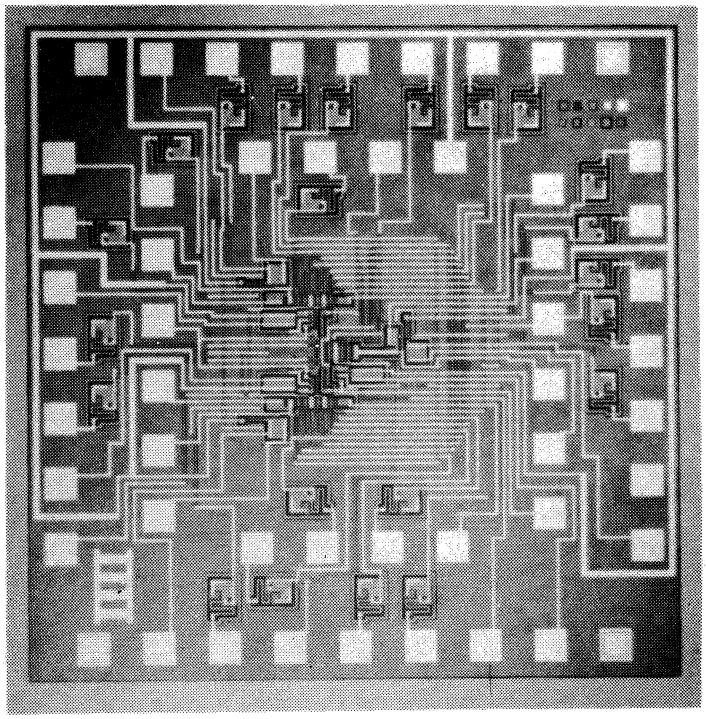


Figure 3. Photomicrograph of One-Quadrant Multiplier, or One-Sample Cross-Convolver/Correlator

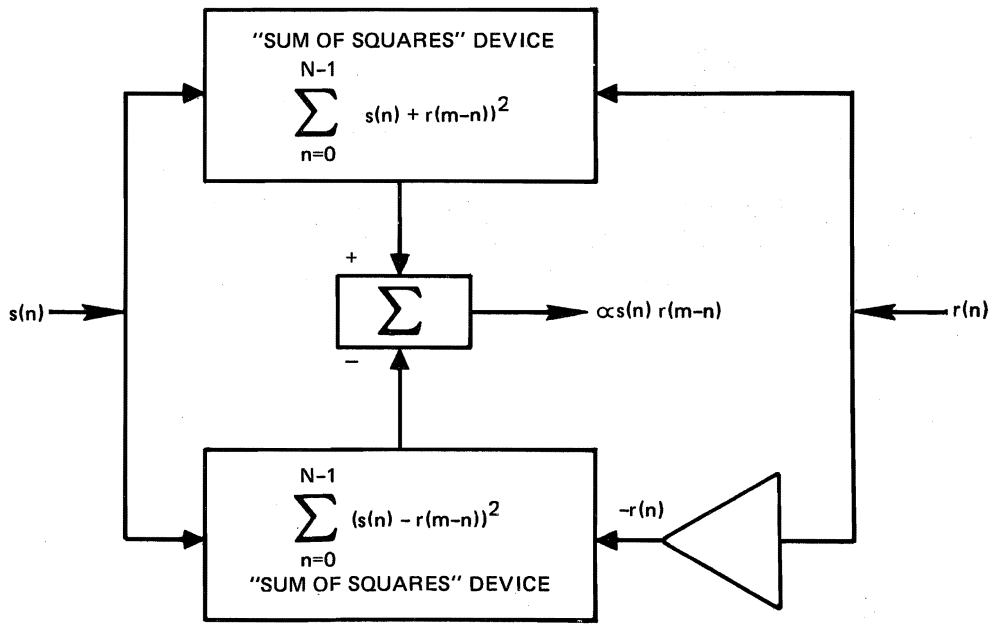



Figure 4. Analog Convolver Using Quarter Square Multiplier Identity

$$sr = \frac{1}{4}\left[(s+r)^2 - (s-r)^2\right]$$

In the present application of CCD's to correlator design, the voltage sequences s(n) and r(n) are transformed into charge sequences $q_s(n)$ and $q_r(n)$, which are non-negative quantities. In order to be able to multiply both positive and negative quantities, a modified quarter-square identity is used, in which the signals are decomposed into their positive and negative parts

$$s = s^+ - s^- \tag{4}$$

$$r = r^+ - r^- \tag{5}$$

where

$$s^+ = \begin{cases} s, & s \geqslant 0 \\ 0, & s < 0 \end{cases}$$

$$s^- = \begin{cases} 0, & s \geqslant 0 \\ -s, & s < 0 \end{cases}$$

The positive and negative parts of r are defined similarly. The decomposition may be used to verify the identity of Eq (6), by expanding the right hand side:

$$s(n)\, r(m-n) = \frac{1}{2}\left\{[s^+(n) + r^+(m-n)]^2 + [s^-(n) + r^-(m-n)]^2\right\}$$

$$-\frac{1}{2}\left\{[s^+(n) + r^-(m-n)]^2 + [s^-(n) + r^+(m-n)]^2\right\} \tag{6}$$

The convolution product of Eq (1), written as

$$\sum_{n=0}^{N-1} s(n)r(m-n) = \frac{1}{2}\left\{\sum_{n=0}^{N-1} [s^+(n) + r^+(m-n)]^2 + \sum_{n=0}^{N-1} [s^-(n) + r^-(m-n)]^2\right\}$$

$$-\frac{1}{2}\left\{\sum_{n=0}^{N-1} [s^+(n) + r^-(m-n)]^2 + \sum_{n=0}^{N-1} [s^-(n) + r^+(m-n)]^2\right\} \tag{7}$$

is thus implemented by a 4-quadrant analog correlator/transversal filter module consisting of four identical "sum-of-square" devices (each one calculating one of the sums in the right hand side of Eq (7)) and a single differential amplifier (D.A.) as shown in Figure 5.

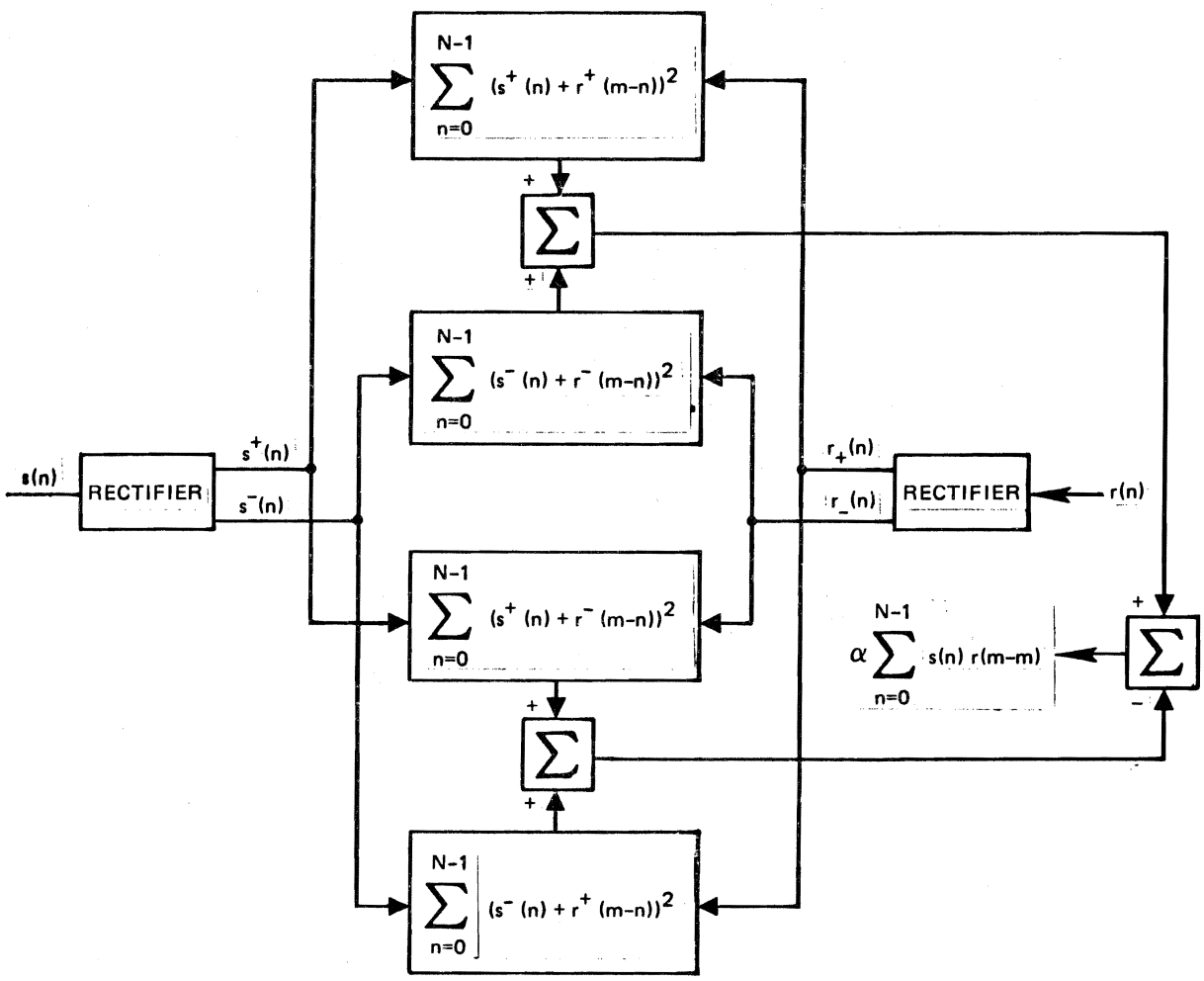



Figure 5. Four – Quadrant Analog Convolver/Transversal Filter Module Using Four "Sum-of-Square" Devices Based on Radix Arithmetic

## HYBRID ANALOG/DIGITAL CONVOLUTION

An analog convolver may be turned into a digital convolver by adding digital to analog converters to the inputs, adding analog to digital converters to the multiplier outputs, and replacing the analog summer by a digital summer as shown in Figure 6. Alternatively, several of the product terms may be summed in analog form prior to A/D conversion and digital summation in order to reduce the required number of A/D converters and digital adders. In either case it is essential that the range of input integers not be too large in order to prevent the (approximate) analog operations from giving the wrong answer when converted to digital form; i.e., the analog error allowable is less than half of the amplitude resolution of the A/D converters. It is difficult to perform analog operations with an accuracy much better than 1%. This will place a limit on the number of levels into which the sum of products may be correctly quantized. If it is desired to perform a long convolution with large dynamic range, it will be necessary to combine several such modules. Several methods for combining low dynamic range digital correlator or convolver modules to perform a computation with greater dynamic range will be discussed.

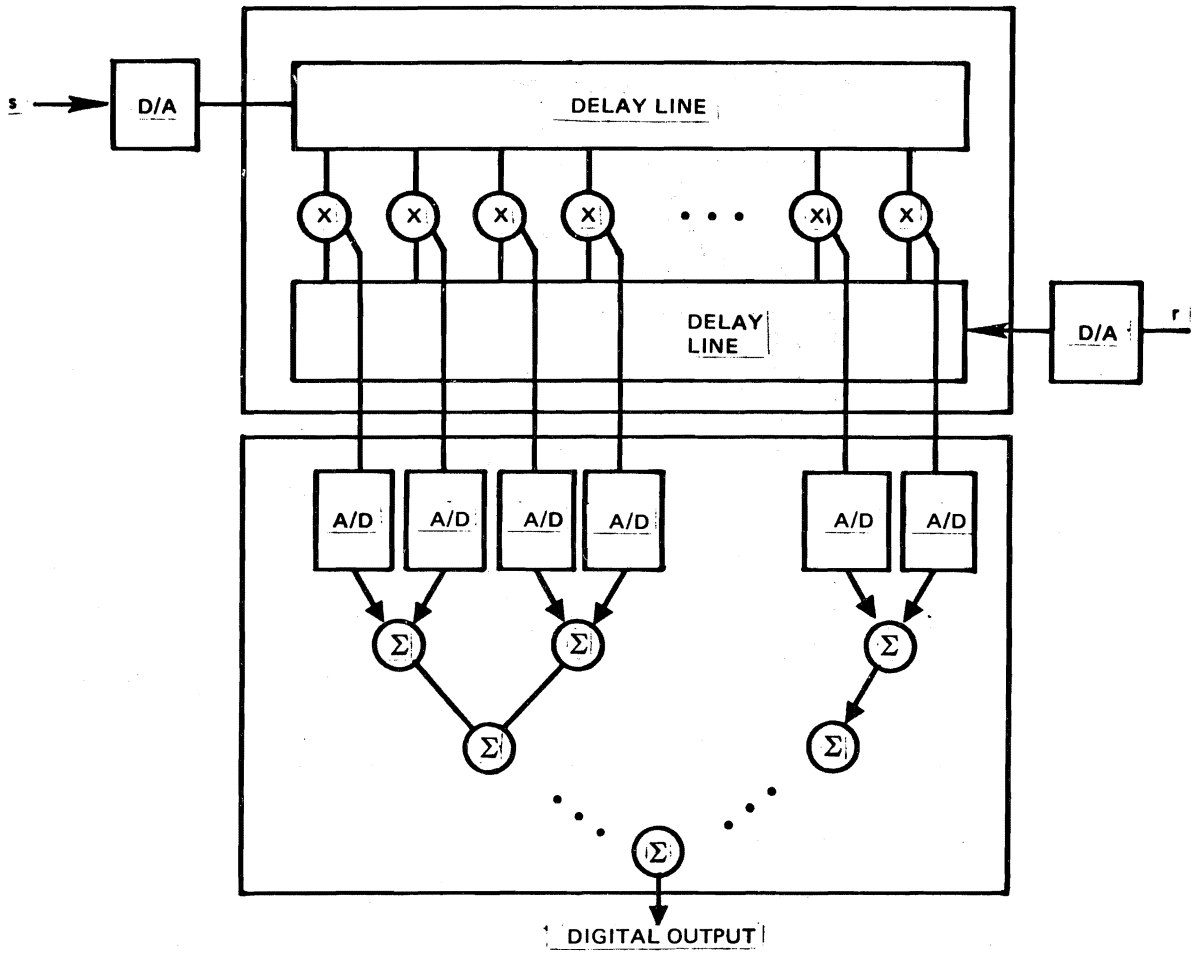



Figure 6. Concept for Digital Correlator Using Analog Multiplication

## DIGITAL CORRELATION USING RADIX ARITHMETIC

We first consider the convolution of two non-negative sequences of integers s(n) and r(n) where the first sequence has a radix $R_1$ representation and the second sequence has a radix $R_2$ representation. The number of digits used in the two representations are $D_1$ and $D_2$, respectively. The radix would be 2 for binary arithmetic, 10 for decimal, etc.

$$s(n) = \sum_{u=0}^{D_1-1} s_u(n)\, R_1^u \tag{8}$$

$$r(n) = \sum_{t=0}^{D_2-1} r_t(n)\, R_2^t \tag{9}$$

Note that the digits in the first sequence range from 0 to $R_1-1$, and the numbers represented range from 0 to $R_1^{D_1}-1$. Similarly, in the second sequence, the digits range from 0 to $R_2-1$, and the numbers represented range from 0 to $R_2^{D_2}-1$. The convolution sum is shown in Eq (10) in terms of the radix representations.

$$\sum_{n=0}^{N-1} s(n)\, r\,(m-n) = \sum_{u=0}^{D_1-1} \sum_{t=0}^{D_2-1} \sum_{n=0}^{N-1} s_u(n)\, r_t(n-m)\; R_1^u\; R_2^t \tag{10}$$

The left hand side of the above equation represents the desired crossconvolution. The right hand side may be implemented using $D_1\ D_2$ crossconvolvers of length N, each of which convolves an $R_1$-level sequence with an $R_2$ level sequence. The most useful cases are when $R_1$ is a power of $R_2$ or when either $D_1$ or $D_2$ is one. In either of these cases the final weighted summation may be performed by using only positional shifts and adds.

In order to accept signals which have negative as well as positive samples, the signals may be first decomposed into positive and negative parts, as in Eq (4) and (5), and then the positive and negative parts may be represented in radix notation, as in Eq (8) and (9).

$$s^+(n) = \sum_{u=0}^{D_1-1} s_u^+(n)\; R_1^u \tag{11}$$

$$s^-(n) = \sum_{u=0}^{D_1-1} s_u^-(n)\; R_1^u \tag{12}$$

$$\begin{aligned} s(n)\, r(m) &= [s^+(n) - s^-(n)]\; [r^+(m) - r^-(m)] \\ &= [s^+(n)\, r^+(m) + s^-(n)\, r^-(m)] - [s^+(n)\, r^-(m) + s^-(n)\, r^-(m)] \end{aligned} \tag{13}$$

Eq (13) represents a general four-quadrant multiplication in terms of one-quadrant (non-negative only) multipliers and elementary operation. It is easily extended to a convolution as shown in Eq (14). Eq (14) shows how to perform a convolution of two arbitrary sequences using convolvers which accept only non-negative inputs.

$$\begin{aligned} \sum_{n=0}^{N-1} s(n)\, r(m-n) = &\left[\sum_{n=0}^{N-1} s^+(n)\, r^+(m-n) + \sum_{n=0}^{N-1} s^-(n)\, r^-(m-n)\right] \\ &- \left[\sum_{n=0}^{N-1} s^+(n)\, r^-(m-n) + \sum_{n=0}^{N-1} s^-(n)\, r^+(m-n)\right] \end{aligned} \tag{14}$$

If the radix representations of the positive and negative parts of the two signals are substituted into Eq (14), then we obtain a method for performing crossconvolution of signed signals with high dynamic range, using convolvers which accept only non-negative signals of low dynamic range as shown in Eq (15).

$$\begin{aligned} \sum_{n=0}^{N-1} s(n)\, r(m-n) = \sum_{u=0}^{D_1-1} \sum_{t=0}^{D_2-1} \Bigg\{ &\left[\sum_{n=0}^{N-1} s_u^+(n)\, r_t^+(m-n) + \sum_{n=0}^{N-1} s_u^-(n)\, r_t^-(m-n)\right] \\ &- \left[\sum_{n=0}^{N-1} s_u^+(n)\, r_t^-(m-n) + \sum_{n=0}^{N-1} s_u^-(n)\, r_t^+(m-n)\right] \Bigg\} R_1^u\; R_2^t \end{aligned} \tag{15}$$

In order to reduce the required number of correlator modules, the terms in Eq (15) may be combined as shown in Eq (16)

$$\sum_{n=0}^{N-1} s(n)\, r(m-n) = \sum_{u=0}^{D_1-1} \sum_{t=0}^{D_2-1} \left\{ \sum_{n=0}^{N-1} [s_u^+(n) - s_u^-(n)]\, [r_t^+(m-n) - r_t^-(m-n)] \right\} R_1^u\, R_2^t \quad (16)$$

Eq (16) requires $D_1\, D_2$ correlators accepting signed inputs, such as the correlator shown in Figure 5.

## DIGITAL CORRELATION USING RESIDUE CLASS ARITHMETIC

Let M be a positive integer and x be an integer. Then x can always be represented in terms of its quotient and least positive remainder upon division by M, as shown in Eq (17).

$$x = q\,M + r,\ 0 \leqslant r \leqslant M - 1 \quad (17)$$

All of the integers x, x ± M, x ± 2M, x ± 3M, . . . have the same least positive remainder, and are said to belong to the same residue class modulo M. There are exactly M distinct residue classes modulo M; the residue classes of 0, 1, . . . M – 1. In the arithmetic of residue classes modulo M, we essentially perform ordinary addition and multiplication but pay attention only to the residue class to which the result belongs, i.e., ignore multiples of M. Residue arithmetic was studied extensively by Gauss. [2] It also has been examined for use in general purpose digital computers because it offers the possibility of relatively simple adders and multipliers, since no carry terms are needed when performing those operations in a multiple residue representation. [3, 4] In such general applications, however, overflow detection and division present formidable difficulties, and hence it has not been extensively used in practice. Cheny [5] pointed out that correlation requires only multiplications and additions – operations which are easily performed with residue arithmetic. His correlator, however, used only a single multiplier and adder, and hence was relatively slow.

In ordinary binary addition and subtraction, if the answer is scaled down so as to avoid overflow, then we are faced with roundoff or truncation errors. Residue arithmetic has no truncation errors. If residue arithmetic is substituted for ordinary arithmetic, we get either the exact answer or we are off by a multiple of M; i.e., we can only make overflow errors. If these overflows are avoided or corrected, the computation is exact.

If $M = M_1\, M_2 \ldots M_T$ where no two of $M_i$'s have a common divisor greater than 1, then the least non-negative residue of x modulo M is uniquely determined by the least non-negative residues modulo $M_1$, $M_2$, etc. Multiplications, additions or convolutions using residue arithmetic using a compound modulus may be performed by implementing the corresponding operation in the factor moduli and combining the results as shown in Figure 7 for cross-convolution [6]. Let r denote the least non-negative residue of x modulo M, and $r_i$ denote the least non-negative residue modulo $M_i$. Converting from r to $(r_1, r_2 \ldots r_T)$ is straightforward: $r_i$ is the remainder of r after dividing by $M_i$.

Example: let $M = 6, M_1 = 2, M_2 = 3$.

| r | $r_1$ | $r_2$ |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 1 |
| 2 | 0 | 2 |
| 3 | 1 | 0 |
| 4 | 0 | 1 |
| 5 | 1 | 2 |

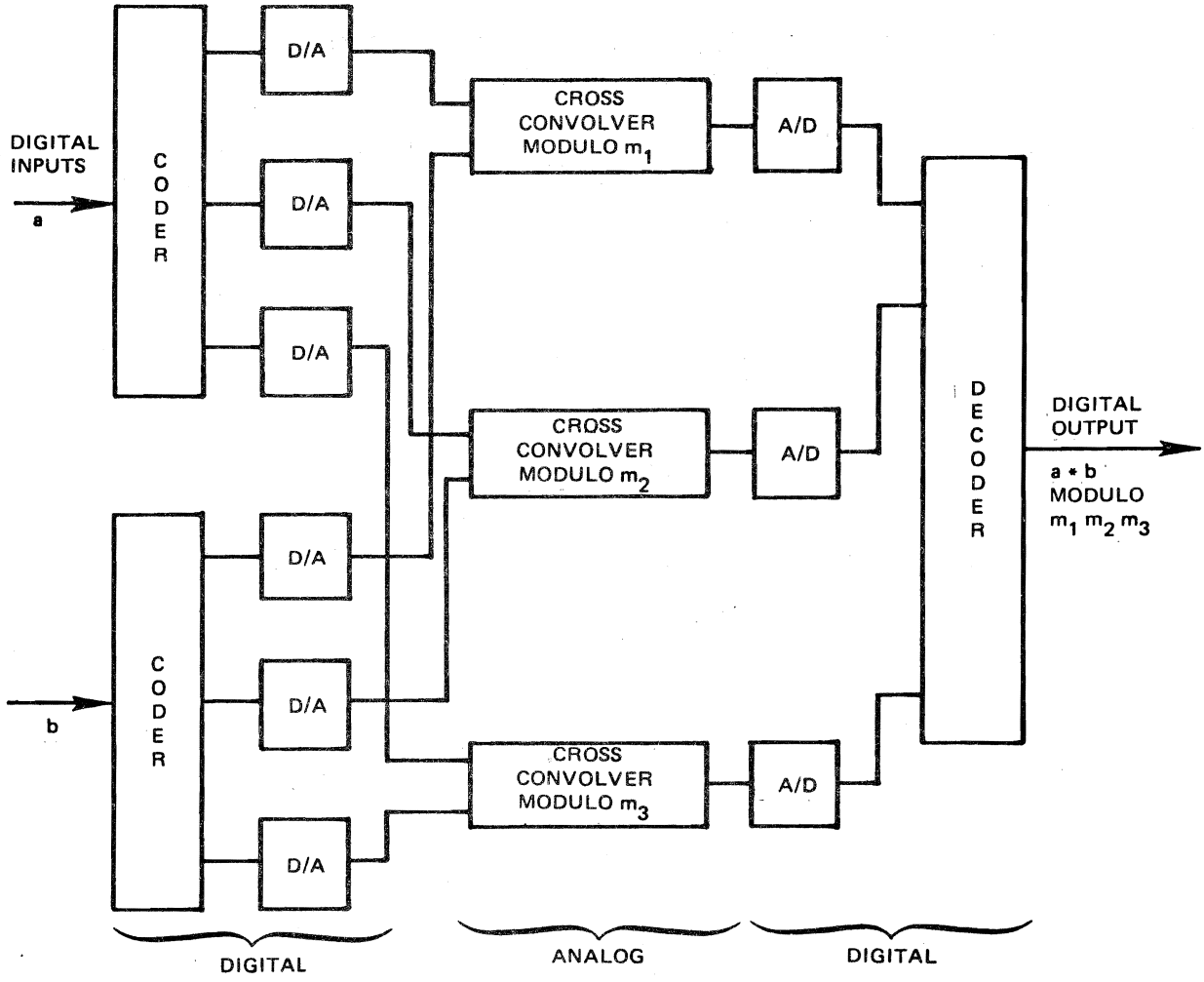



Figure 7. Parallel Analog/Digital Convolver on Residue Arithmetic

Converting from $(r_1, r_2, \ldots r_T)$ may be either simple or complicated depending upon the choice of the individual moduli $M_1, M_2, \ldots M_T$. For the appropriate choice of the moduli, the conversion from the individual residues to the residue relative to the product modulus may be implemented in terms of a small number of comparisons, bit shifts, and adds, and is hence a simple operation for digital implementation.

One further observation should be made concerning residue arithmetic: For signal processing tasks which use matched filtering, it is frequently sufficient to find that shifted version of one signal which is closest to a second signal, i.e., it is only necessary to compute $\Sigma_n [s(n) - r(m-n)]^2$. Since residue arithmetic permits all numbers to be represented by non-negative quantities, this permits a fourfold reduction in the number of modules required by calculating the distance directly rather than the crosscorrelation or crossconvolution. The crosscorrelation peak will occur at the same shift value as the minimum distances, and only the correct shift value is needed in applications such as echo location or communication using pulse position modulation.

# DIGITAL CORRELATION USING MULTIPLICATION BY BINARY CONVOLUTION

It has long been realized that the coefficients of the product of two polynomials is the convolution of their respective coefficients. This is in fact the basis for the convolution using the Z-transform or generating the function

$$A(z) = \sum_n a_n z^n$$

$$B(z) = \sum_n b_k z^k$$

$$A(z)\,B(z) = \sum_n \sum_k a_n b_k z^{n+k} = \sum_s \left(\sum_{n+k=s} a_n b_k\right) z^s$$

This equation may be applied to binary multiplication by letting z = 2 in the above identities.

If

$$A = \sum_{n=0}^{N_1-1} a_n 2^n$$

and

$$B = \sum_{k=0}^{N_2-1} b_k 2^k$$

then

$$AB = \sum_{k=0}^{N_1+N_2-1} \left[\sum_n a_n b_{s-n}\right] 2^s = \sum_s c_s 2^n \qquad (18)$$

If the digits $a_n$, $b_k$ take on the values of 0 or 1, this permits the multiplication of the two integers A, B where A may be 0, 1, . . . $2^{N1}-1$ and B may be 0, 1, . . . $2^{N2}-1$. In order to perform signed arithmetic, we may use symmetric offset binary representation where the digits $a_n$ and $b_k$ take the values ± 1. Then the range of values possible for A and B is ±1, ±3, . . . $\pm(2^n-1)$ where n is the number of bits in the corresponding number. The convolution required in Eq (18) may be performed in analog form by the CCD correlator and the subsequent summation performed digitally after analog to digital conversion as shown in Figure 8. The number of bits of resolution required for the A/D conversion is only $\log_2 (1 + \min (N_1, N_2))$.

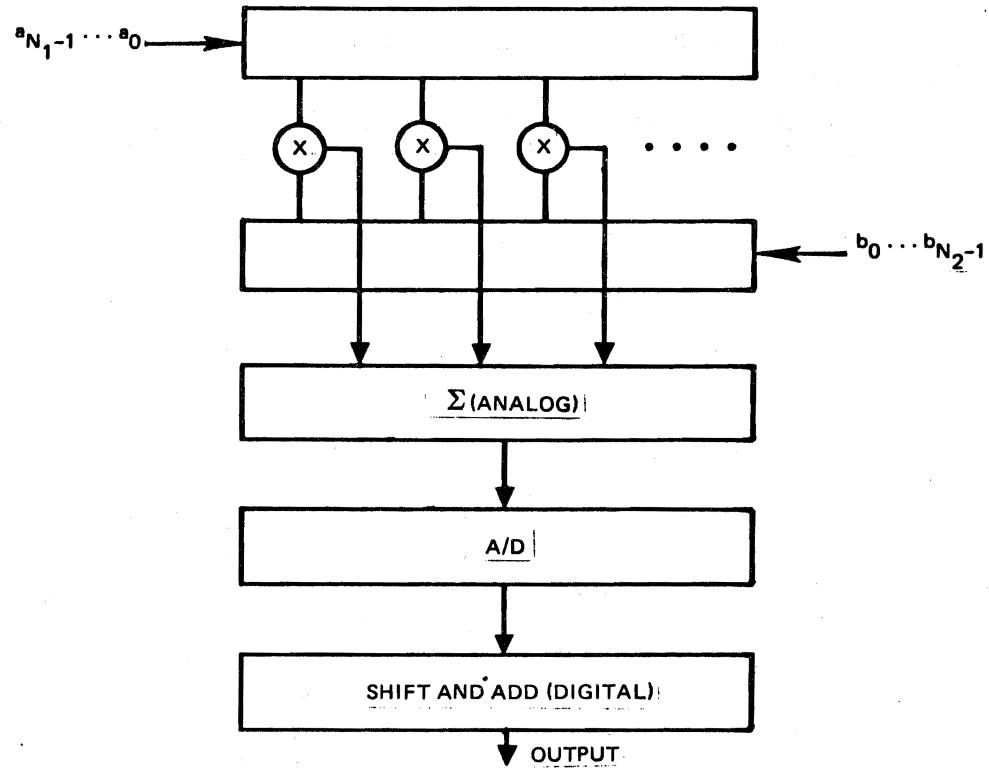



Figure 8. Analog Convolver Used as a Digital Multiplier

## CHIP DESIGN OF THE CCD CROSSCORRELATOR/CONVOLVER

The schematic diagram of the device is shown in Figure 1A. The device consists of two identical 32-sample CCD shift registers (called "signal" and "reference" CCD's), 32 squaring devices and a common summing element. Since it is difficult to transfer charges into one given "bucket" of a CCD from 32 different directions at once, eight partial sums, each of four terms, are performed "on-chip." These eight terms are available for subsequent analog or digital summation "off-chip."

One of the delay lines is designed in such a manner as to allow bidirectional shift of the information. The added flexibility is desired in order to perform both convolution and correlation functions with the same devices, thus eliminating the necessity to time reverse, by external components, the reference wave form before introducing it in the CCD. To achieve bidirectionality, the design of the terminal circuit is optimized for both injection and detection of the information.

The design implementing this concept has been completed and incorporates component modules to perform the following sequence of functions to compute a crossconvolution or crosscorrelation:

a. A floating diffusion input structure to perform charge injection into a CCD. The injected charge is proportional to the voltage differential between each sample of an input sequence and a d.c. reference. This technique provides a stable, uniform, low noise injection of the signal required for large dynamic range.

b. Thirty-two N-delay stages with non-destructive signal tapping at every other stage are naturally provided by a CCD shift register and a floating gate at every other stage,

c. A floating gate whose potential reflects the magnitude of the charge under it and thus provides the non-destructive sensing mechanism,

d. A second floating diffusion structure whose function is to modulate the charge injection and a second CCD (squaring device) proportionally to the input signal.

e. A suitably biased floating gate amplifier whose output voltage is proportional to the square of the voltage on the floating gate.

f. A charge addition structure to achieve a "summing bus" function by injecting charge into a common CCD potential well through multiple input structures. The output of this latter component is

$$\sum_{i=4k}^{4k+3} (s_i + r_i)^2 \quad \text{for } (k = 0, \ldots 7).$$

Two chips were designed: One implements the multiplier concept and the other the full 32-sample sum of squares module. The preliminary test results, discussed in this paper, relate to the multiplier chip.

Figure 9 in conjunction with Table 1 shows the functional form of the relationships which govern the operation of the sum of squares modules. Each equation in the table corresponds to one of the functions in the flow chart representing the system. The squaring equation is empirical; the other equations have been derived from theoretical considerations.

Tests were performed on the multiplier chip to verify (1) the relationship between the differential potential on the input gates and the charge injected, and (2) the relationship between the charge under the floating gate and the potential on the gate.

Similarly, extensive testing of the operation of the floating gate amplifiers was performed. These were tested in a DC mode to relate the input and output voltages. The square root of the output potential was plotted versus the input potential applied to the floating gate. Figure 10 (a and b) shows typical results. The second type of test performed was a small signal response. The bias electrode was held at a fixed potential and a periodic linear ramp signal was applied to the floating gate electrode. These results are shown in Figure 11 and demonstrate the squaring capability of the amplifier.

The response of the floating gate to a voltage on the bias electrode above it was studied and measured on a few devices. The expression for the potential on the floating gate is given by

$$V_{FG} = V_B + \frac{d}{T-t}\left[\frac{Q_{ss}}{C'_o} - \frac{\sigma_o}{C'_o} + V_o - V_o\sqrt{1 + \frac{2}{V_o}\left(V_B + \frac{Qss}{C'_o} - \frac{\sigma_o}{C'_o}\right)}\right]$$

where $V_B$ is the bias electrode potential, $C'_o = \epsilon_o K_o/(T - t)$, $\sigma_o$ is the stored charge, and $V_o = \epsilon_o K_s e N_A / C'^2_o$.

A linear response, as pictured in Figure 12, which appears to closely conform to the theory was obtained. The effect of the low capacitance probe used in the measurement on the response has not yet been evaluated.

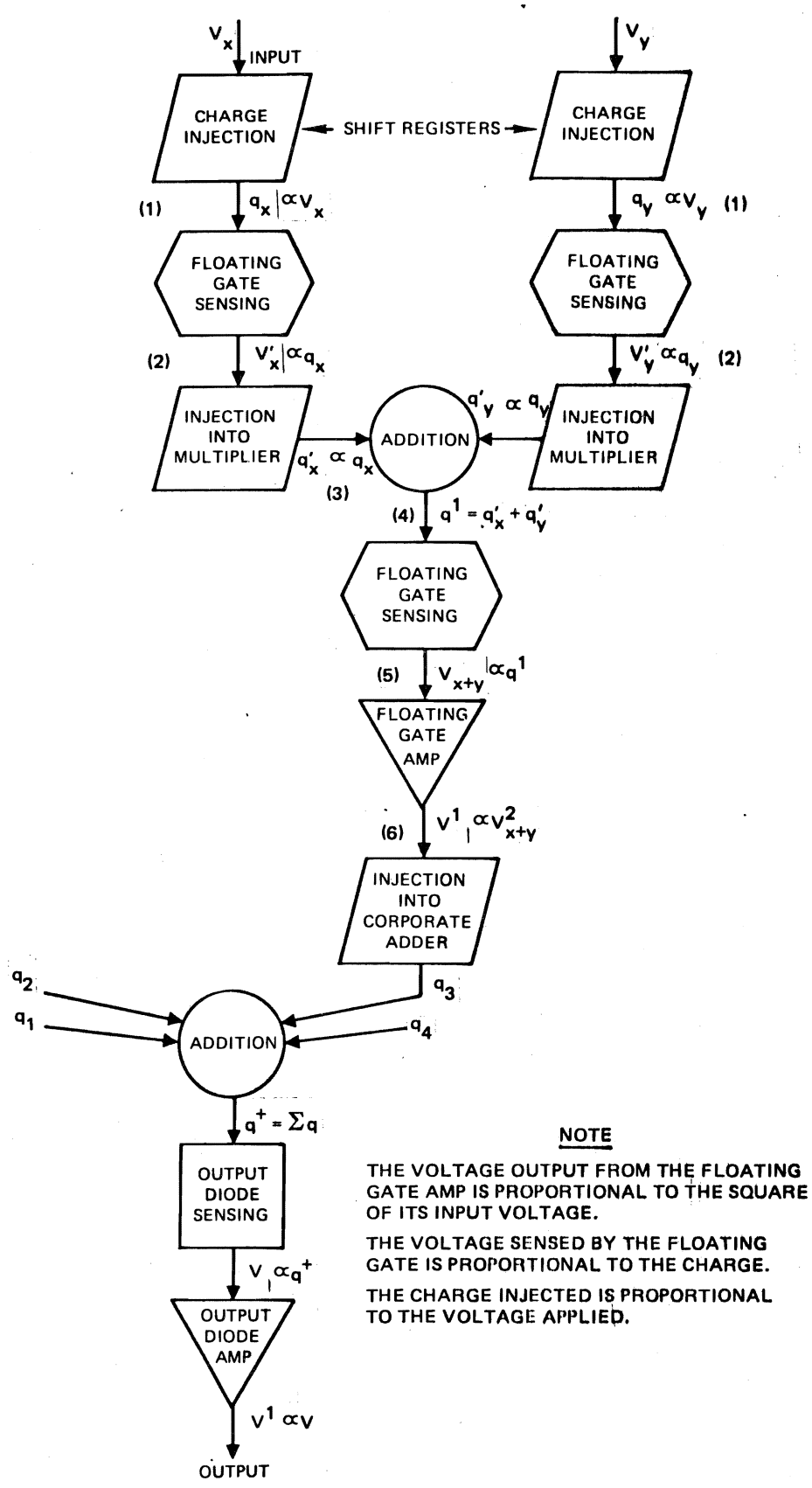

$V_x$
INPUT
CHARGE INJECTION
SHIFT REGISTERS
$V_y$
CHARGE INJECTION
(1)
$q_x \propto V_x$
$q_y \propto V_y$ (1)
FLOATING GATE SENSING
FLOATING GATE SENSING
(2)
$V'_x \propto q_x$
$V'_y \propto q_y$ (2)
INJECTION INTO MULTIPLIER
$q'_x \propto q_x$
(3)
ADDITION
$q'_y \propto q_y$
INJECTION INTO MULTIPLIER
(4) $q^1 = q'_x + q'_y$
FLOATING GATE SENSING
(5) $V_{x+y} \propto q^1$
FLOATING GATE AMP
(6) $V^1 \propto V^2_{x+y}$
INJECTION INTO CORPORATE ADDER
$q_2$
$q_1$
$q_3$
$q_4$
ADDITION
$q^+ = \Sigma q$
OUTPUT DIODE SENSING
$V \propto q^+$
OUTPUT DIODE AMP
$V^1 \propto V$
OUTPUT
NOTE
THE VOLTAGE OUTPUT FROM THE FLOATING GATE AMP IS PROPORTIONAL TO THE SQUARE OF ITS INPUT VOLTAGE.
THE VOLTAGE SENSED BY THE FLOATING GATE IS PROPORTIONAL TO THE CHARGE.
THE CHARGE INJECTED IS PROPORTIONAL TO THE VOLTAGE APPLIED.

Figure 9.

Table 1.

(1) $$\sigma_x = q_x/A = C_{FD}\,(V_x - V_o)$$

(2) $$V_{FG_x} = V_A + \alpha\sigma_x/C'_o$$

$$= V_A + \frac{\alpha}{C'_o}\,C_{FD}\,(V_x - V_o)$$

(3) $$\sigma'_x = C'_{FD}\,(V_c - V_{FG_x})$$

$$= C'_{FD}\left[V_c - V_A - \frac{\alpha}{C'_o}\,(V_x - V_o)\right]$$

To first order in $\sigma$:

$$\alpha = \frac{-d}{T-t}\left[1 + \sqrt{\frac{V_o}{2W}}\right]$$

$$V_A = V_B + \frac{d}{T-t}\left[W - V_B + \frac{V_o}{2} - \sqrt{2V_oW}\right] \quad V_B = \text{externally applied}$$

(4) $$\sigma = \sigma'_x + \sigma'_y$$

$$= 2C'_{FD}\left[V_c - V_A - \frac{\alpha}{C'_o}\,C_{FD}\left(\frac{V_x + V_y}{2} - V_o\right)\right]$$

(5) $$V_{FG_{xy}} = V_A + \frac{2\alpha}{C'_o}\,C'_{FD}\left[V_c - V_A - \frac{\alpha C_{FD}}{C'_o}\left(\frac{V_x + V_y}{2} - V_o\right)\right]$$

(6) $$V_{fga} = (A + B\,V_{FG_{xy}})^2$$

$$= \left\{A + B\left[V_A + \frac{2\alpha C'_{FD}}{C'_o}\left(V_c - V_A - \frac{\alpha C_{FD}}{C'_o}\left(\frac{V_x + V_y}{2} - V_o\right)\right)\right]\right\}^2$$

$$\equiv [G + H(V_x + V_y)]^2$$

where $$V_o \equiv \frac{\epsilon_o K_s e N_A}{C'^2_o} \qquad C'_o \equiv \frac{\epsilon_o K_o}{T-t}$$

$$W \equiv V_B + \frac{Q_{ss}}{C'_o} + \frac{V_o}{2}$$

$C_{FD}$ = floating diffusion capacitance

$\sigma$ = surface charge

$V_c$ = externally applied

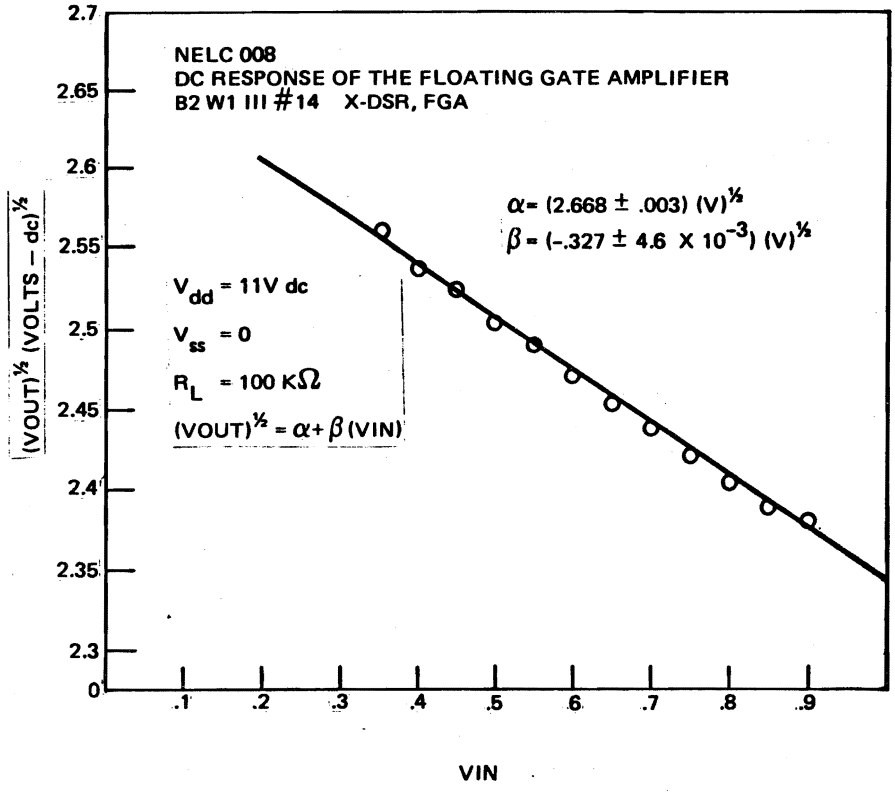
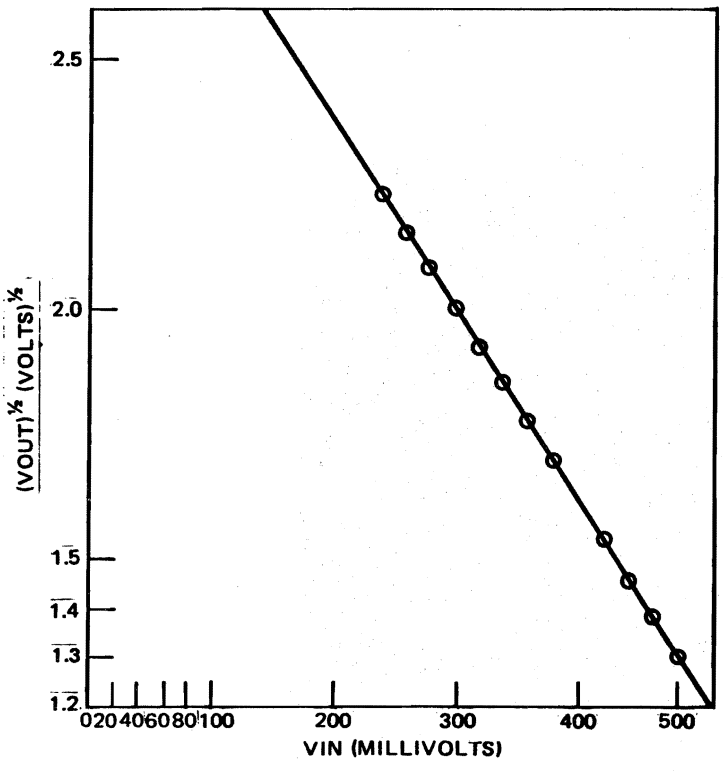



Figure 10a.




NELC 008
DC RESPONSE OF THE FLOATING GATE AMPLIFIER
B2W1 QUAD III #7
Y = DER, FGA

$V_{DD}$ = 11V

$V_{SS}$ = 0V

$R_L$ = 100 KΩ

(VOUT)$^{1/2}$ = $\alpha$+ $\beta$ (VIN)
$\alpha$= (3.169 ± 0.00702) (V)$^{1/2}$
$\beta$ = (-3.876 ±0.0199) (V)$^{-1/2}$

Figure 10b.

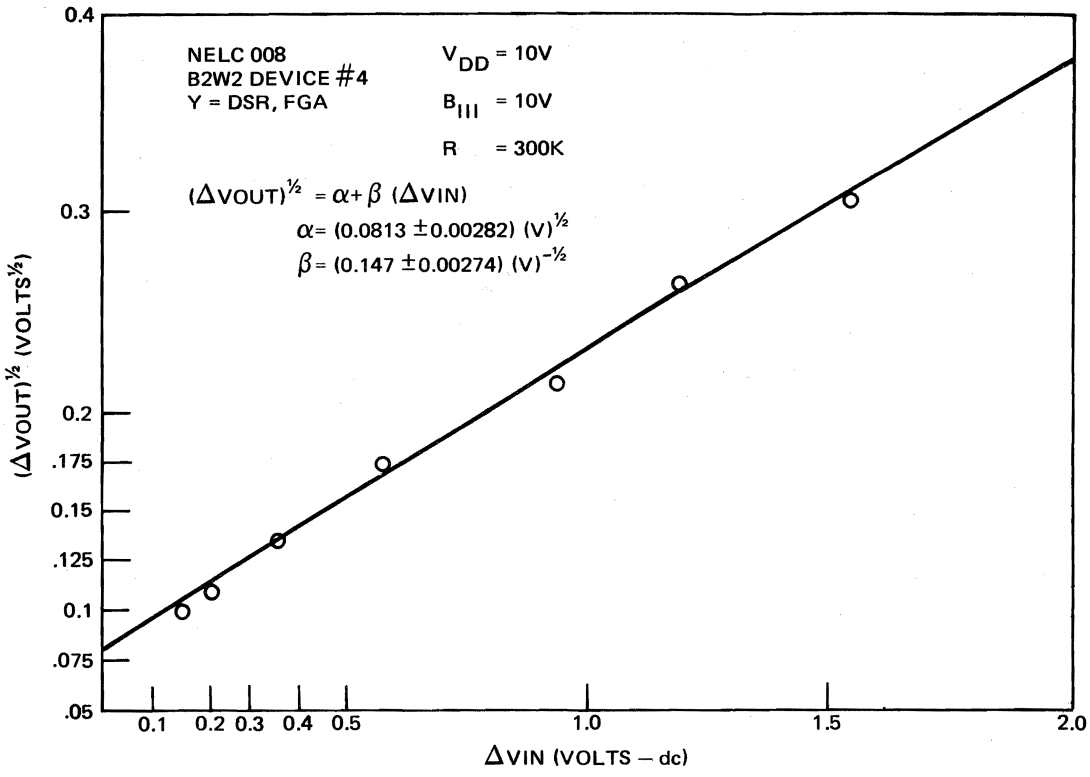



Figure 11. Small-Signal Response of the Floating Gate Amplifier

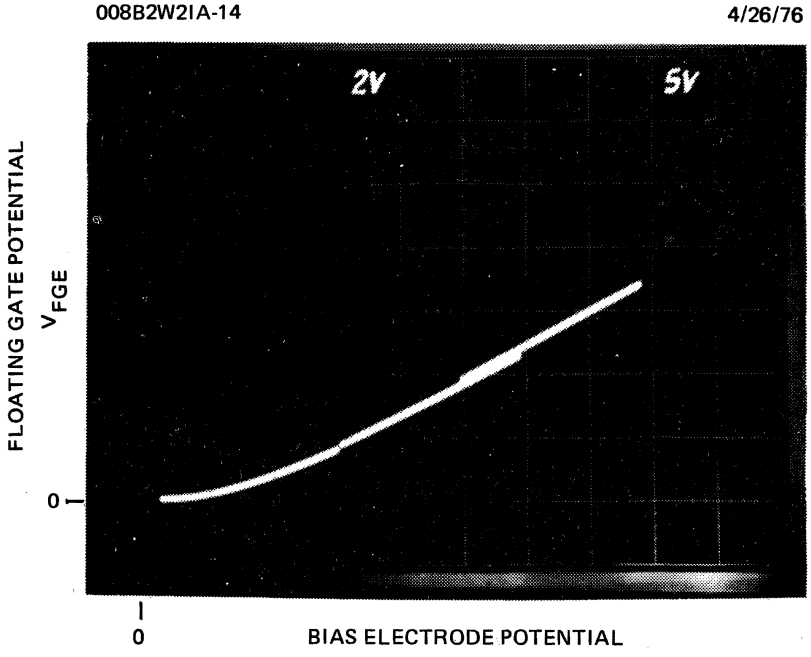



Figure 12. Variation of Floating Gate Potential with Bias Electrode Potential

## CHARACTERIZATION OF THE UTILITY OF THE CCD SUM OF SQUARES CHIP AS A DIGITAL COMPONENT

Let us first determine a necessary condition for the CCD correlator chip to be used as a digital component. Consider the block diagram in Figure 13. The correlator can be used as a digital component if the analog sum of four squares can be correctly digitized, that is if in Figure 13.

$$Z = (x_1 + y_1)^2 + (x_2 + y_2)^2 + (x_3 + y_3)^2 + (x_4 + y_4)^2$$

Suppose that $x_i$ and $y_i$ are each coded into levels $L_1, L_2, \ldots L_m$. Then $x_i + y_i$ can take on levels of the form $(L_i + L_k)$, i.e., at most

$$m + \frac{m(m-1)}{2} = \frac{m(m+1)}{2} \text{ distinct levels.} \tag{19}$$

If the levels are proportional to $0, 1, \ldots, m-1$ then clearly there are exactly $2(m-1)+1 = 2m-1$ distinct values of $L_i + L_j$. Let M denote the number of distinct levels of $L_i + L_j$. Then there are also M distinct levels of $(L_i + L_j)^2$. The sum

$$\sum_{i=0}^{3} (x_i + y_i)^2 \tag{20}$$

can take on at most $(M+1)M/2$ $[((M+1)M/2)+1]/2$ by iterating Equation (19). Let N denote the number of distinct levels that the sum (20) can take on. Then for a given m, N distinct levels must be distinguishable without error at the output of the correlator submodule to allow its use as a digital component. Let us estimate the accuracy requirements on the correlator by calculating N directly for m = 2, 3, 4, and 5 when the levels are $0, 1, 2, \ldots m-1$. The results are summarized in Table 2.

In order to correctly quantize the analog sum of four squares, it is necessary to correctly resolve 17 equally spaced or a minimum of 14 unequally spaced levels when binary inputs are used. The required four-bit A/D conversion can be accomplished using a multiple capacitor conversion circuit. [7, 8]

For the binary case, a much simpler multiplier can be based on LOGICAL AND if the input digits are 0 and 1 or on the EXCLUSIVE OR if the input digits are +1 and -1. If 65 equally-spaced or 46 unequally-spaced levels can be distinguished at the output, then binary sequences can be used for the input and a six-bit A/D converter will be required at the output.

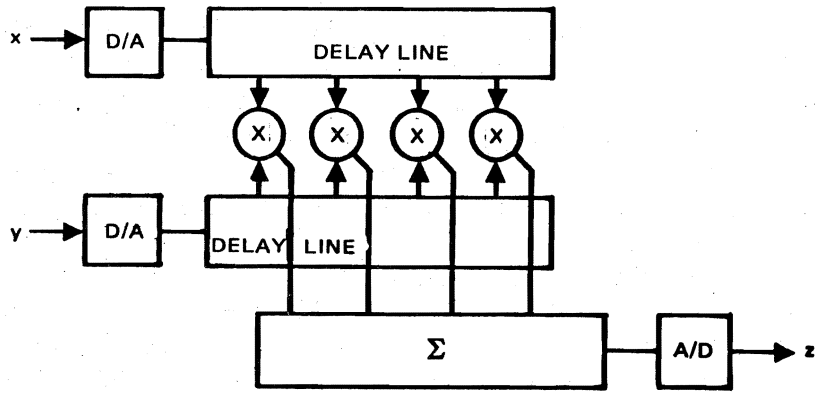



Figure 13. Sum of Squares Submodule

Table 2. Required Number of Correctly Resolved Output Levels for the Analog Sum of Four Squares When the Input Levels are Uniformly Spaced

| m<br>input levels | M<br>square levels | N<br>output levels |
|---|---|---|
| 2 | 3 | 14 |
| 3 | 5 | 46 |
| 4 | 7 | 103 |
| 5 | 9 | >200 |

If 14 levels or more could be distinguished at the output, then radix arithmetic can be utilized to obtain arbitrary high accuracy structures. Set the radix equal to R and suppose that

$$x_i = x_{i,0} + x_{i,1} R + x_{i,2} R^2 + \ldots x_{i,n-1} R^{n-1}$$

and

$$y_i = y_{i,0} + y_{i,1} R + y_{i,2} R^2 + \ldots y_{i,n-1} R^{n-1}$$

with

$$0 \leqslant x_{i,j}, y_{i,j} \leqslant R - 1$$

Then $n^2$ correlators are used to calculate exactly the $n^2$ sums

$$\sum_{i=0}^{3} (x_{i,j} + y_{i,j})^2 .$$

In the digital domain these $n^2$ sums are combined according to

$$\sum_{j=0}^{n-1} \sum_{j'=0}^{n-1} \sum_{i=0}^{3} (x_{i,j} + y_{i,j'})^2 R^{j+j'} \text{ to obtain } \sum_{i=0}^{3} (x_i + y_i)^2$$

exactly. Hence $n^2$ correlators can accept input data consisting of $R^n$ levels.

Let us now investigate the feasibility of using residue arithmetic to improve accuracy in conjunction with the analog sum of four squares. In order to minimize the number of modules, it is desired to use a small number of large moduli. Therefore, the preferred use of residue arithmetic is to provide a multiple precision mode for radix multipliers using analog convolution, rather than directly calculating correlation via a sum of squares.

In this preferred mode of operation, a two-fold increase in precision requires only a two-fold increase in hardware with no decrease in throughput. Conventional radix arithmetic would have required a four-fold increase in hardware or a two-fold increase in hardware together with a two-fold reduction in throughput.

An extremely powerful class of spectral estimators and noise cancellers may be based on adaptive filters using the Widrow LMS (Least Mean Squares) algorithm. The computations required by the algorithm are given in Eq (21), where $W_j$ is the weight vector at time j, $X_j$ is the input vector at time j, and $d_j$ is the training signal at time j. The difference $e_j$ is a feedback "error" signal. Different applications of the adaptive algorithm differ mainly in the way

in which the training signal is provided. An adaptive linear combiner and configuration for noise cancelling and adaptive line enhancing are shown in Figures 14, 15, and 16. [9].

$$e_j = d_j - (W_j, X_j) \qquad \text{(generation of feedback signal)} \qquad (21)$$

$$W_{j+1} = W_j + 2\mu\, e_j X_j \qquad \text{(tap update)} \qquad (22)$$

In adaptive filtering applications, $X_j = \text{col}\,(x_j, x_{j-1}, \ldots x_{j-N+1})$.

Note that at each time, N multiplications are needed to generate the feedback signal, and an additional N multiplications are needed to update the tap weights. These computations are not well suited to implementation via an FFT. Even the generation of the feedback signal is not a convolution because the weights change from one time sample to the next.

Because of the large number of required multiplications, the adaptive spectral estimators and adaptive noise cancellers have been limited to low bandwidth problems for real-time applications.

Multiple analog correlators used as digital multipliers can provide high accuracy multiplication in modules which combine both the signal storage and the arithmetic logic. These modules can be combined in a transversal filter structure to provide simultaneously the required signal storage and parallel computation while retaining the simplicity of common control.

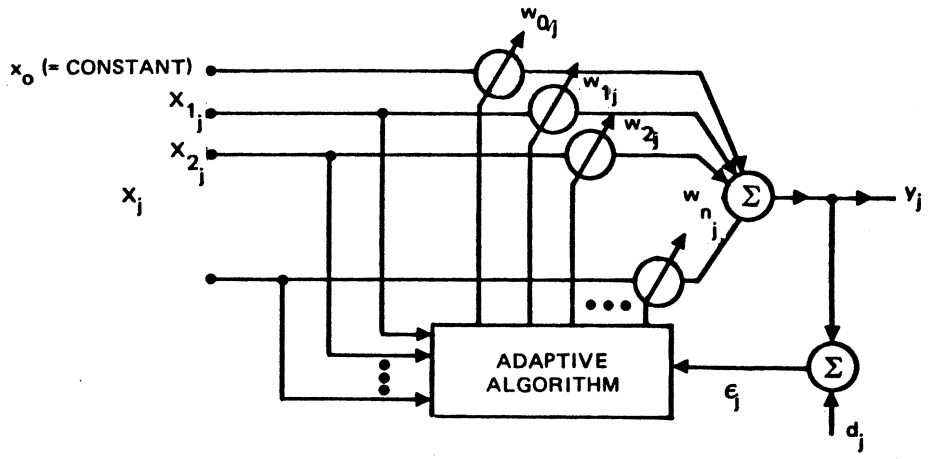



Figure 14. The Adaptive Linear Combiner

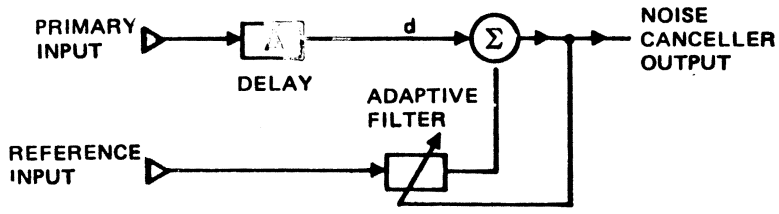



Figure 15. Adaptive Noise Canceller with Delay in Primary Input Path

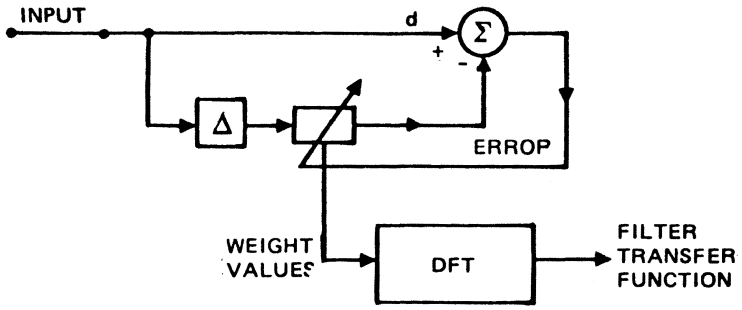



Figure 16. The Adaptive Line Enhancer.

## CONCLUSION

It has been shown that there are a multiplicity of ways in which an analog convolver can be used as a modular building block for digital correlation. For maximum throughput and minimum complexity, it may be used directly as an analog device. For applications requiring higher accuracy, analog convolvers may be combined with A/D converters and digital summation using radix arithmetic, residue arithmetic, or multiplication via convolution. Thus, problems which previously were not amenable to solution using analog CCDs may now be addressed with this technology.

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