The CCD Memory in Microcomputer Systems

by Howard Kornstein, Intel Corporation (UK) Ltd

The introduction of a single-chip 16K bit CCD memory device opened the way towards a low-cost disc and drum replacement semiconductor bulk storage system that not only outperforms the mechanical devices but which is also potentially more reliable. Before looking specifically at the microcomputer applications of the CCD memory device it is worthwhile discussing the basic technology and device architecture.

Device organization and operation

The CCD chip is known as the 2416 and requires the following power supplies: V_{DD} = 12 V and V_{BB} = -5 V. The output is formed by an open drain device to allow the outputs to be OR tied. For TTL compatible operation the output pin is usually tied to a resistor which is returned to V_{CC}. The pin layouts for both the 18 and 22 pin versions of the 2416 are shown in Figure 1.

The 2416 combines both serial and random address memory functions and, as shown in Figure 2, it comprises 64 256-bit charge coupled device (CCD) shift registers. The data in these registers is

simultaneously shifted by exercising the four-phase clock signals ϕ_1 through ϕ_4. After a shift cycle, each of the 64 CCD registers can be selected for an input/output (I/O) function by applying the appropriate 6-bit address code and applying cenable, chip select and write-enable signals in the required manner.

The organization is most easily understood by referring to Figure 3. In this diagram the CCD is thought of as a cylinder consisting of 64 'tracks' (representing the 64 CCD recirculating shift registers) with each track divided into 256 'sectors' (representing the 256 CCD data storage cells). The 'rate of rotation' of the cylinder is controlled by the four-phase clocks and is in the direction indicated by the 'shift direction' arrow shown in Figure 3.

Read/write is performed by 64 bi-directional data buffers (one data-buffer per track). These buffers are located in position 'A' of Figure 3. The cylinder is considered to rotate through the buffers so that each shift of the cylinder (controlled by the four-phase clocks) places the next sequential sector of each track 'in' the buffer. The buffers shown in column A also refresh each cell in addition to performing read/write functions. (Note that an additional refresh-only buffer is shown in column B of Figure 3. These buffers are located half way around the cylinder as shown).

Two basic addressing methods may be used to store data words in

the 2416:

1. In a given sector
2. Around a given track

In the first method the desired word is accessed by shifting the cylinder (using the four-phase clocks) until the sector (0-255) containing the word is coincident with the read/write buffers (shown as column A). The word is then accessed one bit at a time by addressing the appropriate track with addresses A_0-A_5. An example of this addressing technique is shown as the four-bit memory word N shown in Figure 3. The second addressing method places a word sequentially around the cylinder in a given track. Access to a particular word requires both a four-phase clock shift followed by a data access cycle for each bit of the word. (Note that for this case A_0-A_5 do not change once the desired track is accessed.) An example of this addressing technique is shown as four-bit memory word M in Figure 3. Of the two methods of addressing, sector addressing is the most commonly used.

A major advantage of the organization is the low four-phase clock driver power required to achieve the maximum serial data transfer rate of 2 megabits/sec from a single 2416. In most serial applications the four-phase clock signals are only required to operate at less than 55 kHz rate to obtain a 2 MHz I/O data rate. This is because the four-phase clocks are used solely to shift/refresh data and are not used to perform input/output

functions. For each shift of the clock, 64 'new' data bits are available in the 64 internal data registers for access through the address, chip enable and read/write control signals. These data control signals have a low input capacitance which makes them very easy to drive.

An alternate method of visualizing the organization of the 2416 is shown in Figure 4. This diagram is derived from the cylinder shown in Figure 3 by imagining that the cylinder is cut along the line marked C (between sector 0 and 255) and laying the cylinder out flat.

The 2416 internal memory array is comprised of four-phase surface channel charge-coupled structures. The CCD structure is formed by a series of MOS thinfield gate oxide devices placed as shown in Figure 5. Note that these MOS devices do not have the source/drain diffusions usually associated with other MOS structures. Figure 5(a) is the top view of the storage array and illustrates that the clock phases are laid out perpendicular to the shift register channels. Electrical isolation between shift register channels is obtained by channel stop diffusions and thick film oxide methods. Data input/output connections to the registers are obtained from n+ diffusions at the ends of the registers.

Data Storage

The CCD stores data in the form of charge, as do all dynamic MOS memory devices. Indeed, in many respects the storage mechanism of

the 2416 is very similar to the 4096 bit random access memories implemented with single transistor cells. The storage element is most easily understood if it is considered to resemble a 'potential well'. This potential well is formed when a positive voltage potential is applied on the clock gates. The positive voltage repels the majority substrate carriers (holes) from the vicinity of the gate and forms a charge depletion area under it. This depleted region has the capability of accepting and storing a negative charge packet as long as the gate forming the well remains sufficiently positive with respect to the substrate.

The CCD structure is inherently dynamic and therefore must be refreshed periodically to maintain data. The dynamic nature of a CCD device is the result of thermally generated carriers (traditionally called 'dark current effect') which acts to fill an uncharged potential well with charge, thereby changing that particular cell's logic state.

Data Transfer

Figure 6 shows the relationship between the 2416 four-phase clock sequence and the CCD data storage and transfer mechanism.

The position of potential wells relative to the four-phase clock levels is shown in Figure 6(a). When the clocks are sequenced in the manner outlined in Figure 6(b), the potential wells generated provide a 'low impedance' path for the charge packets to follow.

At time A, only the ϕ_2 gates are at a high level forming a storage

well under the ϕ_2 gates. The storage well is assumed to contain an externally injected charge packet. The origin of the charge packet will be discussed later. At time B, both ϕ_2 and ϕ_4 gates are high and an additional storage well is formed in the substrate under the $\phi_4$gates. Note that the storage wells under the ϕ_4 gates do not now contain charge packets. At time C, ϕ_2, ϕ_3 and ϕ_4 gates are all high, which forms ϕ_3 storage wells overlapping both the ϕ_2 and ϕ_4 storage wells. Thus a continuous storage well is formed from the ϕ_2 gates to the ϕ_4 gates which allows charge packets under ϕ_2 gates to disperse throughout the charge wells of all three gates. At time D, the ϕ_2 gate goes to a low level eliminating the storage well under it. This forces the charge packet into the remaining storage wells under the ϕ_3 and ϕ_4 gates. At time E, the charge transfer is complete when the ϕ_3 gate voltage goes low, which forces the charge packet into the remaining storage well under the ϕ_4 gate. The charge packet (data) has now been shifted by one bit position. Note that the shift execution time shown in Figure 6 is the time that data is being shifted as defined by periods B, C and D.

Applying clocks in the above manner (ϕ_3 shift) results in a parallel shift of all data. Another shift cycle can then begin by utilizing ϕ_1 and ϕ_4 (ϕ_1 shift) thus completing a full cycle on the four-phase clocks. The shifting mechanism using the ϕ_1 and ϕ_4 clocks is identical to that described for the ϕ_3 and ϕ_2 clocks.

CCD in Microcomputer Systems

When a microcomputer system requires a large amount of read/write storage and the reliability aspects of an all-semiconductor system are to be preserved, it is worth looking at a CCD memory as an alternative to the drum store. Previously, the only way of implementing such a system was to employ several circuit cards. However, with the CCD a memory of 131,072 eight-bit words (1 Mbits) can easily be implemented on a single circuit card, as shown in Figure 7. This memory can achieve data rates of 16 megabits per second with a clock frequency of 55 kHz.

With such high data rates it would be normal for a direct memory access system to be implemented in which the microprocessor relinquishes control of the address and data busses and data is transferred to and from the CCD memory straight into the system's read/write memory at the maximum data rate.

A microcomputer system comprising three cards: SBC-80/10 computer card, 16K RAM and the CCD card mentioned above, would provide a system with 17K bytes of RAM, 4K bytes of program memory, 48 programmable I/0 lines complete with line drivers and terminators, a communications interface for teletype or VDU, and a high-speed bulk store of 128K bytes. Not so very long ago a computing system of this capacity would have occupied a fair sized room and would have cost a great deal of money. The advent of the microcomputer and the CCD has reduced the size and cost by several orders of magnitude.

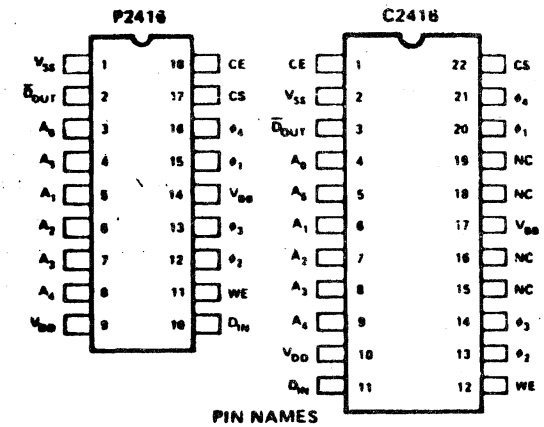

Figure 1. 2416 Pin Configuration.

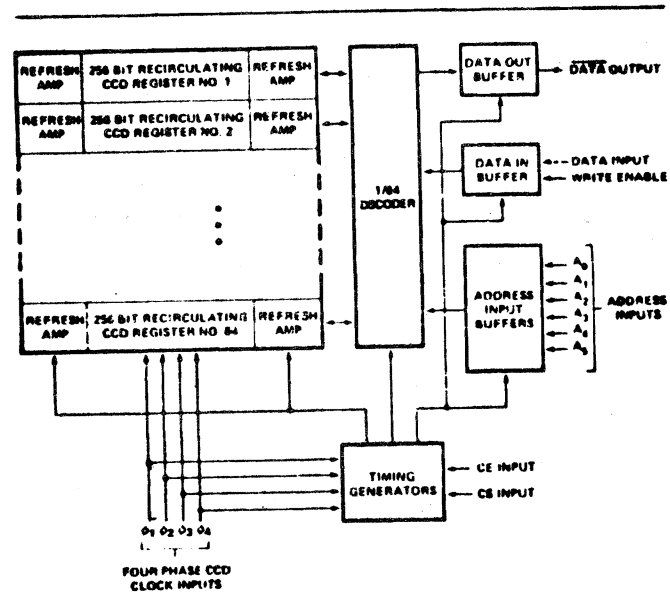

Figure 2. 2416 Block Diagram.

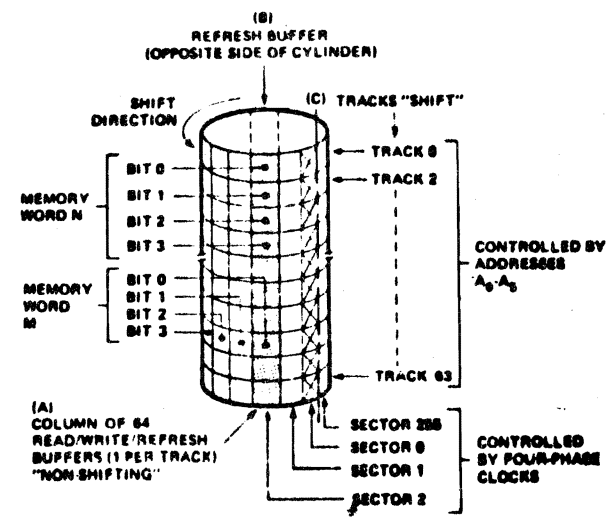

Figure 3. Symbolic 2416 Organization.

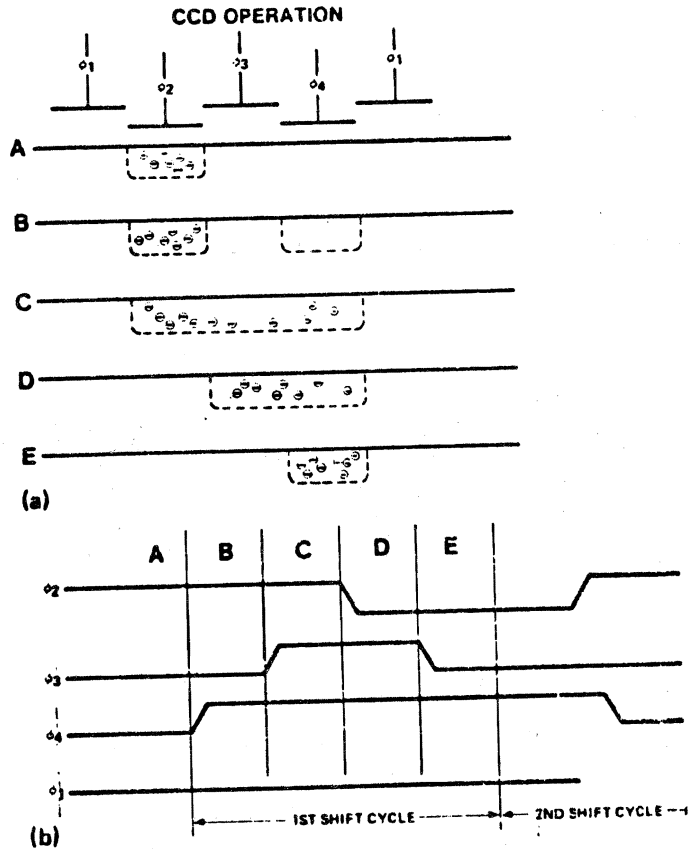

Figure 6. 2416 Charge Transfer Mechanism.