DEVICE DESIGN FOR CCD DIGITAL MEMORY

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ABSTRACT

The device design factors necessary to produce a practical CCD digital memory are considered. The economic influence of the available alternatives is stressed. Among the predominantly MOS circuits considered are the input charge writing techniques, the digital sense amplifier, and the half-charge generator. Among the CCD design considerations treated are the issues of buried channel versus surface channel, transfer efficiency, and leakage current. The chip organizations of existing components are discussed. The design rule factors which limit the memory density of these architectures are established. An interlaced ripple SPS organization which circumvents these limitations is discussed as well as the possibility of multilevel storage.

It is concluded that, in the near term, 64K-bit CCD block organized interlaced ripple SPS organizations will emerge and result in a packing density of 3 or 4 to 1 as compared to MOS single transistor RAMS. These will have a data transfer rate of 4MHz and an average latency of less than 0.5 ms. Power dissipation will be between 1 and 5 μW/bit at standard power supply levels. The price per bit will be approximately 1/4 the price of MOS RAMS. As a consequence, it is predicted that by 1980 more CCD bits will be shipped annually than any other semiconductor memory technology.

I. INTRODUCTION

The governing factor in CCD digital memory component device design is economics. The utility of a memory technology in a system is determined by the tradeoff between cost and performance. Traditionally, this is expressed by the familiar cost vs access time curve, shown in Figure 1. This curve reveals a gap (the so-called "memory gap") which exists between MOS memory and rotating electro-mechanical memory. CCD is one of the several technologies which can fill this gap. Although convenient, the use of access time alone rather than a weighted sum of access time and block transfer time somewhat over simplifies the real picture as has been indicated in a paper by Pohm, (Ref. 1). Nonetheless, practical economics indicates that in order for CCD to be viable as a memory technology it must be between two and four times less expensive than MOS random access memory. In order to achieve this, the CCD designer must strike a judicious balance between process complexity, device performance and die size. A CCD memory process must be no more complex than a typical MOS n-channel process. As a result of recent work in CCD and MOS technology this appears to be a practical assumption. With this issue aside, the designer then must consider the tradeoffs between performance and die size and address the design issues which affect these two important parameters.

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In this paper we will consider some of the more important design issues keeping in mind the economic realities of the ultimate product. These considerations include chip organization, buried channel versus surface channel technology, die size and the use of techniques for increasing the bit density in the memory matrix, signal handling capability, charge writing circuits, sense amplifier circuits, leakage current, and finally, power dissipation.

II. CIRCUIT DESIGN CONSIDERATIONS

A. MOS Related Circuits

In the design of a CCD memory component it is necessary to have numerous MOS peripheral circuits to support the basic memory function. Those circuits which must be designed most carefully are those where the MOS and CCD interface.

(1) Input Charge Writing Techniques

One of the most important interface circuits is the input charge writing circuit. The design of this circuit is dependent on whether the CCD is buried channel or surface channel. (In the case of a surface channel CCD, the circuit must be capable of writing a "fat zero" in place of a "true zero" (no charge)). In addition, the design must be insensitive to process variations; that is, it must be self-metering. There are two basic approaches to the design of a CCD charge input circuit. These are characterized by an input diffusion, an input gate and a first storage electrode and are illustrated in Figure 2.

The first scheme (Figure 2(A) described in the literature by Tchon (Ref. 2) and Mohsen (Ref. 3) operates by clocking the input diffusion. The voltage on the diffusion is lowered to a point where charge can spill over a barrier into a storage well. Before the end of the cycle, the diffusion is raised to a high voltage, and any excess charge in the well is drained off. The second scheme, shown in Figure 2(B) is the complement of this approach where the diffusion potential, V_S, is held constant but the input gate is clocked. In this case, the input storage well and its barrier are clocked to a high potential, thereby filling up the well. Before the end of the cycle the gate is lowered and excess charge is spilled back into the diffusion. This approach has been described in the literature by Varshney, et. al. (Ref. 4) and, like the first, is self-metering.

In each of these cases, the first well is slightly smaller than the internal wells in the CCD. This is controlled by the geometry of the layout and is required so that as leakage current is added to the charge packet as it transfers through the CCD, the charge level will not exceed the saturation limit of the internal CCD cell. Typically, the input charge level for a logical "1" is on the order of 75 to 80% of the saturation limit of the internal CCD cells. As will be discussed later, this determines the permissable leakage current within the memory structure.

(2) Digital Sense Amplifier

Perhaps the most important circuit in the design of a CCD memory chip is the sense amplifier. This circuit must be capable of detect-

ing charge levels as small as 50 fC with set up times less than 50 ns. In order to achieve this performance the designer usually uses a balanced approach. Balanced sense amplifier designs have been reported by Rosenbaum, et. al. (Ref. 6), Varshney, et. al. (Ref. 4) and Guidry, et. al. (Ref. 7). Schematics for these sense amplifiers are shown in Figure 3. Note that all use the variation in voltage on the gates of the load devices to determine which way the latch will set up. A more careful look, however, shows that in other respects the sense amplifiers are different. In Figure 3(A) the input to the sense amplifier (the output of the CCD) is to one side of a balanced flip-flop while the other side is to a dummy charge generator similar to the approach used in some MOS RAM designs. The amount of charge from the dummy charge generator can be adjusted by design to establish the discrimination level of the sense amplifier. In Figure 3(B) a reference voltage generated on-chip by a reference generator circuit is applied to the opposite side of the sense amplifier from the CCD input charge. This reference voltage generator is itself a sense amplifier which is identical to all of the other sense amplifiers in the memory, but with a dummy shift register for its input. The dummy shift register provides an input charge of approximately 1/2 of the saturation charge limit. A feedback circuit then adjusts the voltage on the opposite side so that the latch sets up neither as a "1" nor as a "0". This reference voltage is then supplied to the remainder of the sense amplifiers throughout the circuit. It is important that the sense amplifier in the reference voltage generator circuit be laid out in a manner identical to the sense amplifiers in the remainder of the memory so that layout imbalance cannot affect its operation. This is a very important consideration when the area available for the sense amplifier is very small and it may not be possible to lay out the circuit precisely symmetrical. This layout insensitivity is the principal advantage of this approach.

The sense amplifier shown in Figure 3(C) is very similar to that of Figure 3(A) except that both sides of the sense amplifier are used to sense data and both sides have dummy shift registers. The selection of the side used for data and the side used for reference is determined by the address decode. The design considerations for this type of circuit are similar to those of Figure 3(A) except that in this instance it is imperative that the amplifier be perfectly balanced. In circuits where ample room is available to lay out the sense amplifier, this is, in general, not a penalty. The sense amplifier in Figure 3(C) has one other very important feature. This is the decoupling circuit which decouples the output diffusion capacitance from the input capacitance to the sense amplifier (Ref. 7). Schemes similar to this have been discussed previously (Ref. 8) but all have suffered from pattern sensitivity and slow speed.

In the circuit in Figure 3(C), the floating output diffusion is precharged during the off cycle. This sets the output diffusion at the threshold of the transmission device. Subsequently, when the CCD charge is transferred to the floating diffusion, the transistor turns on and the signal charge is transferred to the input of the sense amplifier. In the circuit reported, the capacitance ratio between the output diffusion and the input to the sense amplifier is approximately 5 to 1 (250 fF versus 50 fF). This gives an effective voltage gain of five and makes the sense amplifier latch faster and its design much less critical. Simulations indicate that the set up time for this design is approximately 25 ns.

Not all sense amplifier configurations need be balanced.

For example, in the case of a serpentine architecture, where it is necessary for data moving in one direction in one register to be refreshed and written into an adjacent register with data moving in the opposite direction, the design of a so-called "turnaround" cell is required. Due to layout restrictions a balanced configuration is not practical. "Turnaround" cell design has been reported by Chou (Ref. 5) and Varshney, et. al. (Ref. 4) in which the information coming from the CCD shift register is placed on a precharged output diffusion which, in turn, modulates the gate of a subsequent transistor, as shown in Figure 3(D). This transistor is then either conducting or non-conducting, depending upon the level of charge at the input. Note that this refresh amplifier inverts the data. Turnaround cells lay out in no more than two mils^2 and, because they are dynamic, consume very little power. They are not practical for output configurations because of their very low driving capability.

(3) Half-Charge Generators

In each of the balanced sense amplifier designs discussed above, it is necessary to generate a reference charge which ultimately is compared with the data. This reference charge is approximately 1/2 of a full well, 1/2 Q_{SAT}. Such a half-charge packet can be generated in one of two ways. One is to generate a full charge packet, transfer it into a CCD register which splits the CCD channel in half with half of the charge being destroyed and the other half moving into the comparator circuit. Alternatively, the half-charge can be generated by designing a half size input well and transferring this reference charge to the comparator circuit. The latter scheme is more sensitive to process variations and consequently is less accurate. However, it has the advantage of occupying less space than the first case considered. The channel splitting approach has been used by Varshney, et. al. (Ref. 4). The geometrically smaller half charge input cell is more common and has been reported by a number of workers.

B. CCD Design Considerations

(1) Buried Channel Vs. Surface Channel

Superficially, it may appear that surface channel CCD technology is superior to buried channel technology for digital memory because it permits a greater charge handling capability and because distinguishing zeros and ones rather than an analog continuum does not require a high degree of charge transfer efficiency. Although there is some merit to these arguments, a full technical consideration is more complex. In making a selection between buried channel and surface channel, it is necessary to consider the charge required to obtain reliable performance, the margins needed in the input and sense amplifier circuit, the amount, if any, of fat zero needed and its effect on signal charge, the maximum frequency of operation desired, and the frequency range over which the circuit must operate, including the possibility that it may be desirable to temporarily halt the memory.

In an optimum design the margins obtained at the sense amplifier are invariant over all operating conditions. Let's take a closer look at buried channel versus surface channel with this consideration in mind. First, in order to use surface channel technology effectively, even in

memory devices, a "fat zero" is necessary to compensate for surface state losses (the effect of fat zero on transfer efficiency in surface channel CCD is reported extensively in the literature; for example, see Tompsett (Ref. 9). As pointed out in Tompsett's article, a "fat zero" does not provide complete compensation for surface state losses due to "edge effects". Basically, the edge effect theory states that the electrons transferring in a CCD tend to be confined to the center of the channel. The charge in a fat zero is confined to a smaller portion of the channel than the greater quantity of charge in a "1". The difference between the two areas is uncompensated by the fat zero and, hence, produces the full loss of charge due to surface states in these regions. For wide channel CCD's this is not a serious problem because this one or two micron region is not a significant fraction of the total channel width. However, in the case of a very high density CCD memory, one or two microns out of perhaps fifteen microns is a very significant fraction and surface state losses are proportionally larger. This places great demand on the process to maintain minimum surface state densities. Typically, the surface state density must be on the order of 10^9 $eV^{-1}cm^{-2}$ in order to give satisfactory transfer efficiencies in narrow channel surface channel CCD's. In addition, even with an effective fat zero the transfer efficiency is enhanced only for operation at a constant frequency. This is due to the fact that surface states are more-or-less uniformly distributed throughout the entire band gap. If operating frequency is abruptly changed, new surface states must be either filled or emptied resulting in a possible change in the data in the register. Depending on the magnitude and abruptness of the frequency change data bits can be dropped. In particular, the possibility of halting the memory momentarily is excluded unless the fat zero is made inordinately large. If it is necessary to make the fat zero very large the change handling capacity benefit associated with surface channel technology is not realized. If the fat zero must be 50% of QSAT, the operational charge handling capacity for a surface channel CCD is no larger than for a buried channel CCD. This seems to be the case with narrow channel devices.

If it is not necessary to change the frequency of operation and still retain data, then such a large fat zero is probably not necessary. Although one must still contend with the design of input circuits which generate a fat zero, the design of a surface channel sense amplifier is less difficult because level shifting from buried channel potentials to normal MOS levels is not required.

Detailed studies done at the author's laboratory comparing buried channel to surface channel for high density memory applications have suggested that the buried channel approach is superior. The design issues are generally easier to attack and the knowledge that the transfer efficiency and performance of the register are essentially constant over a range of operating conditions is a significant design and process benefit.

(2) Transfer Efficiency in High Density CCD

In surface channel technology the primary factor determining transfer efficiency is surface state density. As indicated above, several workers have recorded densities as low as 10^9 eV^{-1} cm^{-2}, however, a more representative number in production is 10^{10} eV^{-1} cm^{-2}. For a narrow channel, high density CCD, this value is too large to give acceptable transfer efficiencies even in the presence of a nominal fat zero. However, it is likely that the state-of-the-art will advance so that surface state

densities in the range to 4 to 5 x 10^9 eV^{-1} cm^{-2} can be achieved in a production environment. Under these conditions and with adequate fat zero a surface channel design may be viable.

In the case of buried channel technology, the primary factor determining transfer efficiency is bulk traps. Unlike surface states, bulk traps tend to be localized in the band gap. Several workers have reported the observation of bulk traps with time constants from 8 μsec to approximately 1 msec. Like surface states, bulk traps reduce transfer efficiency; however, bulk trap densities are on the order of 10^{11} cm^{-3}. For a 1 μm deep buried channel layer, a bulk trap density of 10^{11} cm^{-3} is equivalent to a surface state density of only 10^7 eV^{-1} cm^{-2}. The results, an order of magnitude better transfer efficiency in the buried channel device.

(3) Leakage Current

A typical "1" written into a CCD register is approximately 3/4 of the saturation value of that register. This is to allow 1/4 Q_{SAT} for leakage current accumulation as the packet transfers through the register. As a consequence, the storage time is:

$$\tau_s = \frac{Q_{SAT}}{4I_L(T)} \qquad (1)$$

where I_L (T) is the leakage current density.

The refresh frequency requirement of the memory is inversely proportional to the storage time and consequently, is proportional to the leakage current. The leakage current is a strong function of chip temperature. Furthermore, the chip temperature is, in general, substantially higher than the ambient temperature. For example, for a package thermal resistance Θ_J of 75°C/watt and a memory power dissipation of 400 mW, chip temperature is 30°C above ambient.

The leakage current density is given by the equation:

$$I_L\ (T) = 1/2\ qn_i\ (S_o + \frac{WD}{\tau_o} + \frac{2n_iL_n}{N_A\ \tau_n}) \qquad (2)$$

where S_o is the surface recombination velocity, WD is the depletion depth, L_n is the diffusion length, N_A is the acceptor concentration, τ_o and τ_n are the lifetimes of electrons in the depletion region and neutral bulk respectively, and n_i is the intrinsic carrier concentration and is proportional to $e^{-\frac{Eg}{2kT}}$

Equation 2 is plotted in Figure 4. Note that in the temperature range between 0°C and 70°C the leakage current rate doubles every 8°C to 9°C. However, at higher temperatures, the leakage current increases at a more rapid rate as the diffusion current term in the equation becomes more and more significant. Based on reasonable assumptions for bit size, charge storage capacity, and power dissipation, peak leakage currents less than 20 to 30 nA/cm^2 at room temperature must be achieved by the process. The state-of-the-art for average leakage current is about 10 nA/cm^2. Consequently, the leakage current peak can be no worse than 2 to 3 times the background. In a memory which is to be halted as a normal mode of

operation, the designer must assume peak leakage current in allowing for adequate margins. In a memory in which the data is continuously moving, it is necessary to assume leakage current only. This has a significant impact on the complexity of the process technology and, consequently, on the cost of the manufactured unit. Nonetheless, the present state-of-the-art is capable of producing high density CCD's which can operate comfortably at 70°C ambient.

(4) Power Dissipation and Operating Temperature

There are substantial benefits, however, in lowering the temperature of operation of a CCD memory. At increased temperature the memory must be refreshed more frequently. Generally, for a large secondary memory only a small fraction of the data is active at any one time whereas most of the memory is being refreshed. Since this must be done more frequently at elevated temperatures the power dissipated by the memory increases proportionately, and the refresh duty cycle correspondingly increases. Assuming a 100 megabyte memory with an 8 byte wide access channel, the system power dissipation as a function of ambient temperature is shown in Figure 5. Reducing the ambient operating temperature of the memory system from 70°C to 25°C results in a 67% power reduction.

Power saving is not the only benefit of reducing temperature. The reliability is also enhanced. Figure 6 shows the Arrhenius plot which graphs relative component life as a function of ambient operating temperature. Depending on the activation energy, the life of a semiconductor memory will be extended by one or two orders of magnitude as the ambient temperature is reduced. In summary, although CCD memory components have been and will continue to be designed to operate at conventional ambient temperatures, there are some benefits to be gained by reducing ambient temperature. These are: (1) storage time increased by 1½ orders of magnitude, (2) average power is decreased by one half order of magnitude, (3) reliability is improved by 1 to 2½ orders of magnitude, (4) the refresh duty cycle is reduced by 1½ orders of magnitude and (5) access speed is improved by about 25%. The logical conclusion is that future memory systems using dynamic memories and, in particular CCD will most likely be cooled.

Despite this prediction today's designer must operate on the assumption that the part will operate in an ambient of 70°C. This requires consideration of internal organization so that wherever possible leakage currents can be averaged and the memory area utilization factor maximized. At the same time, the process engineer must maintain state-of-the-art leakage currents on the production line. Significant experience has been gained in the manufacture of single transistor MOS RAMS and is contributing to practical low cost CCD memory components.

III. CHIP ORGANIZATION

A. Present Chip Organizations

The CCD design issues discussed above lead naturally to a discussion of chip organization. Today there are four organizations which are commonly recognized. These are: the serpentine, the drum, the serial-parallel-serial (SPS), and the line-addressable random access

memory (LARAM) organizations. These are illustrated schematically in Figure 7.

The first organization, the serpentine, is composed of a number of shift register segments each connected by a "turnaround cell" so that the data passes serially through all of these register segments. Architectures of this type have been reported by Varshney, et. al. (Ref. 4) and Rosenbaum, et. al. (Ref. 10). The drum organization is similar to the serpentine except that instead of connecting the register segments serially, the register segments are connected in individual loops which are accessed through a decode circuit. An architecture of this variety has been reported by Chou (Ref. 5). The serpentine and drum architectures are referred to as synchronous organizations since all the bits in the memory move simultaneously. In the serial-parallel-serial organization the data is introduced into a fast register which, when full, transfers the data into an adjacent set of slower parallel registers on a line-by-line basis. After the data moves through these parallel registers, a final transfer into another fast serial register occurs which takes the data to the output. This architecture has been discussed by Mohsen, et. al. (Ref. 3). In the line-addressable random access memory architecture the CCD shift registers segments are not interconnected, but rather are driven through a decode matrix which activates each register segment independently. Input and output are through common busses. This organization has been discussed by Gunsagar, et. al. (Ref. 11). The SPS and LARAM architectures are non-synchronous because not all the bits in the memory move simultaneously. We will not discuss the details of any of these architectures in this paper. It should be noted, however, that all the structures discussed above require two or more electrodes per bit. Based on an analysis of design rules, a bit of this type can be laid out in an area no smaller than 6 to 8 L^2 where L is the minimum design rule dimension. As discussed by Terman and Heller (Ref. 12) this is less than a factor of 2 better than one-transistor MOS RAMS. In an effort to circumvent these layout limitations, Bower, et. al. (Ref.13) have developed an offset mask technique in which mis-registration is employed in order to eliminate a design rule requirement in the data transfer direction. The difficulty with this approach is that the CCD bit is now not inherently self-aligned and there can be large fluctuations in the magnitude of the charge handling capacity for small CCD electrodes. Although the CCD bit is less than a factor of two smaller than MOS RAM bits, a conventional memory requires less overhead structure than an MOS random access memory and as a result the actual packing density ratio between an MOS and a CCD memory is approximately 2 or 3 to 1. Even so, at the 64K bit level, the die size becomes too large for volume production and it is desirable to explore new approaches to increasing the packing density of a CCD memory.

B. New Approaches to Chip Organization

(1) The Interlaced Ripple SPS Organization

As has been pointed out originally by Collins, et. al. (Ref. 14) and more recently by Rosenbaum, et. al. (Ref. 6) it is not essential to have two or more electrodes per bit. It is possible to have n-bits

in n+1 electrodes by using a unique n-clock system. The system works by sequentially clocking a set of nominally low electrodes in such a way that the absence of a bit propogates backwards through the register. This is illustrated in Figure 8. Because of the large number of clocks, the "ripple" concept is most easily adapted to the SPS type organization.

In the typical SPS organization there are two series electrodes for each parallel register as shown in Figure 9(A). It is possible to have only one electrode per column if the series register first transfers data to the odd numbered columns and then, on a second scan, transfers data to the even number registers, as in Figure 9(B). This "interlaced" approach in the series registers combined with a ripple architecture in the parallel registers, results in an extremely dense CCD array. The number of electrodes per bit is $\frac{N+1}{N}$. For practical purposes N is usually between 3 and 7. Smaller values of N give little benefit over the traditional 2 electrode per bit organization and larger values of N create very complicated clocking requirements. With an interlaced ripple SPS organization bit densities on the order of 0.3 $mils^2$/bit can be achieved. Moreover, this architecture has the advantage of reducing the influence of leakage current because of the greater area utilization factor as well as of averaging the leakage current because the data does not reside in any one location for a significant period of time. An operating interlaced ripple structure has been reported by Rosenbaum, et. al. (Ref. 6).

(2) Multi-Level Storage

An alternative approach to achieving high-density memory storage is to utilize the analog properties of the CCD shift register which can store a continuum of charge levels. For example, by storing four discrete levels of charge, two bits of information can reside in one physical location. The difficulty with such an approach is that the sense amplifier design is much more difficult. The simple flip-flop which has proven to be so valuable in memory technology will no longer suffice. In addition, margins become tighter and the question of bit error rate must be treated. The possibility of multi-level storage has been considered theoretically, but to date no actual design work has been done. In the future this opportunity for increasing bit density will be explored but probably not for several more years. Alternative architectural approaches can achieve production costs consistent with memory requirements in the near future.

IV. SUMMARY

The rapid progress in CCD technology has taken place largely because of the compatibility of CCD technology with MOS technology. Recent advances in MOS technology are further narrowing the difference between the two technologies. The similarities result in manufacturing techniques and production costs per wafer that are essentially the same. Not only are the manufacturing techniques compatible, but CCD fits well into semiconductor memory systems. Packages, operating voltages, reliability, and system design procedures are the same.

The real issue in CCD digital memory design is that of production cost. On the basis of layout design rules, a CCD cell can be approxi-

mately 50% the area of a one transistor MOS RAM cell. However, this is rarely achieved. Typical numbers are more like 60% to 70%. Lower overhead requirements for CCD memory, further improve memory density. The ratio of RAM memory area to total die area runs between 30% and 40%. CCD digital memory typically is running from 50% to 60%. Interestingly, CCD memory designs to date have been more performance-oriented than cost-oriented, with average latencies under 100 μsec. New designs addressing the cost issue are underway. These designs at the 64K bit level will require less than 30% more area than 16K MOS RAM and can be expected to achieve a bit cost of 1/4 of the cost per RAM bit.

In addition to the geometric considerations, there are yield factors at work which could further lower the CCD cost. The major impact will be in chip design. For large low cost systems, the interlaced, ripple SPS organization offers significant advantages. With this organization, the register size can be greatly increased without increasing the number of transfers between input and output. This allows the elimination of many internal refresh amplifiers. Power is reduced since the internal parallel registers are clocked at a low frequency. Leakage current is averaged over all the bits in a register eliminating the problems associated with non-uniform leakage current. All data moves in synchronism, simplifying the refresh control logic. As a result of the fewer refresh amplifiers and the reduced overhead circuitry, power dissipation for CCD memory can be an order of magnitude lower than comparable MOS RAM designs.

The lower power dissipation is important to designers of large systems. The added bonus is that yield and reliability are also improved. A reduction of 500 mw in power dissipation can mean 40°C lower junction temperature. With leakage current doubling every 8°C to 9°C, this lower power dissipation results in 30 times lower leakage current. The continued reduction in RAM cell size makes it more susceptible to leakage current non-uniformity. The SPS structure provides an averaging which will result in superior high temperature performance. Of course, RAM refresh intervals need not be as long as CCD memory refresh intervals. For example, a 16K RAM organized in 128 rows and 128 columns can be refreshed with 128 clock cycles. An SPS CCD memory with 4K bit registers requires 4K clock cycles to complete its refresh. This gives a poor memory utilization rate if the CCD memory is used in a random access mode. However, when properly compared against moving magnetic storage, the performance of CCD is clearly attractive.

An interlaced, ripple SPS CCD memory is now viable. Such a component would store 65536 bits organized as 16 blocks of 4K words (an alternative possibility is 32 blocks of 2K words) decoded to a single input and output. The 4K word organization is preferred over a 2K word from cost and power considerations. Assuming this organization, 4 addresses are required to decode the 16 blocks to the input and output pins. Thus one block is accessed while the remaining 15 recirculate and refresh in synchronism with the accessed block. In a deselected chip, all 16 blocks are automatically refreshed a bit at a time whenever the memory is clocked.

The mode of a selected chip is controlled by a write pin. Whenever the write mode is selected, the input pin controls the data written into the selected register. In all cases the output of the selected block is read to the output. Output data is latched and remains valid

until reset by the next cycle.

The data rate ranges from below 1 MHz to above 5 MHz (several devices have been designed with data rates up to 10 MHz). The combination of data rate and block size determine average latency. Latency can be improved at the expense of power dissipation and added chip complexity. Average latency ranges from 200 μsec to 500 μsec. Active power dissipation on chip is about 5 μ watts per bit at maximum data rate. Standby power dissipation is less than 1 μ watt per bit.

Power is supplied by a 12 volt supply. TTL compatibility at the output requires a 5 volt supply. Substrate bias of -5 volts is used. In keeping with the philosophy of economy of cost and power, most designs require high level clocks. Two clocks at the data rate drive the high speed series registers. The remaining clocks will be low frequency clocks either driving the transfer gates or the parallel registers. Most designs buffer the clocks to the parallel registers. The transfer clocks are low duty cycle clocks occurring approximately every 32 cycles of the data clocks. All other pins, including addresses, chip enable, data in, data out, and write, are TTL compatible. The device can be packaged in a 16 pin DIP. Table 1 lists the device features:

TABLE 1. POSSIBLE FEATURES OF A BLOCK STORAGE 64K CCD DIGITAL MEMORY

o Organization	16 blocks of 4K bits decoded to a single Input and a Single Output
o Data Rate	1 MHz to 5MHz
o Average Latency	500 μsec @ 4 MHz data rate
o Refresh	All 16 blocks move in synchronism for simultaneous refresh
o Power Dissipation	Active @ 4 MHz 5 μwatt/bit Standby @ 1 MHz < 1 μwatt/bit
o Power Supplies	+12v Ground + 5v -5v
o High Level Clocks	$\emptyset_1$, $\emptyset_2$ non-overlapping clocks at the data rate 0-12v 100pF each $\emptyset T_1$, $\emptyset T_2$ low duty cycle clocks at 1/32 data rate 0-12v 50pF each
o TTL Compatible	Write, Data in, Data out, A_0-A_3, Chip Select
o 16 Pin Package	

The past year has witnessed the emergence in production of CCD digital memory components as part of the CCD family. These components have been fast access memories and shift registers offering performance advantages not usually associated with CCD memory and not necessarily consistent with minimum cost. The year has also seen the movement of mass produced MOS RAM technology to the split gate double poly process used by CCD. Together these events have made clear that the time is right for CCD digital memory to address the low cost block store memory sector of the performance range.

In conclusion, future high density CCD memory components will employ a simple buried channel process. They will incorporate an interlaced ripple SPS architecture and will utilize advanced circuit design techniques for charge sensing and internal clock generation. They will cost approximately 1/4th the price of an MOS RAM and will operate in commercial environments up to 70°C. However, system designers will discover that significant performance advantages will accrue if CCD system operating temperatures are decreased.

The question no longer is whether CCD will be useful in digital memory applications; it is how soon will CCD be designed-in and how large will be the volume of units shipped. As a prediction, by 1980 there will be more CCD memory bits shipped per year than any other semiconductor memory technology and the price per bit will be under 10 millicents. Already the price per bit for CCD memory components is less than other semiconductor technologies. With the continued advancement of CCD memory design knowledge the costs will decrease manyfold and will initiate a new era of semiconductor pervasiveness through all memory system architecture.

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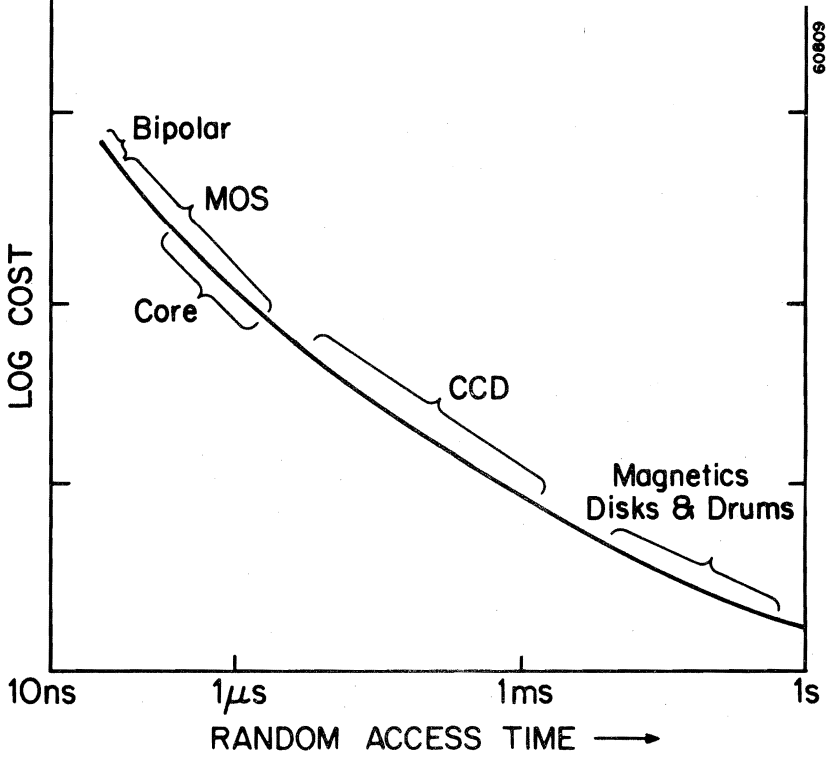

FIG. 1 - Memory Gap in the
Cost/Performance Curve

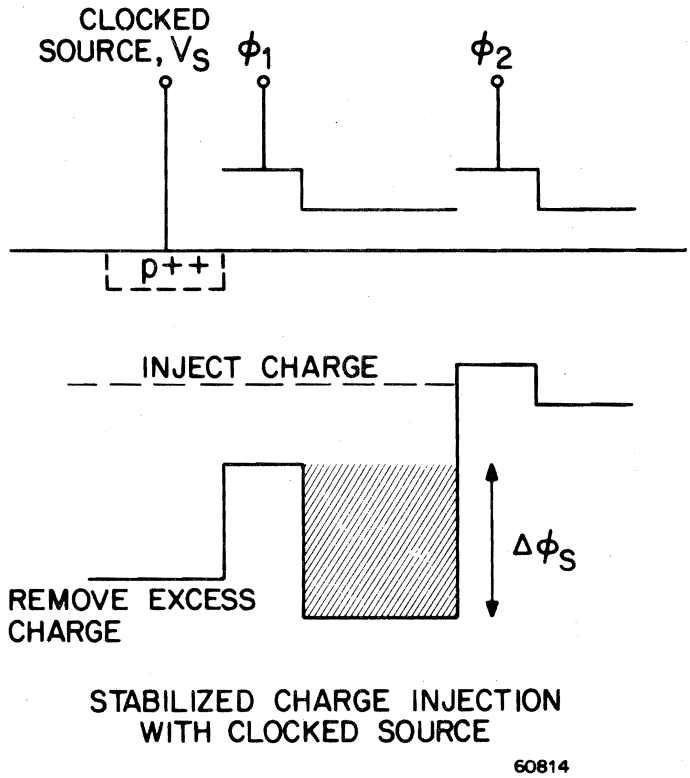

FIG. 2 - CHARGE WRITING TECHNIQUES

FIG. 2(A)- Clocked Input
Diffusion

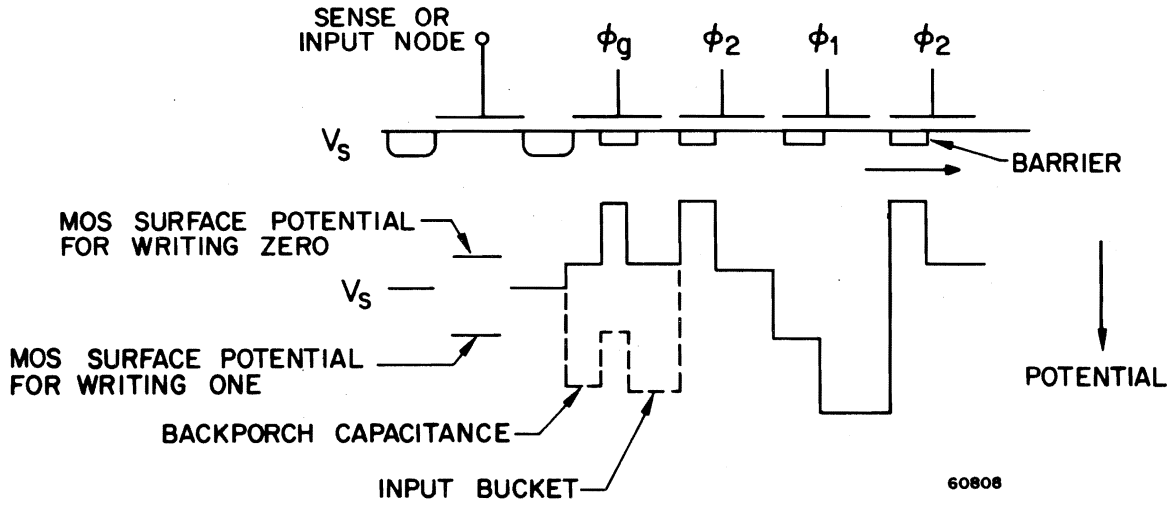

FIG. 2 -CHARGE WRITING TECHNIQUES

FIG. 2(B)-Clocked Layout Gate

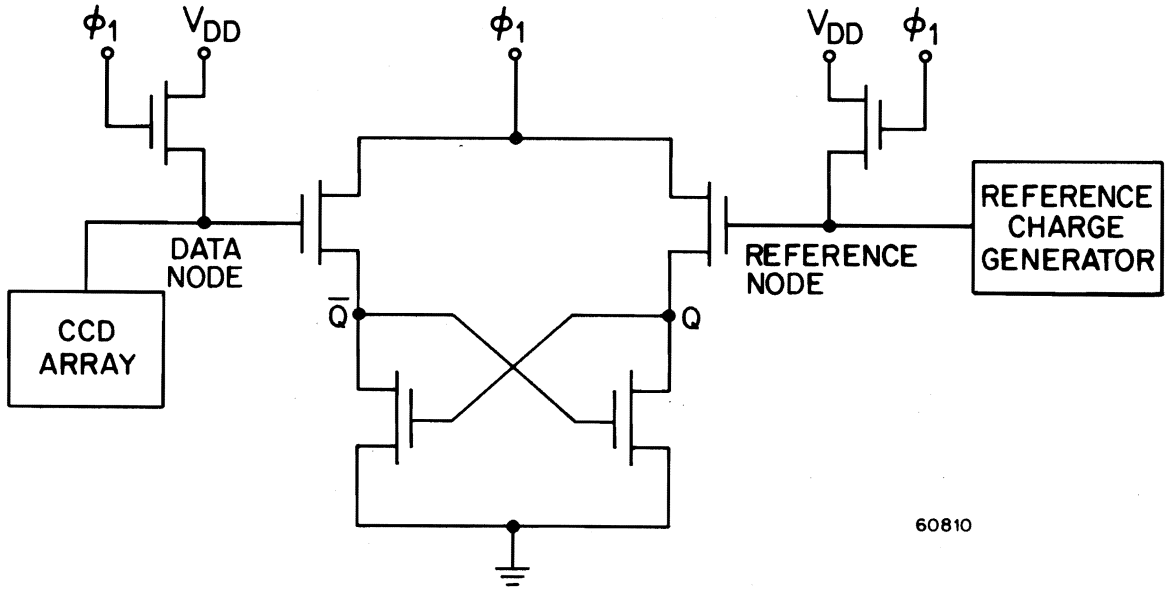

FIG. 3-CCD DIGITAL SENSE
AMPLIFIER DESIGNS

FIG. 3(A)- Sense amplifier with
dummy reference charge generator

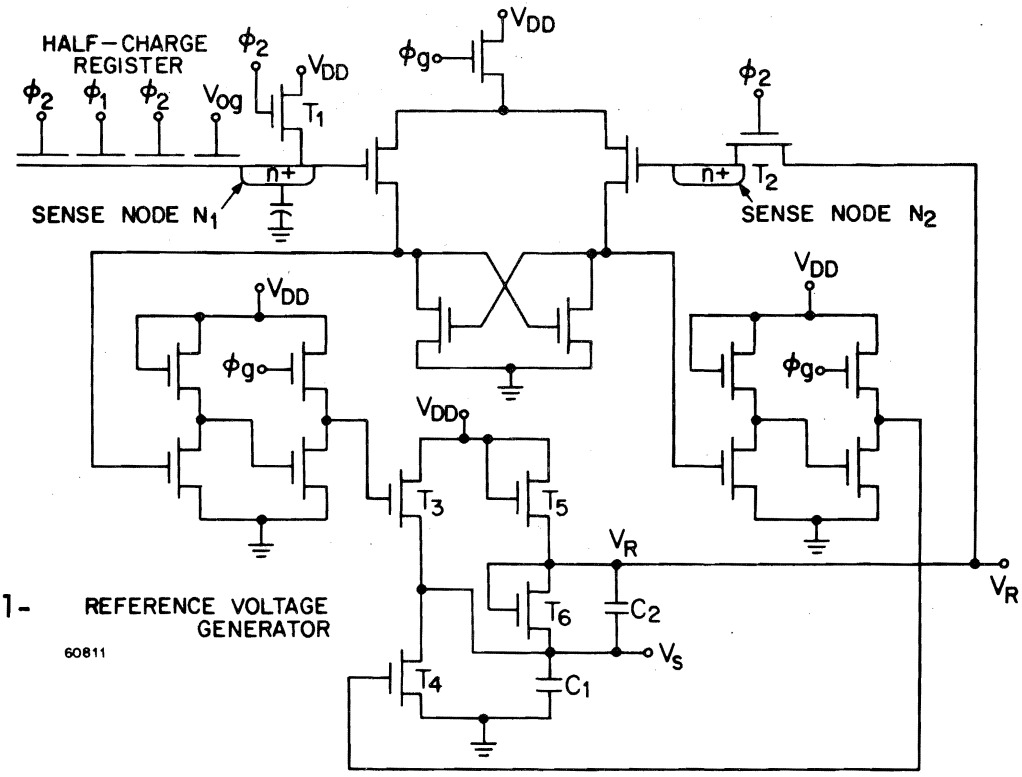

FIG. 3(B)1- REFERENCE VOLTAGE GENERATOR

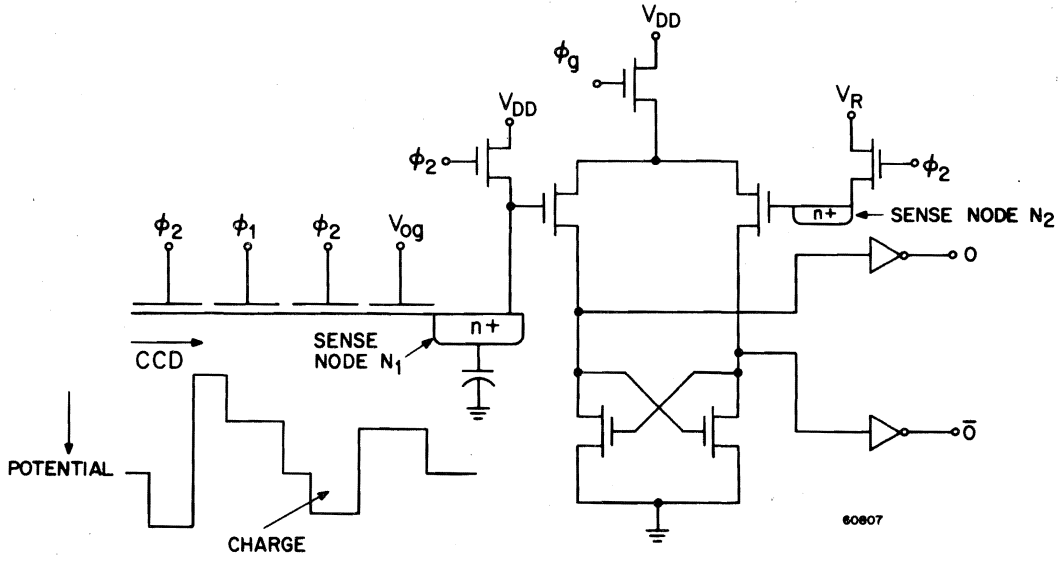

FIG. 3(B)2- Sense Amplifier with Reference Voltage Generator

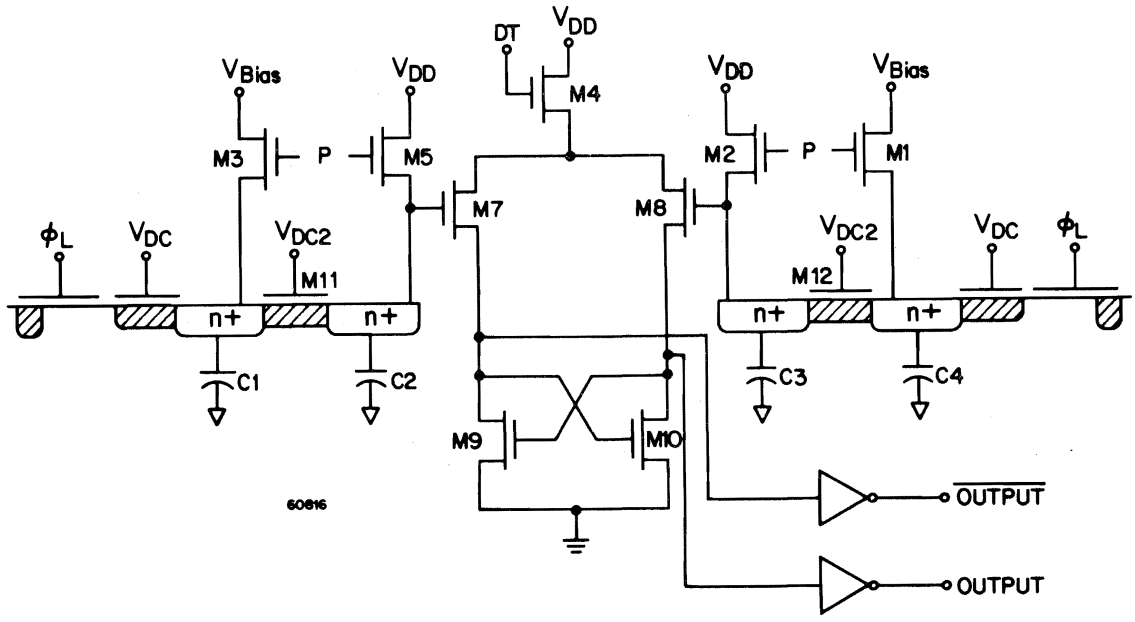

FIG. 3(C) - Symmetric Sense amplifier in which either side can act as dummy register

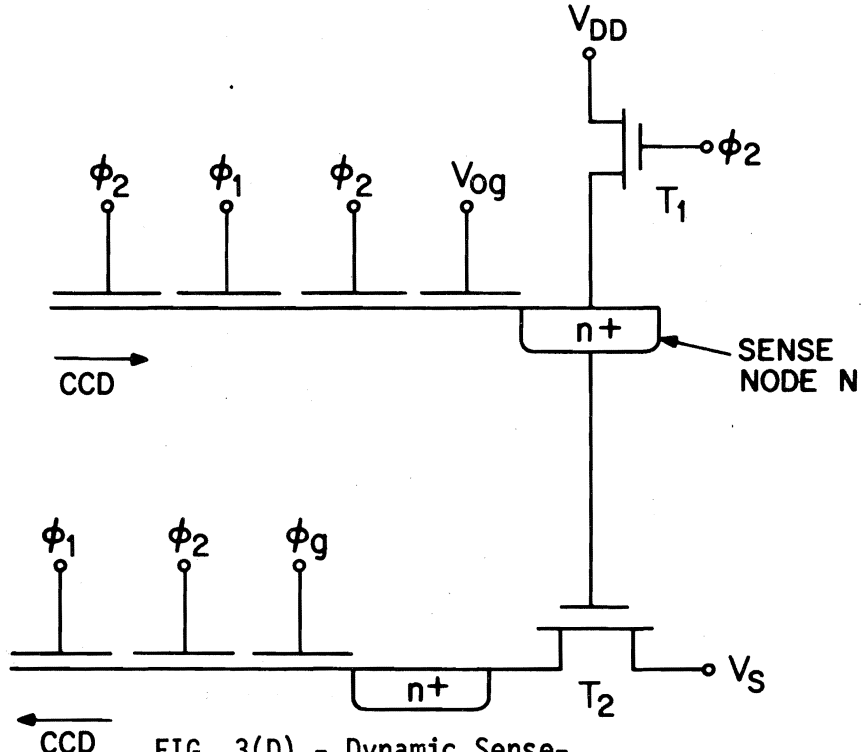

FIG. 3(D) - Dynamic Sense-Refresh amplifier ("Turn-around cell").

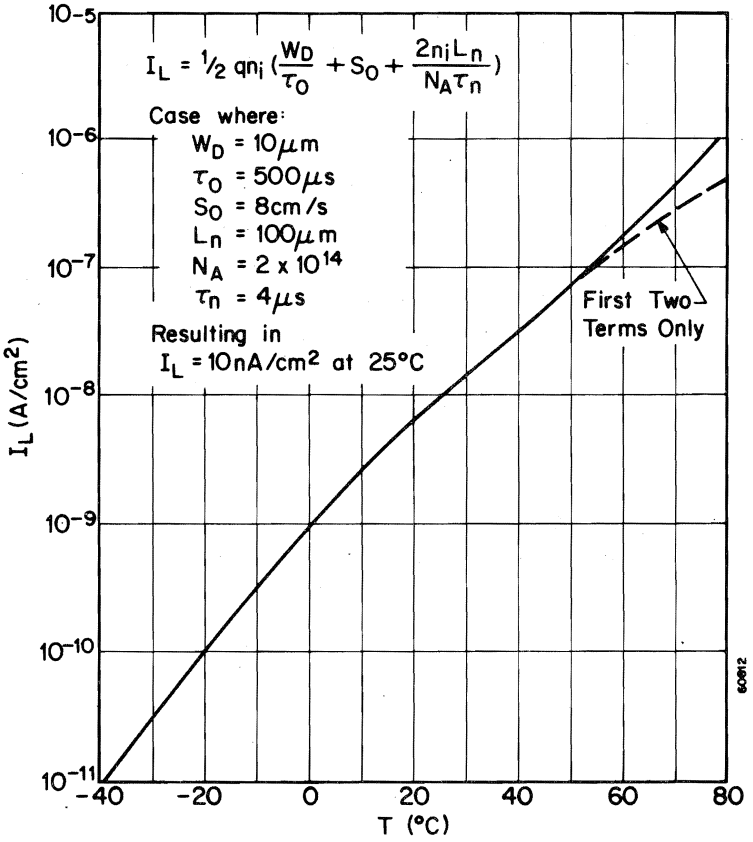

FIG. 4 - LEAKAGE CURRENT VS. TEMPERATURE

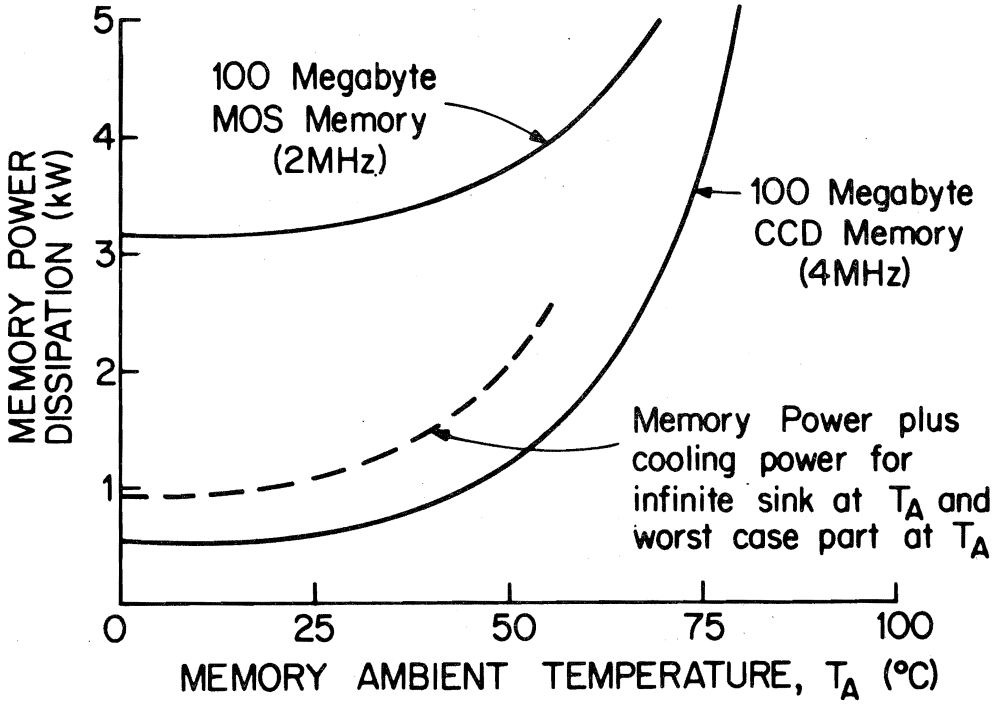

FIG. 5 - SYSTEM POWER DISSIPATION VS AMBIENT TEMPERATURE

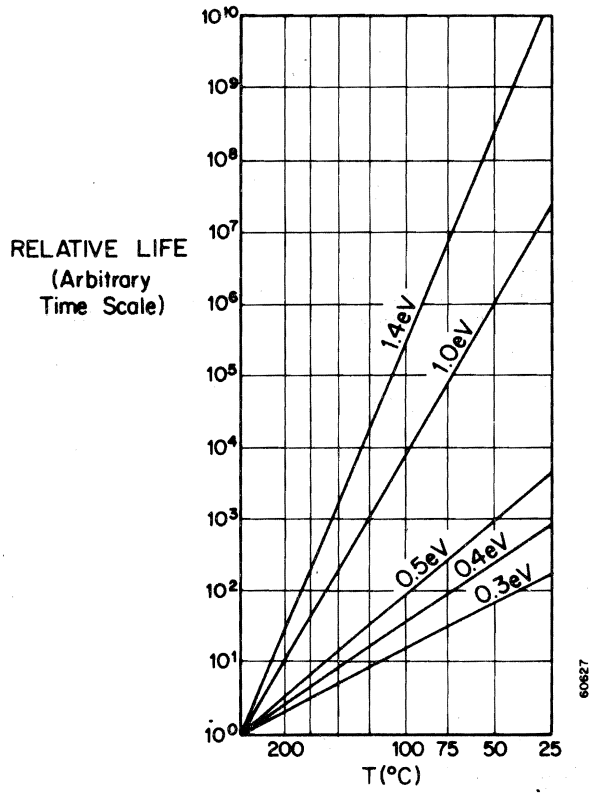

FIG. 6 - ARRHENIUS PLOT

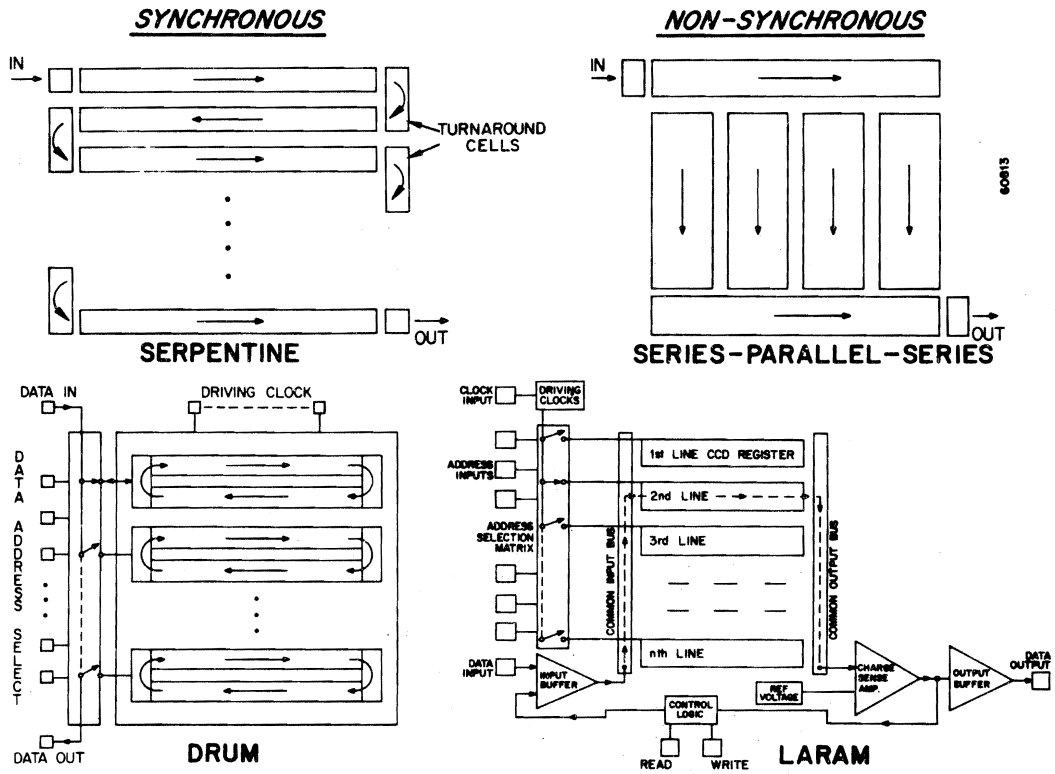

FIG. 7 - CCD MEMORY ORGANIZATION

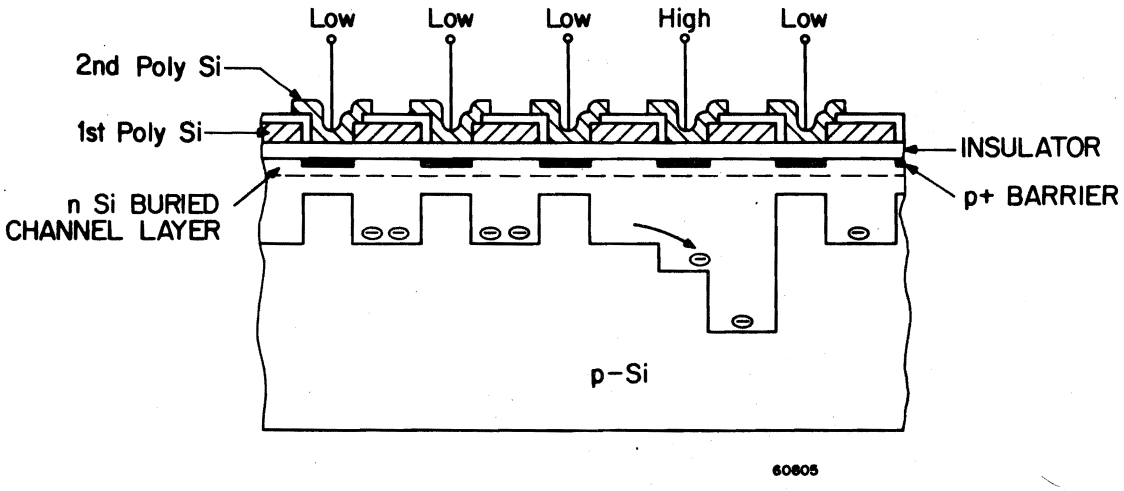

FIG. 8 CROSS-SECTION OF CCD
"RIPPLE" SHIFT REGISTER

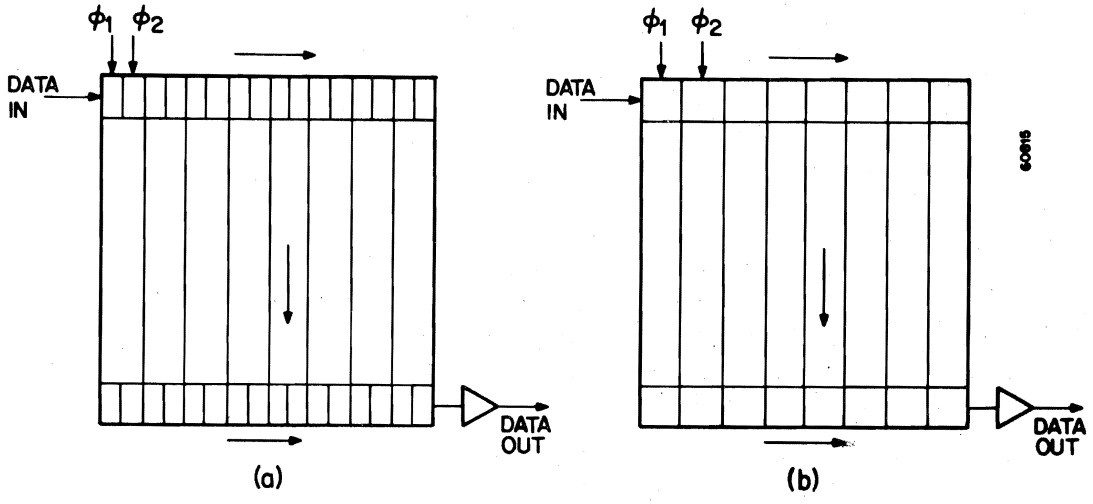

FIG. 9 SCHEMATIC DIAGRAM OF
THE SPS STRUCTURES FOR
TWO-PHASE CCD's.
(a) Standard (b) Interlaced