SIMULATION FOR DEVICE DESIGN OF SHORT GATE CHARGE-COUPLED DEVICES: A COMPLETE CCD SHIFT REGISTER COMPUTER MODEL

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ABSTRACT

A computer model has been developed that simulates charge transport of carriers in a surface channel charge-coupled device. This model is based on the charge continuity and current transport equations with a time dependent surface field.

The model can be employed to analyze charge transport in CCD short gate shift registers. In addition it can be used to analyze the linearity and transfer characteristics of any type of CCD input scheme. Further, the model can be employed to investigate the performance in terms of transfer characteristics and linearity of the output circuitry of the CCD shift register. Essentially the present model simulates a complete CCD shift register.

I. INTRODUCTION

Since the introduction of the charge coupled device (ref. 1) considerable theoretical and experimental work has been carried out. The CCD has been shown to be useful in optical imaging arrays, signal processing and memory applications (ref. 2-7). The charge transfer efficiency, the characteristics of the input and output structures of CCDs are important in all these applications.

In this work a computer model that simulates the two-dimensional dynamics of electrons and holes for practical CCD structures with a source diffusion has been developed. In this model the charge is electrically injected from the source diffusion. The analysis is based on solving the transport equation with the actual time-dependent surface field for a practical CCD structure with the appropriate boundary conditions. Both the self-induced and fringing field terms are included in the formulation.

The model presented in this paper is expected to be useful for the analysis of any input stage of surface channel CCDs, CCD shift register charge transfer dynamics and analysis of any output CCD shift register stage. Particularly it can be used to study the low-level signal charge injection and the linearity of electrical charge injection into surface channel CCDs. The formulation and explanation of the computer model for the charge injection and charge transfer in surface channel CCDs including the input diffusion is given in Section II.

To demonstrate some of the capabilities of the model the linearity of electrical charge injection into surface channel charge-coupled devices has been studied. The input characteristic of the diode cutoff injection method and the generated harmonic components of a sinusoidal input signal are given in Section III. The comparative results of other input schemes obtained using the model, will be described at the conference.

For charge transport analysis in CCD shift registers, our model was used to study the surface charge transfer process for short gate CCDs using an actual charge profile which was electrically injected from the source diffusion. A fundamental investigation of the relative significance of the self-induced, fringing field and the diffusion currents in the charge transfer process was then carried out. An explanation of the effect of

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signal-charge level on the speed of the charge transfer for short gate devices is given in Section IV. Conclusions are presented in Section V.

II. MATHEMATICAL MODEL

The mathematical formulation for the computer model is based on the general form of a CCD structure which includes a source diffusion, an input gate and subsequent transfer gates as shown in Fig. 1(a). Signal charge can be injected and transferred by the application of the pulse sequence illustrated in Fig. 1(b). In order to treat the transient behaviour of minority carriers in the n-channel CCD, Poisson's equation and the continuity equation have been solved simultaneously by numerical computation. The method of solution presented is different from the treatment given in (ref. 11-12) since our model includes the input stage.

The analysis is based on the accurate numerical solution of the time dependent transport equation
with the time dependent surface field. Both the self-induced and fringing field terms were included in the formulation. The minority carriers, $n^*(x^*, t^*)$, (an asterisk is used to represent unnormalized quantities), are injected from the source diffusion and flow along the silicon surface within a channel of infinitesimal thickness. The transport equations governing the dynamics of minority carriers in the x^* direction are

$$q \frac{\partial n^*}{\partial t^*} = \frac{\partial J^*}{\partial x^*} \quad , \tag{1}$$

$$J^*(x^*,t^*) = q \mu^* \left[\frac{kT}{q} \frac{\partial n^*}{\partial x^*} + n^* E^*\right], \text{ and} \tag{2}$$

$$\mu^* = \frac{\mu_o^*}{[1 + (E^*/E_c^*)^2]^{1/2}} \quad ,$$

where J^* is the current density per unit area perpendicular to the direction of the carrier flow, μ_o^* is the low electric field mobility at the silicon surface, E_c^* is the critical electric field (ref. 13), k is Boltzman's constant, T the absolute temperature and q is the magnitude of the electronic charge.

At the surface, the tangential electric field $E^*(x^*,t^*)$, is determined by solving the two-dimensional boundary value problem defined by the equations

$$\nabla^2 \phi^* = 0; \quad y^* \leq 0 \quad , \tag{3}$$

$$\nabla^2 \phi^* = \frac{-q}{\varepsilon_{si}^*} [p^* - n^* + N^*]; \quad y^* \geq 0 \text{ , and} \tag{4}$$

$$E^*(x^*,t^*) = -(\partial \phi^*/\partial x^*)\Big|_{y^* = 0} \tag{5}$$

where $\phi^*(x^*,y^*,t^*)$ is the potential at time t^*, $n^*(x^*,y^*)$ and $p^*(x^*,y^*)$ are the electron and hole densities, $N^*(x^* y^*) = (N_D^* - N_A^*)$ is the net concentration of the ionized impurity atoms, and ε_{si}^* is the dielectric permittivity of silicon.

Equations (1) to (5) can be normalized by defining the following parameters:

$$L_D = [(\varepsilon^*_{si}\ kT)/(q^2\ n_i)]^{1/2} ;\quad x = x^*/L_D ;\ y = y^*/L_D ;$$

$$\psi = \frac{\phi^*}{kT/q} ;\quad n = n^*/n_i^* ;\quad p = p^*/n_i^* ,\quad N = N^*/n_i^* ;$$

and

$$\tau = \left(\frac{\mu^* kT}{L_D^2\ q}\right) t^*$$

where n_i^* is the intrinsic carrier concentration.
The normalized equations become

$$\frac{\partial n}{\partial \tau} = \frac{\partial J}{\partial x} , \tag{6}$$

$$J = \mu\left(\frac{\partial n}{\partial x} - n\frac{\partial \phi}{\partial x}\right) , \tag{7}$$

$$\nabla^2\psi = 0 \quad ; \quad y \leq 0 , \tag{8}$$

$$\nabla^2\psi = (n - p - N) \ ; \ y \geq 0 \tag{9}$$

In the solution of equation (9) we have neglected the bulk minority carriers, and have assumed that the majority carriers in the N^+ source diffusion and the substrate are in thermal equilibrium at all times under pulse voltage operation (ref 14). At the silicon surface the minority carrier concentration $n(x,\tau)$ can be expressed in the form

$$n = \Phi_n \exp(\psi),$$

where $\Phi_n(x,\tau) = \exp(-\phi_n(x,\tau))$ and $\phi_n(x,\tau)$ is the electron quasi-Fermi level at the silicon surface.

Initial and boundary conditions are defined by

(i) Along AB, wherethe behavior is approximately one-dimensional, we have $\partial\psi/\partial x = 0$.
(ii) Along EF, we assume an infinite barrier, i.e. $\partial\psi/\partial x = 0$, $J(x,\tau) = 0$.
(iii) At the source contact, we assume that the semiconductor is in thermodynamic equilibrium (the usual assumption for ideal ohmic contacts). Given the applied voltage V_s, we can then find the boundary value of ψ and Φ_n at the contact.
(iv) At the gate electrodes $\psi = V_{electrode}$.
(v) At the silicon-oxide boundary.

$$\psi(x,0-) = \psi(x,0+)$$

$$\partial\psi(x,0-)/\partial x = \partial\psi(x,0+)/\partial x$$

To obtain the complete solution equations (6) through (9) with the above boundary conditions have been solved numerically.

III. ANALYSIS OF THE INPUT STAGE

As an example our CCD model was used to analyse the nonlinearities of the input of the device structure shown in Fig. 1(a). The length of the gates used was 8 μm. The substrate was p-type silicon doped uniformly with an acceptor density of 8×10^{15} cm^{-3}. The source diffusion was assumed uniformly doped n-type with a donor density of 10^{18} cm^{-3}. The oxide thickness was 1100Å, gap size between electrodes was 1 μm and the overlapping region between the input gate and the source diffusion was 0.5 μm. The

low field surface mobility was assumed to be 450 cm^2/v-sec.

Using the model presented in Section II the charge was injected from the **source** diffusion into the device. The voltage input method (ref 3) sometimes referred to as the "diode cutoff method" was used with the pulse sequence as that shown in Fig. 1(b). A clock frequency of 1 MHz with fall time of 40ns was used. The sampling pulse frequency applied to the input gate was assumed to be equal to one half of the clock frequency, with a fall time of 20ns.

To obtain the input characteristics (the transfer function), the input diode is held at a constant d.c. bias with respect to the substrate, and the input gate is pulsed to perform a sampling function. During the time the storage gate (2nd gate of fig. 1(a) is turned on and held at $(V_R + V_p)$ the input gate is pulsed on to a value $V_I = (V_R + V_p)$; charge then flows into the well under the storage gate. The charge is injected from the input diffusion until the surface potential under the input and storage gates is reset to the level of the input diode. The charge under the input and storage gates is then calculated. The analytic expression reported in (ref. 15) has been used to calculate the surface charge density per unit area under the storage gate from the computed surface volume concentration of the injected signal charge. The input gate is then turned off to V_R, thus isolating the charge packet under the storage gate from the input diode. Since the input gate does not act as an "infinitely sharp knife" in cutting off the charge packet, the charge residing underneath the input gate is then distributed between the input diode and the storage gate. The fraction of the charge under the input gate which spills forward increases as the input diode potential is increased. This fraction increases from zero to 45 percent as the diode potential is increased from zero to 14V. After turning off the input gate the total charge under the storage gate which represents the charge packet is then calculated. Figure 2 shows the total charge under the storage gate as a function of the diode potential. This curve represents the input characteristic of the diode cutoff method.

The nonlinearity shown in the input characteristic is due to two factors; i) nonlinearity is introduced due to the depletion capacitance which changes with the diode potential. The interface potential under the storage gate held at potential $(V_R + V_p)$ is therefore related in a nonlinear manner to the signal charge per unit area under gate (ref 1). ii) the partitioning of the charge underthe input gate between the input diode and the storage gate results in increased nonlinearity, it becomes more significant as the ratio of the input gate area to the storage gate area increases.

A sinusoidal signal was applied to the input diode and the generated harmonic components of the resultant signal were then calculated. The input characteristic curve shown in Fig. 2 was used in conjunction with the fast Fourier transform (FFT) algorithm (ref 16) to calculate the generated harmonic components. The generation of higher harmonics depends on the amplitude and the d.c. bias of the input signal. The peak to peak amplitude of the input signal was set to one half the input range, which was 12V as derived from the input characteristic curve. The d.c. bias of the input signal was then varied to cover the full input range. The fundamental (f_1), the second harmonic (f_2) and the third harmonic (f_3) components are shown in Fig. 3. The calculated harmonic components were normalized to the maximum of the fundamental components. The second harmonic component of the signal can be made to be less than 10% by proper choice of the biasing conditions which are determined by the CCD model used in this section. As shown in Fig. 3 the generation of higher harmonics depends strongly on the d.c. bias level of the input signal. At

both extremes the signal experiences saturation or clipping with a steep increase of the generated harmonic components.

Beside the diode cutoff injection method which was used and analyzed in this section, there are two other injection methods, namely; dynamic injection and potential equilibriation. Our CCD model which includes the input diffusion can be easily used for a comparative study of the input characteristics and harmonic distortions of these injection methods with different device geometries and pulse sequences. Such studies will be presented at the conference.

IV. USE OF THE MODEL FOR CHARGE TRANSFER INEFFICIENCY ANALYSIS

To further examine the effect of the fringing field in short gate CCDs, we investigated the relative importance of the different components of the surface current and their contribution towards the charge transfer. The total surface field $E(x,\tau)$ can be expressed by the sum of two terms, E_f the fringing field and E_s the self-induced field (ref. 10)

$$E(x,\tau) = E_f(x,\tau) + E_s(x,\tau) \tag{10}$$

A one-dimensional linear approximation between the surface potential and the surface charge density has been widely assumed(ref. 8-9). Using this approximation the self-induced field can be written in the form

$$E_s(x,\tau) = \alpha \frac{\partial Q(x,\tau)}{\partial x} \quad , \tag{11}$$

where α is a constant and is given by

$$\alpha = \left(\frac{n_i^* L_D}{kT/q} \right) \alpha^* \quad ,$$

and

$$\alpha^* = \frac{q(\phi_{so}^* - \phi_{ss}^*)}{C_o^*(V_G^* - V_{TH}^*)} \quad , \tag{12}$$

$Q(x,\tau)$ is the surface charge density, ϕ_{ss}^* is the equilibrium surface potential, ϕ_{so}^* is the surface potential in deep depletion, C_o^* is the oxide capacitance per unit area, V_G^* is the gate voltage, and the threshold voltage V_{TH}^* can be defined by

$$V_{TH}^* = 2\phi_p^* + \frac{[2q\epsilon_{si}^* N_A^*(2\phi_p^*)]^{1/2}}{C_o^*} \quad , \tag{13}$$

where ϕ_p^* is the Fermi potential of the substrate.

From the computed total surface field and the surface charge density during the charge transfer process, and using equations (10) through (13) we can calculate the self-induced and the fringing field terms. The total surface current and its components are then calculated. As an illustrative example, Fig. 4 shows the spatial variations of the total current and its components at two different times under the storage and transfer gates for 4 μm gate lengths. The calculated diffusion current at different stages of the charge transfer process was found to be insignificant. The spatial variations of the self-induced current I_s, the fringing field current I_F, and the total current I at the beginning of the charge transfer process

(t = 0.01ns) is shown in Fig. 4(a). At the beginning of the charge transfer the effect of the self-induced field is pronounced under the storage gate. However near the gap between the two transfer gates, the drift current caused by the fringing field is the dominant current. Variations of the surface current components at t = 0.1ns, where 30% of the charge is still left behind is shown in Fig. 4(b). The effect of the self-induced field seems to be weakened under the storage gate. Near the gap the self-induced field causes a drift-current which opposes the current due to the fringing field. Figure 5 shows the time-dependent charging current of the transfer gate calculated at the left edge of the transfer gate. From Fig. 4 and Fig. 5 it can be seen that, during the intermediate and final stages of the charge transfer process, the charge transfer is controlled by the self-induced current and the fringing field current near the gap between the transfer gates. For 6 μm and 8 μm a similar spatial current distribution with a lower fringing field effect was obtained.

From the investigation of the relative significance of the current components in the charge transfer process for short-gate devices we can conclude that (i) the diffusion current can be neglected during the different stages of the charge transfer, (ii) the fringing field is actually responsible for most of the charge transfer and not for the last few per cent of the charge as has been assumed in the literature, (iii) the self-induced field enhances the transfer at the beginning of the charge transfer process, however, during the intermediate and final stages of the charge transfer the self-induced field opposes the fringing field near the gap between the transfer gates, (iv) by decreasing the signal-charge level the fringing field becomes larger and the self-induced field becomes smaller; hence the transfer speed increases with decreasing signal-charge levels for short-gate devices. However, for long-gate devices, where the fringing field is less effective, the diffusion current component is responsible for the transfer of the last few per cent of the signal charge. In such cases the transfer process can be considered to be the same as the charge transfer process in the one-dimensional model and the transfer speed increases with increasing signal-charge level as has been concluded by other authors (ref. 8-10).

The charge transfer inefficiency is defined as the ratio of the charge left behind under the storage gate to the initial charge under the same gate at the beginning of the charge transfer process. Then the charge transfer inefficiency can be written as

$$\frac{Q}{Q_s} = \frac{\int_0^L Q_s(x,\tau)dx}{\int_0^L Q_s(x,0)dx} \quad , \tag{14}$$

where L is the length of the storage gate.

Transfer characteristics for three different gate lengths with a full charge packet Q_o and a fraction of charge packet 0.4 Q_o under the storage gate are shown in Fig. 6. As was to be expected from the above discussion the transfer speed increases as the gate length is decreased. For 4 μm gate lengths the speed increases with decreasing signal level. From this diagram we can see that for 8 μm gate lengths and signal charge of 0.4 Q_o, the charge transfer efficiency for the time period less than 10ns is degraded relative to that for a signal charge of Q_o. Since for short gate devices the charge transfer efficiency improves as the signal charge

is reduced, then it is expected that a fat zero would degrate the charge transfer efficiency in short gate devices.

V. CONCLUSIONS

The mathematical formulation of a computer model has been outlined. The present model which can handle the input and output stages of CCD shift registers provides a tool for the designers to investigate the different methods of charge injection and the linearity of electrical charge injection into surface channel CCDs. As an example, in this paper the model has been used to study the input characteristic of the diode cutoff injection method and the generated harmonic components of a sinusoidal input signal.

Further this model has been used for charge transfer studies in short gate CCDs. The effect of the device gate lengths and the signal-charge level on the charge transfer process has been investigated. For short gate devices ($L \leq 8$ μm) it was found that the diffusion current can be neglected during the different stages of charge transfer. The transfer efficiency is governed mainly by the fringing field and self-induced current mechanism. The self-induced field enhances the transfer at the beginning of the transfer process; however, the fringing field is the dominant component during the intermediate and final stages of the charge transfer. Our results help to clarify the mechanisms by which the signal-charge level and gate length affect the charge transfer efficiency.

VI. REFERENCES

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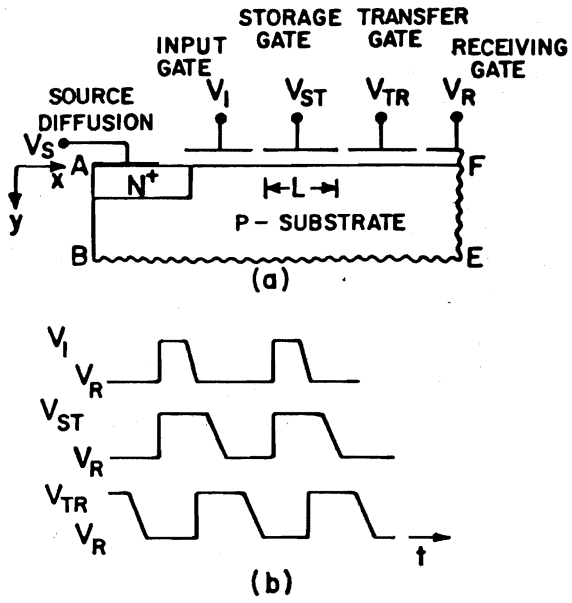

Fig. 1

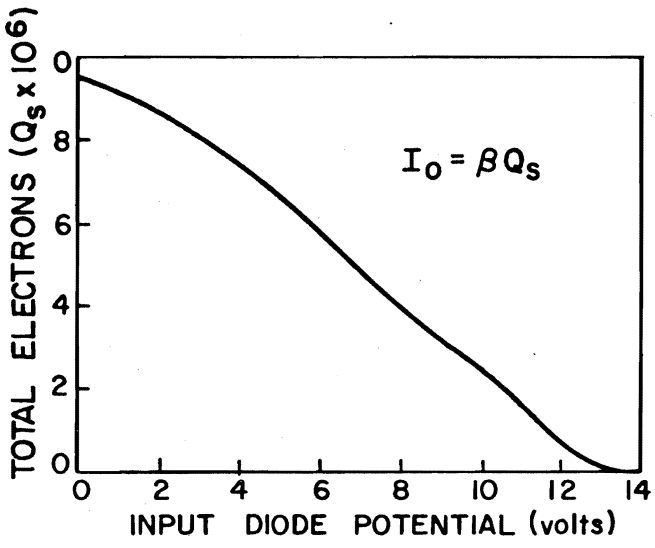

Fig. 2

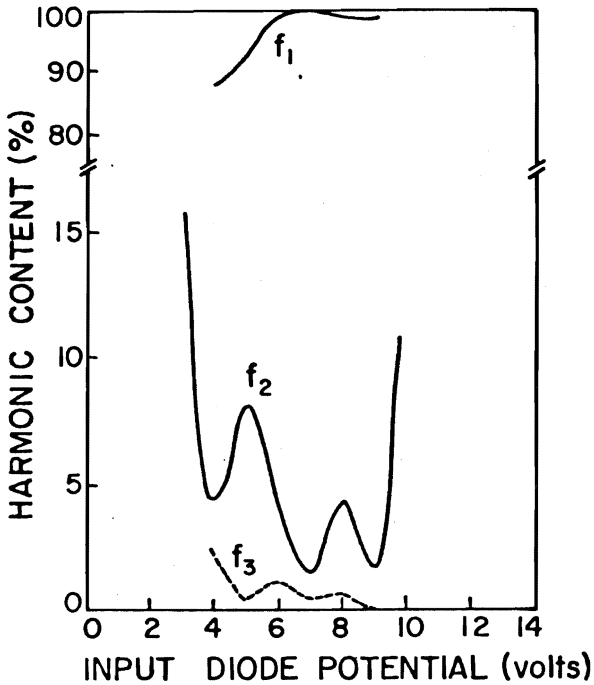

Fig. 3

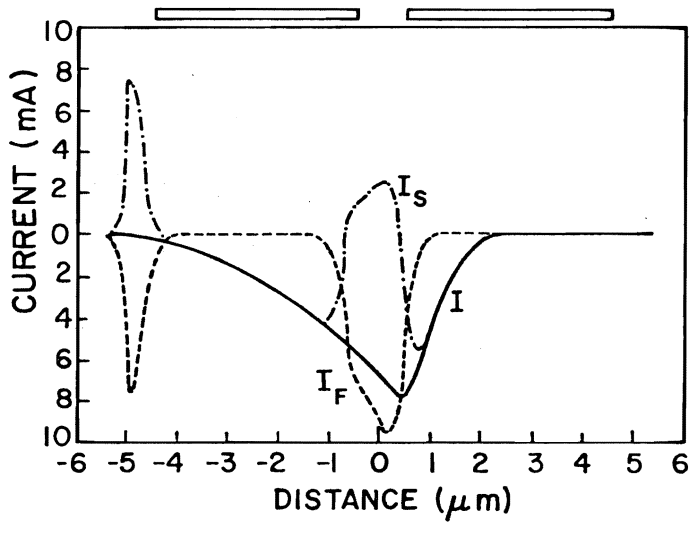

Fig. 4

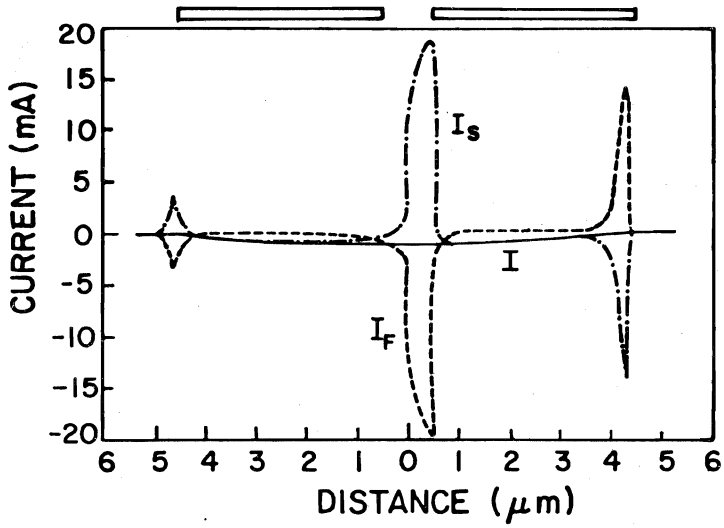

Fig 4(b)

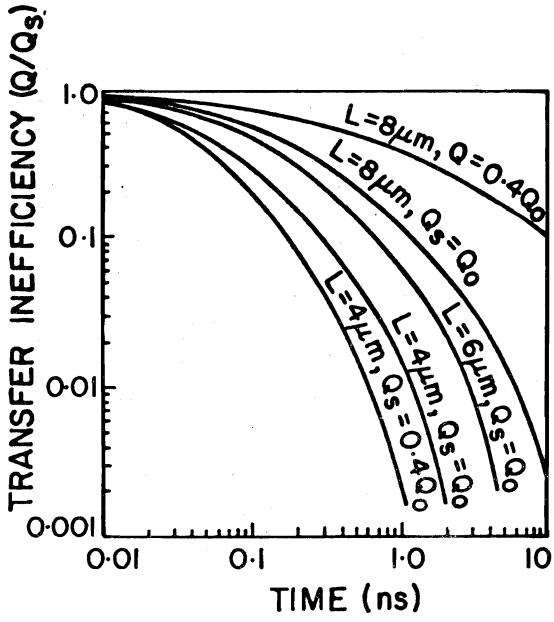

Fig. 6

Note change for pocket size different transfer efficiency

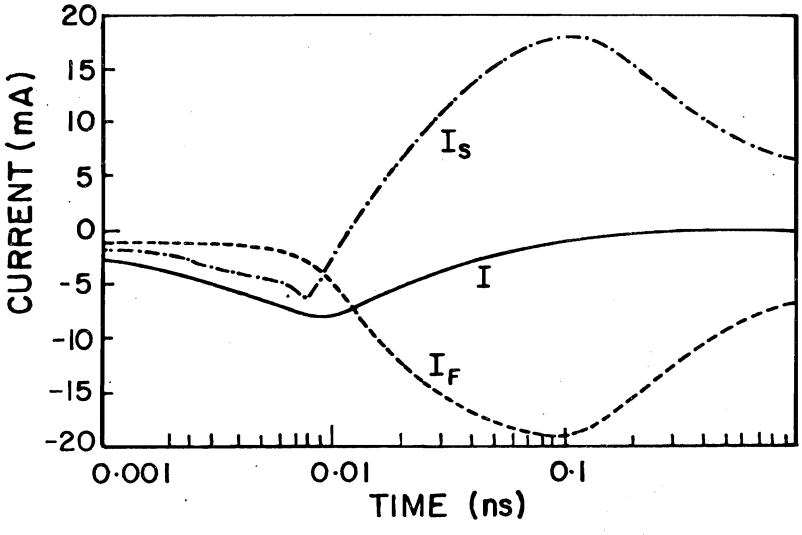

Fig. 5