TRANSVERSAL FILTERING USING CHARGE-COUPLED DEVICES

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ABSTRACT

To perform transversal filtering with a charge-coupled device (ccd), it is necessary to non-destructively tap the analogue signal as it transverses the shift register.

The biased-gate tapping technique requires that one set of clocking electrodes be charged to a dc potential. When charge is clocked under this electrode, the surface, and hence electrode potential, alters, and remains at the new value until the charge is removed. The potential changes may be sensed by a mos transistor operating as a small signal amplifier.

This method of tapping has been successfully used to perform the autocorrelation of both an eight chip uniform pulse train and a thirteen-chip Barker coded p-n sequence.

In order to make full use of the potential bandwidth of ccd's, it is proposed to operate the shift registers in parallel, sampling the input on each of the clock phases. This technique yields a factor of three improvement in data rate for a three phase device, and in many applications, may eliminate sample-hold circuitry.

INTRODUCTION

The ability of the ccd to satisfy many signal processing applications is dependent on achieving an effective technique for non-destructively sensing the signal as it is clocked down the register. Several solutions have been proposed (ref 1, 2, 3), with varying degrees of flexibility and complexity; the split gate technique (ref 1) has been successfully applied to the fabrication of high performance matched filters.

The technique outlined in this paper offers the possibility of programming the filter impulse response, thus allowing the fabrication of programmable matched filters and related devices in ccd technology. The ultimate acceptance of this type of device, and many others, by system designers, relies on the ability of the device designer to understand and solve practical problems, such as the linearity of the device transfer function and minimisation of the off-chip peripheral circuitry. Some of these aspects of device operation will be considered in this paper.

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BIASED-GATE TAPPING

The biased-gate tapping technique, (ref 3, 4), requires that one set of clock electrodes be charged to a direct-voltage potential, the other clock or clocks being allowed to swing about this potential so that charge may be transferred to and from the depletion well below the biased electrode, (fig 1a, b). When a signal charge is introduced into the well, the potential on the gate electrode will alter in order to maintain charge equilibrium in the semiconductor. Removing this charge causes the gate potential to revert to its original value. The potential changes on the gate may be sensed by simply extending it to form the gate of a mos transistor.

Owing to the clock voltages swinging about the biased-gate potential, the effective clock voltage swing is the difference between the peak clock voltage and the potential of the biased gate. The consequence of this reduced effective clock voltage is a reduction in the device transfer efficiency and charge handling capability compared with that obtained when all gates are clocked to the peak voltage. The reduced efficiency may be overcome, if necessary, by increasing the clock voltages. Should the efficiency be acceptable, the reduced charge handling capability and thus dynamic range may be partially overcome by increasing the area of the biased electrode; the maximum charge handling capability, Q_{max}, being given by:

$Q_{max} \propto \frac{A_b \times A_c}{A_b + A_c}$, where A_b is the area of the biased gate and A_c that of the clocked gate. Alternatively, the channel width may be increased.

The response of the biased gate to signal charge may be determined approximately using the circuit of fig 2b, and assuming the depletion capacitance per unit area, C_d, to remain sensibly constant with varying signal charge. The gate voltage change, V_s, due to signal charge per unit area, Q_s may then be expressed as:

$V_s \doteq Q_s A/C_g$ for $C_g \gg C_d A$ and $C_d \ll C_{ox}$, where A is the gate electrode area, C_{ox} the oxide capacitance per unit area and C_g the total capacitive loading applied external to the ccd channel.

This equation is plotted for various values of the sensing transistor gate capacitance in fig 2a, together with the exact solutions obtained using the equations of Boyle and Smith (ref 5). Under practical conditions, with substrate bias or clock offset voltage applied and operating the device with partially filled wells, the signal excursions would be kept to the near linear region of the curves shown. In order to satisfy many applications requirements, an improved linearity must be obtained and a technique is under development to linearise the overall device transfer function.

RESULTS

The tapping technique was tested using a three phase, single level metallisation, 8 bit, ccd shift register, fabricated on 50 Ω.cm, <100> orientation, n-type silicon with an oxide thickness of 1500Å. The clock electrodes were 12 μm long with 3 μm gaps in the channel direction and 300 μm wide. The impulse response and autocorrelation function for this device are shown in fig 1c.

A 14 bit device has been designed along similar lines to the above, except that all the second phase electrodes were extended to form the gates of tapping most's. Both the source and drain of the tapping device were taken to a bonding pad for ease of electrical characterisation and coding. Fig 3 shows the input and output waveforms obtained when the device is used to perform the autocorrelation of a 13 chip, Barker coded, p-n sequence. The waveforms are shown prior to sample and hold circuitry, and the zero level is the level of output pulses obtained for no analogue input. Owing to the continuous operation of the device, the autocorrelation function should consist of twelve - 1's before and after the correlation peak of +13. The sidelobe levels obtained lie within the range -1.2 to +0.6; the deviation from theoretical being due primarily to residual and tap weight errors.

PARALLEL OPERATION

In order to make fuller use of the potential bandwidth of ccds, it is proposed to operate the shift registers in parallel, with clock drives as shown in fig 4. A sample of the input signal is taken on each of the clock phases and passed down separate registers. After an equal number of transfers in each register, the signal is detected, thus increasing the data rate or bandwidth by a factor of three for a three phase device. Consider, for example, the design of a 127 bit, 1 MHz data rate, linear array. If a cell length of 18 μm, a channel width of 100 μm, and a transfer inefficiency of 10^{-4} is assumed, then the primary advantages of using a parallel as compared to a normal design are given in Table 1. An added advantage of this technique is that when combined with biased-gate detection, integrated sample hold circuitry results (ref 6).

	Normal Design	Parallel Design	
Active Length	2.286	0.762	mm
Active Width	0.100	0.300	mm
Residual level	-28.4	-37.9	dB
Clock frequency	1.000	0.333	MHz

TABLE 1: Comparison of normal and parallel designs of a 127 bit, 1 MHz data rate, linear ccd array.

CONCLUSIONS

A tapping technique, which may be applied to virtually any of the current technologies, has been successfully demonstrated and some of the advantages and disadvantages outlined. For applications where a ccd programmable analogue filter is required, this technique should prove extremely useful. The operation of devices in parallel should also help to increase

data rates and aid in the manufacture of long linear arrays by reducing the physical length of the devices.

ACKNOWLEDGEMENTS

The authors wish to thank the British Science Research Council, the Ministry of Defence (CVD) and Microwave and Electronic Systems Limited for sponsoring these studies. Our thanks are due also to the semiconductor processing and evaluation laboratory at RRE for device fabrication, and the Director of RRE for permission to publish this article.

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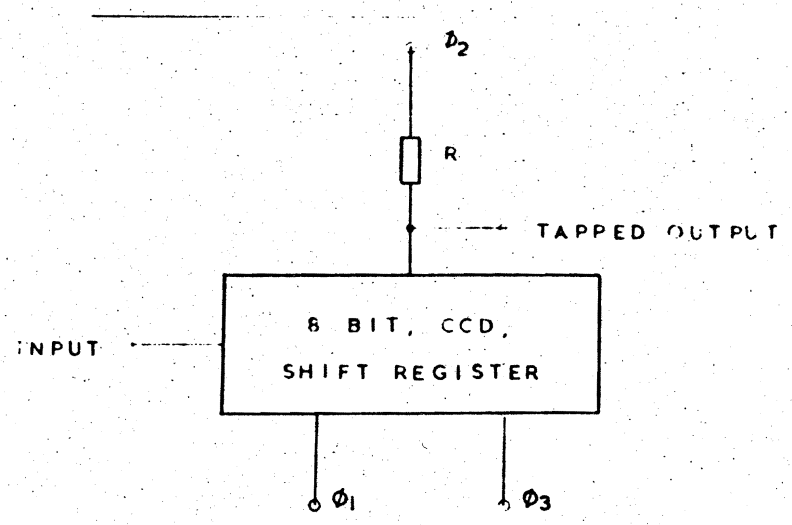
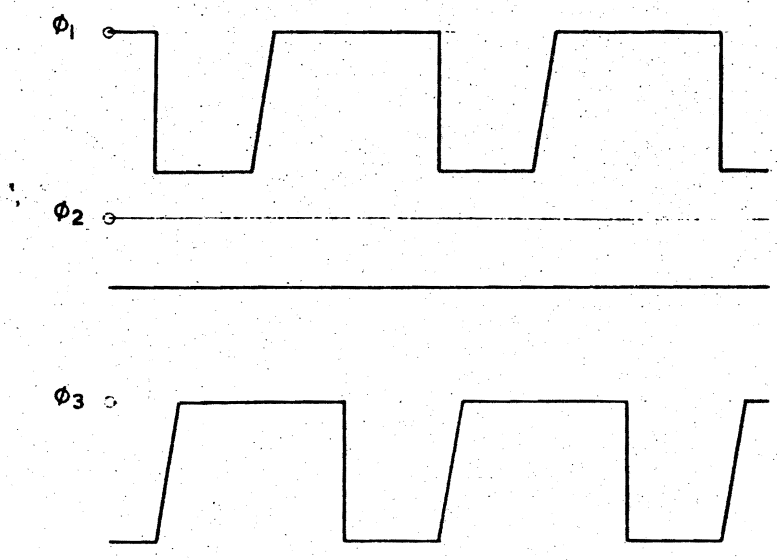
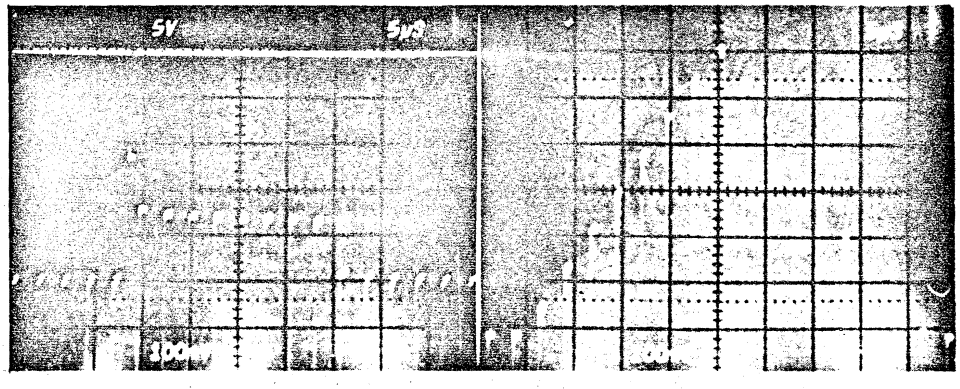


a) Electrical Connection

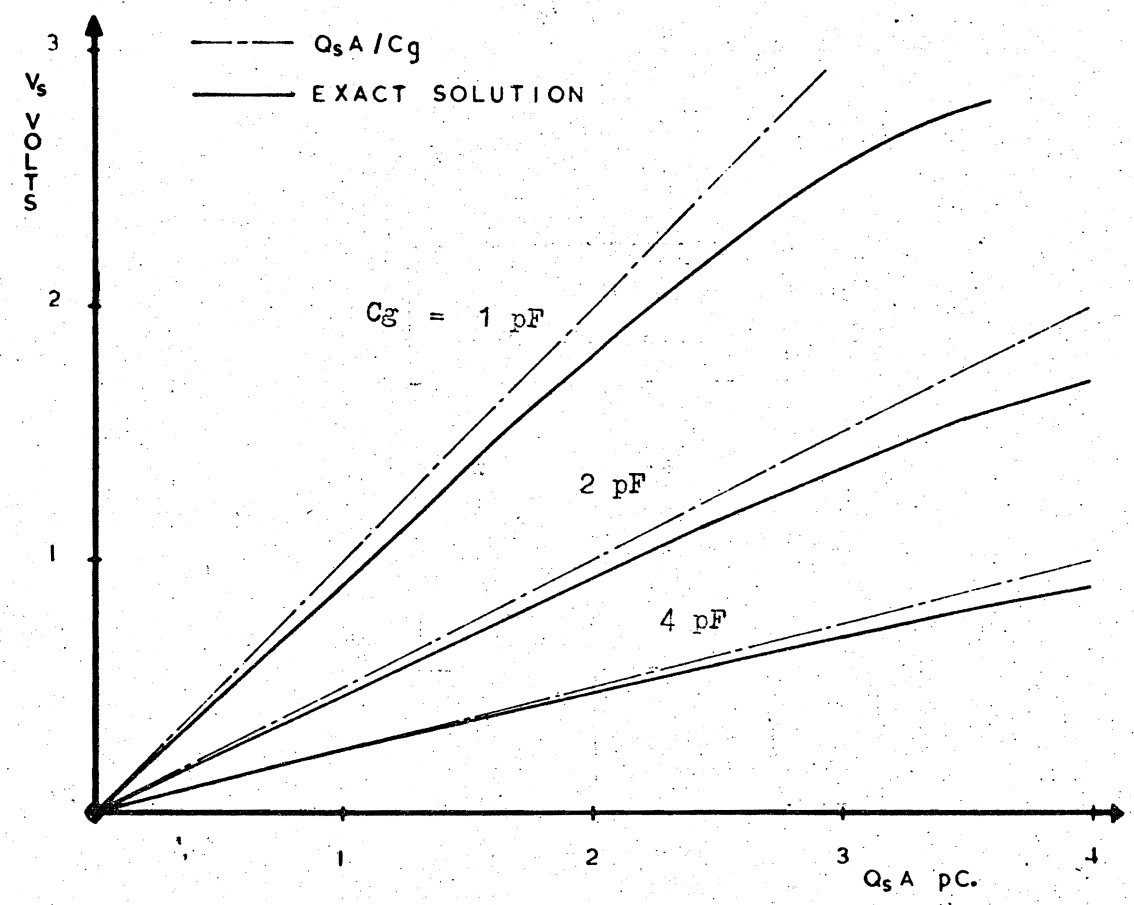


b) Clock Waveforms

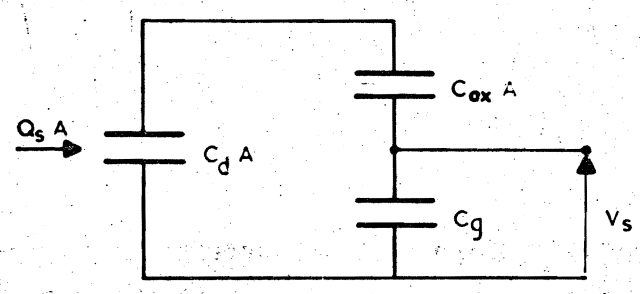


c) Impulse Response and Autocorrelation Function

Figure 1 Biased Gate Tapping Technique

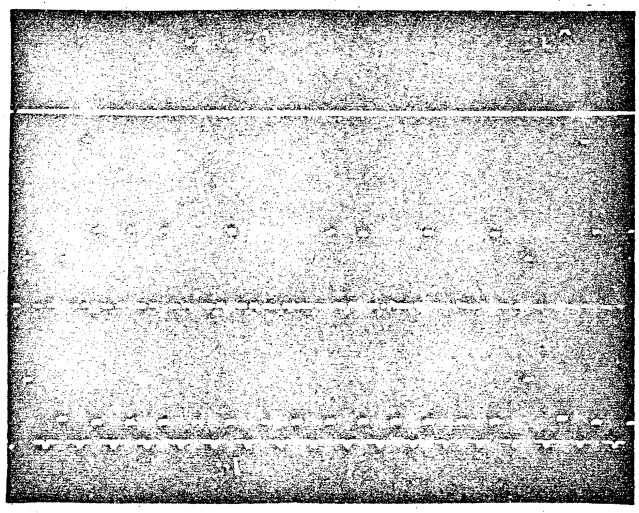


a) Signal Charge v. Output Voltage for varying Capacitance Cg

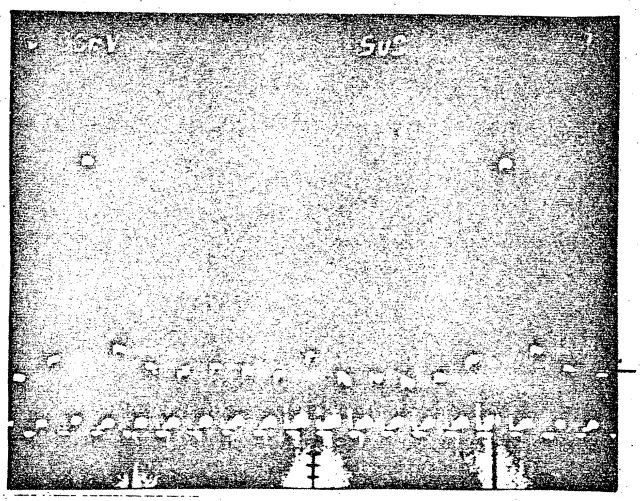


b) Simple Equivalent Circuit for Biased Gate.

Figure 2 Response of Biased Gate to Signal Charge



a) Impulse Response



b) Autocorrelation Function

Figure 3 Impulse Response and Autocorrelation Function for a 13 Chip Barker Coded p-n Sequence.

All waveforms are shown prior to sample and hold circuitry. The zero level is the level of output pulses due to fat zero and breakthrough: the output level obtained for no analogue signal input.

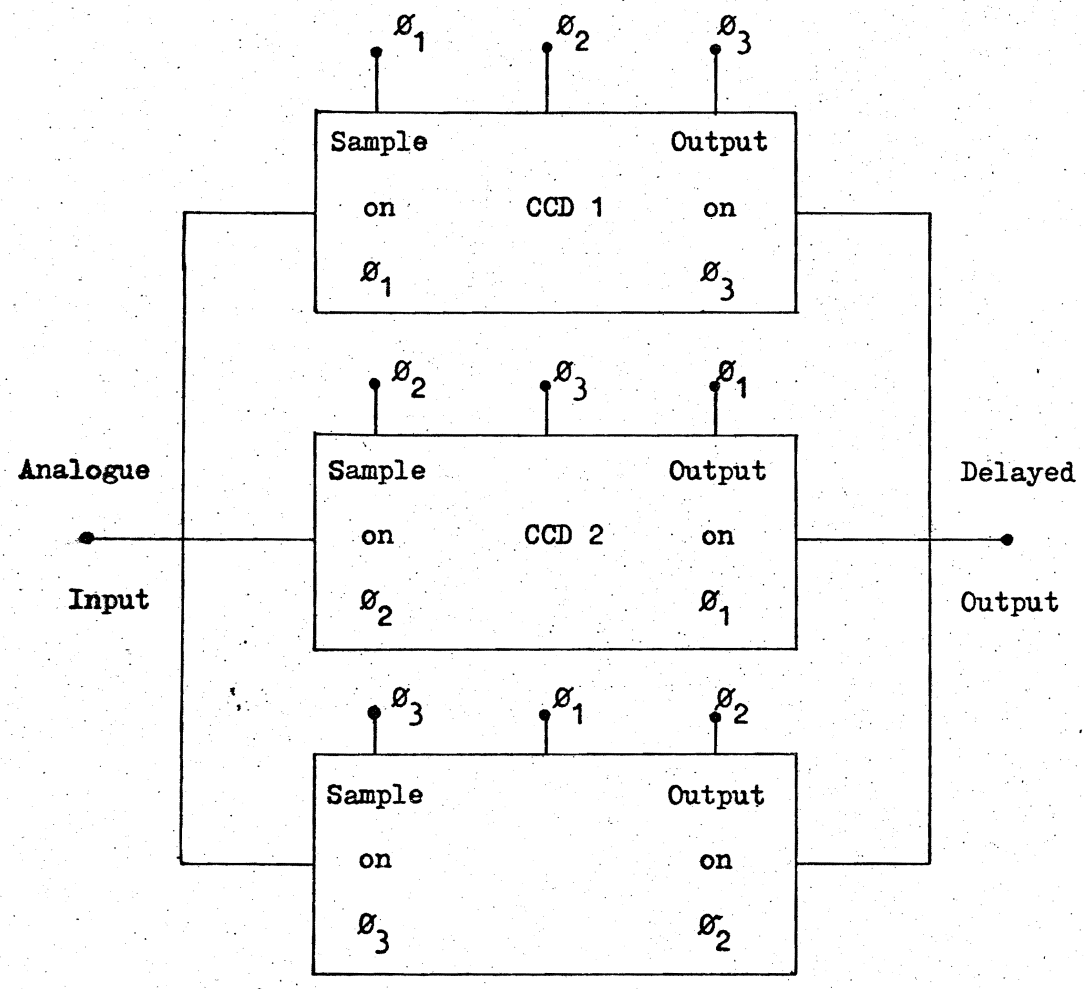


Figure 4 Parallel Operation of 3 Phase Devices