A TRADEOFF ANALYSIS OF TRANSFER SPEED VERSUS CHARGE-HANDLING CAPACITY FOR CCD'S

D. F. BARBE* AND N. S. SAKS*

ABSTRACT

In analog signal processing applications both speed and signal-handling capacity are of major importance. Therefore, it is important to know the tradeoffs between speed and signal-handling capacity for different CCD designs. These tradeoffs are discussed in this paper for surface-channel, shallow buried-channel, and deep buried-channel CCD's.

INTRODUCTION

The signal-handling capacity (SHC) of a CCD can be obtained from the basic electrostatic equation for an MOS capacitor. The transfer speed is obtained from an analysis of the dynamics of charge transfer. Accurate determination of both SHC and speed require computer calculations; however, the use of approximate analytical expressions for SHC and speed provides a better "feeling" for the tradeoffs involved. In this paper, approximate analytical expressions will be used.

SIGNAL HANDLING CAPACITY

The basic electrostatic equation for an n-channel surface-channel (SC) CCD is (Ref. 1)

$$V_G - V_{FB} - \frac{eN}{C_{eff}} = \phi_s + \frac{d}{\epsilon_{ox}} (2eN_A\epsilon_s)^{1/2} \phi_s^{1/2}, \qquad (1)$$

where $C_{eff} = C_{ox} = \frac{\epsilon_{ox}}{d}$, and

V_G = voltage applied to the electrode with respect to the substrate,
V_{FB} = flatband voltage of the MOS structure,
e = electronic charge,
N = mobile surface - electron density,
ϕ_s = surface potential,
d = oxide thickness,
ϵ_{ox} = dielectric constant of the oxide,
N_A = substrate doping density, and
ϵ_s = dielectric constant of the semiconductor.

*Naval Research Laboratory, Code 5260, Washington, D.C. 20375

If a potential well is formed by applying different voltages to adjacent electrodes, $\Delta V_G = V_{G_i} - V_{G_{i-1}}$, then it follows from Eq. (1) that the electron density required to fill the potential well is

$$N_{full} = \frac{C_{eff}\,\Delta V_G}{e} \quad , \tag{2}$$

where $C_{eff} = C_{ox}$ for a surface-channel CCD.

The basic electrostatic equation for a buried-channel CCD is somewhat more complicated than that for a surface-channel CCD and is derived as follows. The profile of potential vs. distance into semiconductor for a buried-channel MOS capacitor is shown in Fig. 1. It is assumed that the buried channel is depleted of charge by the application of a large positive voltage to the buried-channel layer and that minority carries density, N, is collected in the MOS capacitor. By Kirchoff's Law

$$V_G - V_{FB} + V_{ox} = \phi_j + \phi_c + \phi_s \tag{3}$$

Since $V_{ox} = \frac{1}{C_{ox}}$ (mobile charge density + fixed charge density), it follows that

$$V_{ox} = \frac{d}{\epsilon_{ox}}\ eN_D\ (t - \Delta t - N/N_D). \tag{4}$$

Using the depletion approximation, it follows that:

$$\phi_s = \frac{eN_D(t - \Delta t - N/N_D)^2}{2\epsilon_s} \quad , \tag{5}$$

$$\phi_c = \frac{eN_A L^2}{2\epsilon_s} \quad , \tag{6}$$

and

$$\phi_j = \frac{eN_D(\Delta t)^2}{2\epsilon_s} \quad . \tag{7}$$

Also,

$$\phi_{min} = \phi_c + \phi_j \quad , \tag{8}$$

and

$$\Delta t = \frac{N_A}{N_D}\ L. \tag{9}$$

Combining these equations gives

$$V_G - V_{FB} + V_I - \frac{eN}{C_{eff}} = \frac{N_D}{N_D + N_A}\,\phi_{min} + \left(\frac{d}{\epsilon_{ox}} + \frac{t}{\epsilon_s}\right) \times$$

$$\times \left(\frac{2e\epsilon_s N_D N_A}{N_D + N_A}\right)^{\frac{1}{2}} \phi_{min}^{\frac{1}{2}} \quad , \tag{10}$$

where

$$V_I = eN_D t \left(\frac{d}{\epsilon_{ox}} + \frac{t}{2\epsilon_s}\right) \quad , \tag{11}$$

$$\Delta t = \left(\frac{2\epsilon_s}{e}\,\frac{N_A}{N_D(N_D+N_A)}\,\phi_{min}\right)^{\frac{1}{2}} , \tag{12}$$

$$C_{eff}^{-1} = \frac{d}{\epsilon_{ox}} + \frac{t}{\epsilon_s}\left(1 - \frac{\Delta t}{t} - \frac{1}{2}\,\frac{N}{N_D t}\right), \tag{13}$$

and $N/N_D \leq t - \Delta t$.

Equation (10) has the same form as Eq. (1), and it is noted that if t is replaced by zero and $N_D/(N_D + N_A)\,\phi_{min}$ is replaced by ϕ_s in Eq. (10), this equation reduces to the surface-channel equation; i.e., Eq. (1). The interpretation of C_{eff} in Eq. (10) is the same as the interpretation in Eq. (1); i.e., $N_{Full} = C_{eff}\,\Delta V_G/e$.

Equations (10-13) are the basic electrostatic equations for buried-channel CCD's. Figure 2 shows curves of ϕ_{min} vs. $V_G - V_{FB}$ with N as a parameter for a shallow buried-channel (SBC) device; i.e., a device in which the channel is formed by ion implantation. Figure 3 shows similar curves for a deep buried-channel (DBC) device; i.e., a device in which the channel is formed by epitaxy. For a SBC CCD, $N_D \gg N_A$; therefore, $\Delta t/t \ll 1$. Then for the SBC case

$$C_{eff}^{-1} \simeq \frac{d}{\epsilon_{ox}} + \frac{t}{\epsilon_s}\left(1 - \frac{1}{2}\,\frac{N}{N_D}\right). \tag{14}$$

For a DBC CCD Δt, is not negligible, and C_{eff} is given by Eq. (13); however, C_{eff} is a slowly varying function of ϕ_{min} and for practical purposes C_{eff} can be treated as a constant in Eq. (13).

The signal-handling capacity of a CCD is defined as the full-well capacity; i.e.,

$$SHC = N_{full} = C_{eff}\,\Delta V_G/e. \tag{15}$$

Values of C_{eff} and SHC for three phase SC, SBC, and DBC devices

SPEED

A short time after the transfer process begins, the dominant transfer mechanism is self-induced drift. The fractional charge remaining in a well at time t after transfer is initiated is

$$\frac{N_r}{N_o} = \frac{t_{si}}{t_{si} + t} \quad , \tag{16}$$

where

$$\tau_{si} = \frac{2\ell^2 C_{eff}}{\pi \mu_n e N_o} \quad , \tag{17}$$

and

N_o = electron density in the transferring well at t = o,

N_r = electron density remaining in the transferring well at time t,

ℓ = center-to-center electrode spacing, and

μ_n = effective electron mobility.

For $t > t_{si}$, the fringe field mechanism becomes dominant. The minimum fringe field under the transferring electrode is (ref. 2)

$$E_{min} = \frac{\Delta V_G}{L} \exp\left(-\frac{\pi \epsilon_s}{3 C_{eff} \ell}\right) - \exp\left(-\frac{\pi \epsilon_s}{C_{eff} \ell}\right) \tag{18}$$

In cases where the approximation $\exp(-x) \simeq 1-x$ can be used, Eq. (18) takes on the simple form

$$E_{min} \simeq \frac{2\pi \epsilon_s \Delta V_G}{3 C_{eff} \ell^2} \quad , \tag{19}$$

and

$$\frac{N_r}{N_o} = e^{-t/\tau_{ff}} \quad , \tag{20}$$

where

$$\tau_{ff} = \frac{\ell}{\mu_n E_{min}} = \frac{3 C_{eff} \ell^3}{2\pi \epsilon_s \mu_n \Delta V_G} \tag{21}$$

The values of τ_{si} and τ_{ff} for the structures discussed here are given in Table I.

CAPACITY-SPEED PRODUCT

For a CCD operated at frequencies where transfer is self-induced field limited,

$$\text{capacity x speed} \simeq \frac{\pi W C_{eff} (\Delta V_G)^2 \mu_n}{2 e \ell} \tag{22}$$

Consider the tradeoffs of the SC structure vs. the SBC structure vs. the DBC structure. Since the surface mobility is ~ 500 cm^2/V-sec, the bulk mobility in a region having a doping density of $N_D = 3 \times 10^{16}$ cm^{-3} is ~ 1000, and the bulk mobility in a region having a doping density of $N_D \simeq 7 \times 10^{14}$ is ~ 1500,, it follows that capacity-speed product is greatest for the SBC structure operated in the self-induced-field limited regime.

For a CCD operated at frequencies where transfer is fringe-field limited, the product of the speed $(1/\tau)$ and the signal capacity (SC = SHC x Wxℓ) is

$$\text{capacity x speed} \simeq \frac{2\pi \epsilon_s W (\Delta V_G)^2 \mu_n,}{3 e \ell^2} \tag{23}$$

Taking into account the different values of μ_n for the SC, SBC, and DBC structures as indicated in Table I, the DBC device has the largest capacity-speed product in the fringe-field limited regime.

SUMMARY

In summary, the capacity-speed product is different for surface-channel, shallow buried-channel, and deep buried-channel CCD's because of two factors: (1) the effective capactance of the structure and (2) the minority carrier mobility. In all three structures the capacity-speed product is increased by increasing W and ΔV_G or by decreasing ℓ. For the specific structures considered in this paper, the capacity-speed product was greatest for the SBC structure in the self-induced-field limited regime and for the DBC structure in the fringe-field limited regime.

REFERENCES

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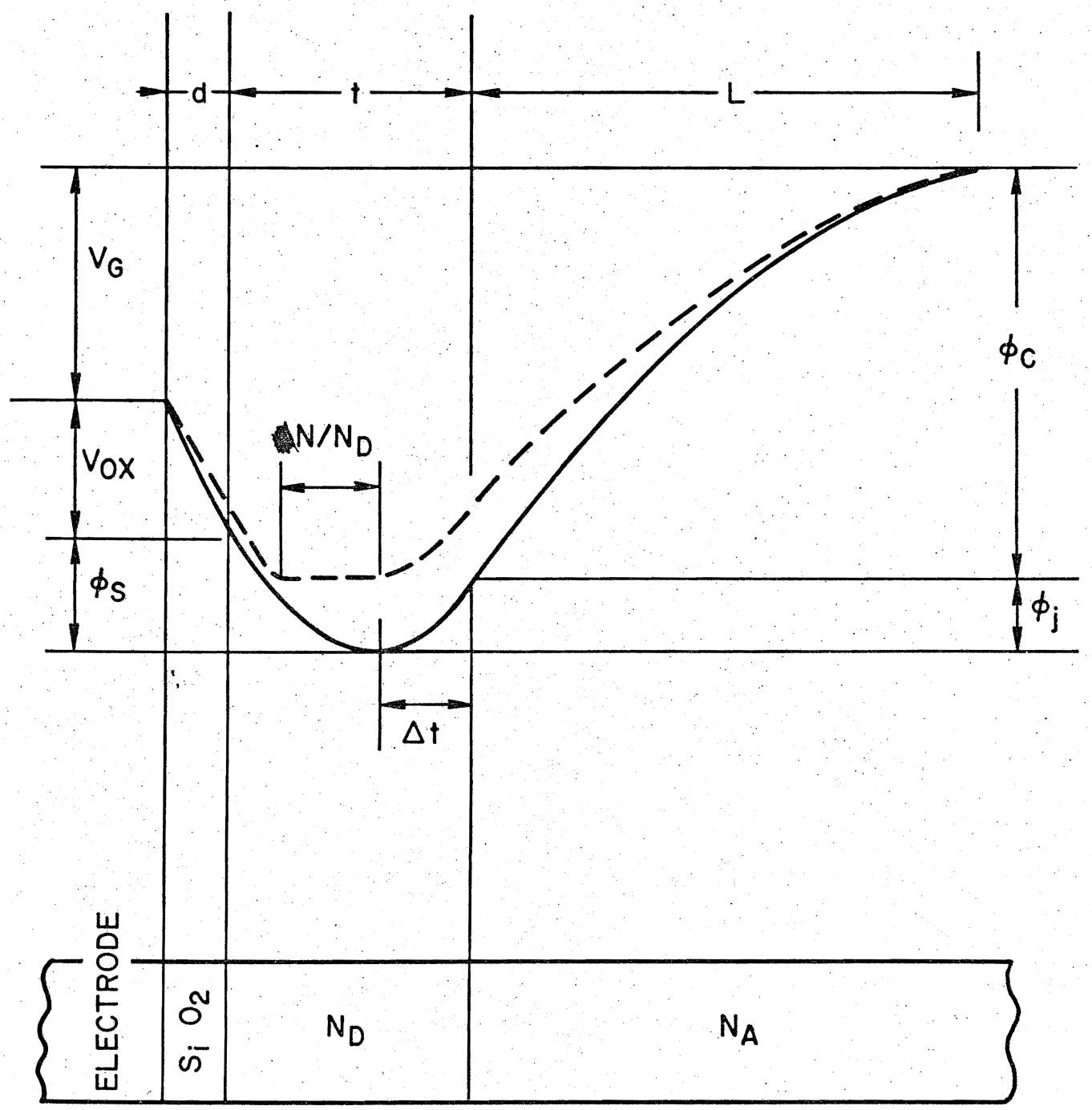

Fig. 1. Potential profile of buried channel CCD

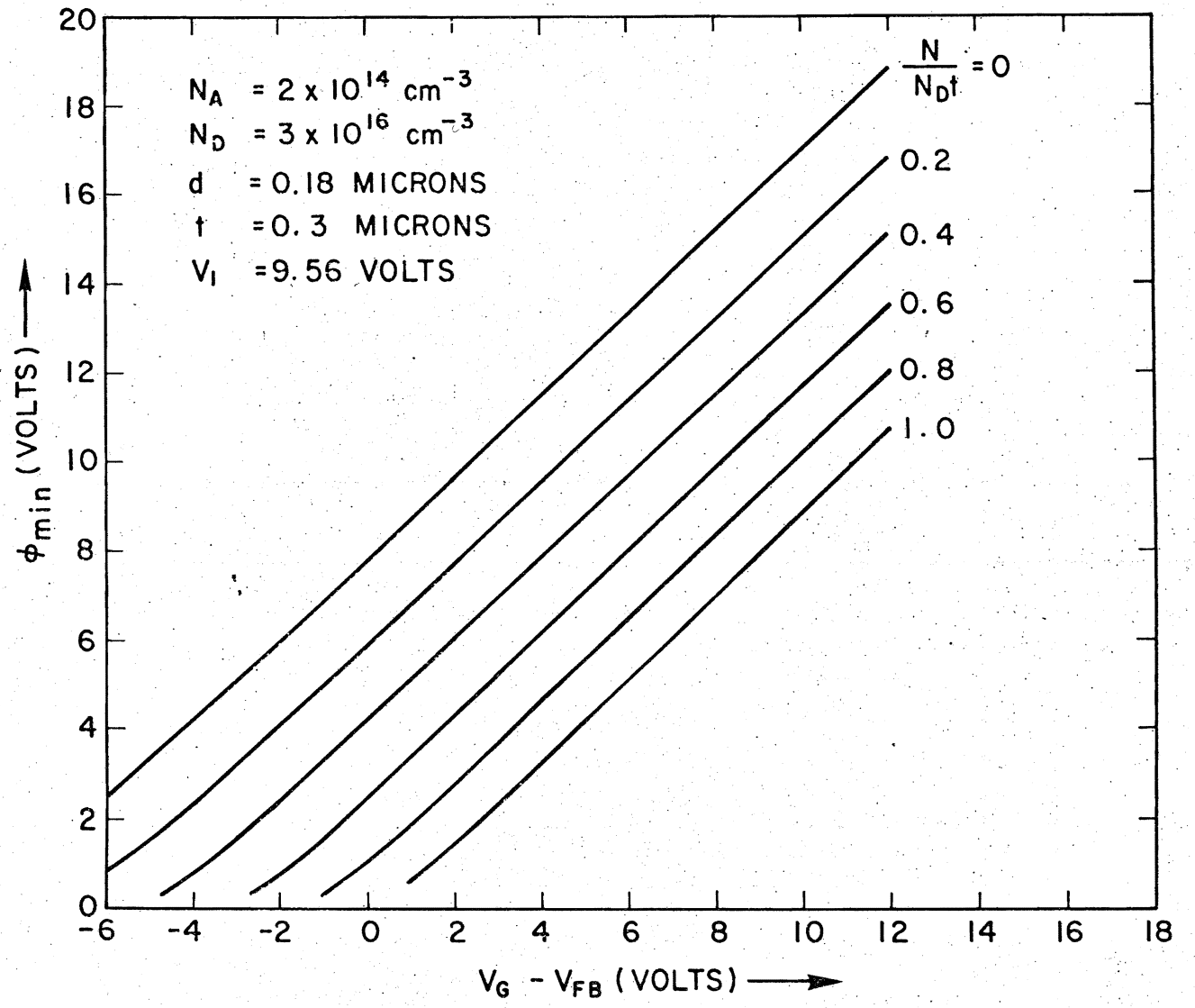

Fig. 2. Minimum potential vs. gate voltage for an implanted-channel CCD.

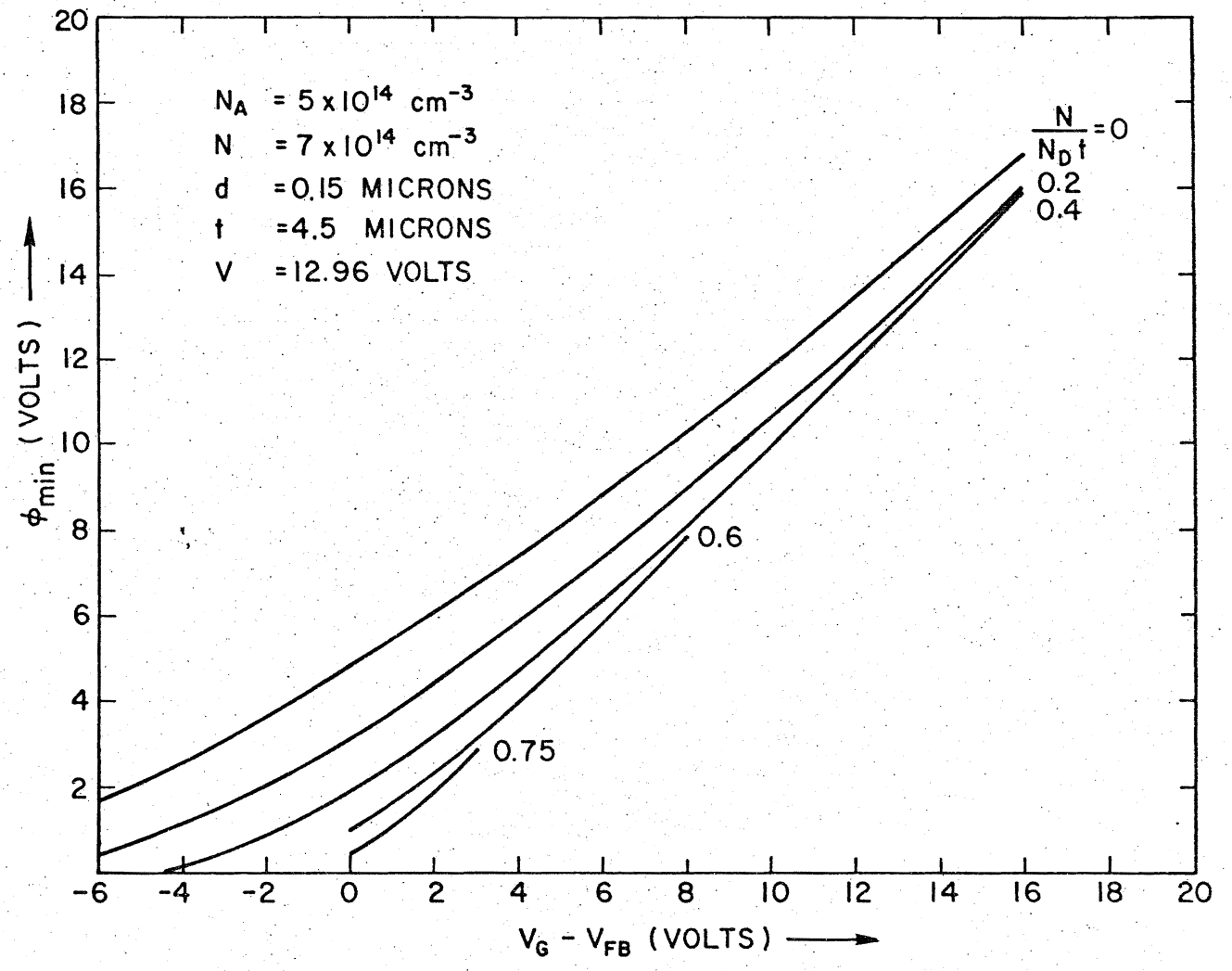

Fig. 3. Minimum potential vs. gate voltage for an epitaxial-channel CCD.

Table I. Parameters which influence the capacity-speed product for CCD's

	C_{eff} (f/cm^2)	SHC (cm^{-2})	μ_n ($cm^2/V\text{-}sec$)	τ_{ff} (ns)	τ^*_{si} (ns)
SC	2×10^{-8}	6×10^{11}	500	3.8	0.26
SBC	1.5×10^{-8}	5×10^{11}	1000	1.4	0.13
DBC	0.46×10^{-8}	1.4×10^{11}	1500	0.26	0.09

ΔV_G = 5 volts, $^*N_0$ = SHC, 3-Phase with 1.2 mil cells.