CHARGE-COUPLED STRUCTURES WITH SELF-ALIGNED SUB-MICRON GAPS

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ABSTRACT

A technique for fabricating charge-coupled devices with sub-micron gaps is described. The method relies on a "shadowing" effect produced by oblique deposition of the metal in an otherwise standard vacuum evaporation process. The biggest advantage of the technique is its extreme simplicity, particularly for one-dimensional C.C.D. structures.

The feasibility of the technique has been demonstrated for two- and three-phase devices; the two-phase structure was a 32-bit shift register which has been operated at up to 10 MHz.

With some additional processing the technique can be used to make bi-directional C.C.D. arrays as required in area imagers and serpentine shift registers.

INTRODUCTION

It is well established that for efficient charge transfer in charge-coupled structures, the interelectrode gap must be made very small (< 2 μm). Such a small dimension is not easily achieved with conventional processing and novel techniques for overcoming this problem, and indeed making gaps much smaller than 2 μm, have recently been proposed; these include aluminium anodisation (ref 1) and undercut isolation (ref 2). These techniques suffer from the disadvantages of complex fabrication technology.

We have developed a technique for fabricating C.C.D. structures with sub-micron lateral gaps. The method relies on a "shadowing" effect produced by oblique deposition of the metal in an otherwise standard vacuum evaporation process. The technique is much simpler than those which have previously been proposed for producing narrow lateral gaps for C.C.D. structures; it can also be used to fabricate two- or three-phase devices.

THE SELF-ALIGNED GAP TECHNIQUE

For two-phase structures a layer of silicon dioxide is first grown on the surface of the silicon slice and a series of windows then etched in this oxide film. The slice is subsequently re-oxidised so that a thin oxide forms in the original windows which are now surrounded by thicker oxide. A section through the structure now has a castellated appearance - see Fig. 1. (We discuss below the factors that determine the two-oxide

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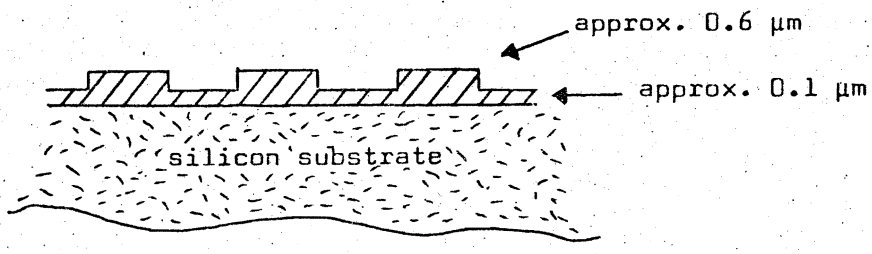

Figure 1. Castellated structure prior to metallisation.

thicknesses but typical figures are 0.1 μm and 0.6 μm.) The silicon slice is now placed in an evaporation unit and metallised from a single source so that discontinuities are created in the deposited metal layer wherever steps in the oxide shield part of the silicon surface from the beam (see Fig. 2). These discontinuities form the required inter-

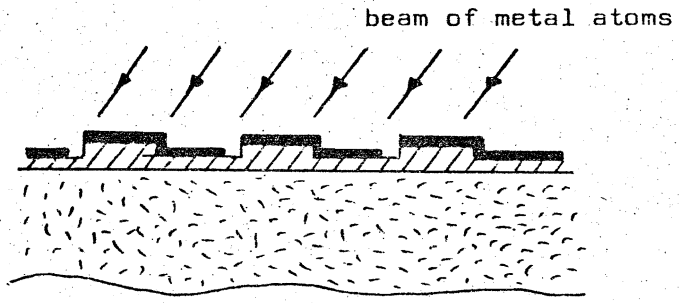

Figure 2. Metallisation at angle so as to produce "shadow" on oxide.

electrode gaps, the width of which will be of the same order as the height of the oxide step (0.5 μm in the above example) for an angle of incidence of the metal atoms of 45°. The remainder of the C.C.D. electrode pattern is subsequently defined by a standard etching process.

Each electrode is thus separated from the underlying silicon by two different thicknesses of oxide, thereby producing a structure suitable for two-phase operation in which the adjacent electrode pairs are automatically connected together. This simplifies the electrode interconnection pattern subsequently required and also obviates the need for dig downs as in a conventional two-layer structure. It will be appreciated that the sub-micron interelectrode gaps do not require critical alignment or any special photolithographic techniques.

To obtain well defined gaps in the metallisation a good quality oxide step (ideally as near-vertical as possible) and a well collimated metal-vapour beam are necessary. In this connection we have investigated the effect of etch temperature upon the profile of the oxide step (ref 3); we have found that a near-vertical oxide edge can be obtained near the top of the step if the etch temperature is no more than 25°C (at higher temperatures the oxide edge becomes shallower). By evaporating the metal at a relatively low rate (of the order of $10^{-3}cm^{-3}s^{-1}$) from a conventional tungsten spiral and employing a source-to-target distance of 20 cm, we have obtained a sufficiently well-collimated beam to produce satisfactory self-aligned gaps. The simplicity of this technique is highlighted by the fact that the differential oxide thickness, which allows two-phase

operation of the device and also gives rise to the sub-micron gaps in the metallisation, is achieved with only one photolithographic stage.

A variation on the above technique can be used to fabricate three-phase C.C.D.'s. In this case a uniform oxide layer is grown on the silicon and the slice is then metallised in the conventional way. Most of the metal is now etched away to leave a series of parallel stripes on the oxide surface. The slice is now metallised at an oblique angle as for the two-phase structure. The second metallisation covers the existing stripes and the oxide in between these stripes except for the regions in the "shadow" of the original stripes. By using standard etching techniques to remove the excess metal, a series of closely spaced electrodes can be formed, all of which are separated from the silicon substrate by a uniform thickness of oxide.

INVESTIGATION OF GAP FORMATION

Two- and three-phase C.C.D. structures have been fabricated using the techniques described above. Most of our effort so far has, however, been expended on two-phase devices which we have made using aluminium and gold/nichrome metallisation. Electron microscopic examination of the gap formation has been carried out in each case and the results are presented below.

Aluminium: In the case of gaps formed in aluminium films our studies have revealed that the gaps are always smaller than would be expected on a geometric basis. It became apparent that this was due to the migration of aluminium atoms into the gap region during evaporation. Fig. 3 shows a

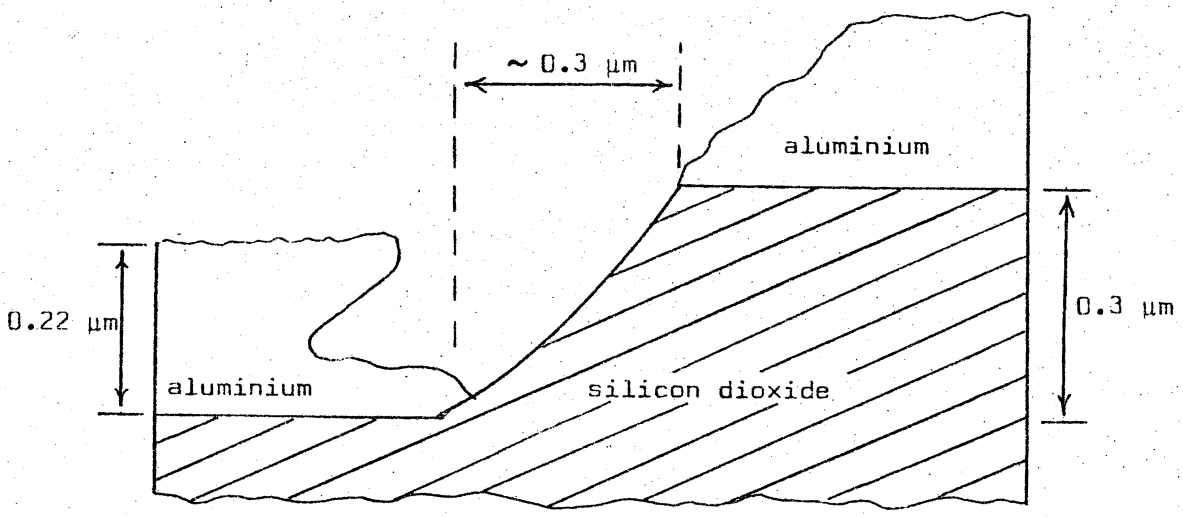

Figure 3. Cross-section of self-aligned gap in aluminium film.

cross-section of the gap deduced from a transmission electron microscope study using a standard replication technique. The oxide step height in this case was 0.3 µm and a source-to-target evaporation angle of 60^{o} (to the normal) was used. The expected gap width was therefore 0.3 tan 60^{o} $\simeq$ 0.5 µm but from the figure it can be seen that the gap is only 0.3 µm wide. It was found that gaps could not be formed reliably with such a geometrical arrangement - shorts between adjacent electrodes frequently occurred.

It might be thought that, for this particular oxide step, a more oblique angle of metallisation could be used to overcome this problem of shorts. However we found that at very oblique angles ($\gtrsim 70^{\circ}$) the aluminium film was of poor quality (it became non-conducting). Thus it became necessary to increase the oxide step height. A substantial improvement in reliability was obtained for oxide steps in excess of 0.4 μm. In the fabrication of the C.C.D.'s described later in this paper we used an oxide step height of 0.6 μm. In this case the geometrically predicted gap width is 1 μm, but it was 0.8 μm in practice; i.e. in both cases atom migration appears to reduce the gap width by 0.2 μm.

Gold/Nichrome: Experiments performed using gold/nichrome for the metallisation revealed that no significant atom migration takes place during evaporation. The cross-section of a gap formed in a gold/nichrome film (again deduced from transmission electron microscope studies) is shown in Fig. 4. In this case the oxide step was 0.3 μm and the angle of evapora-

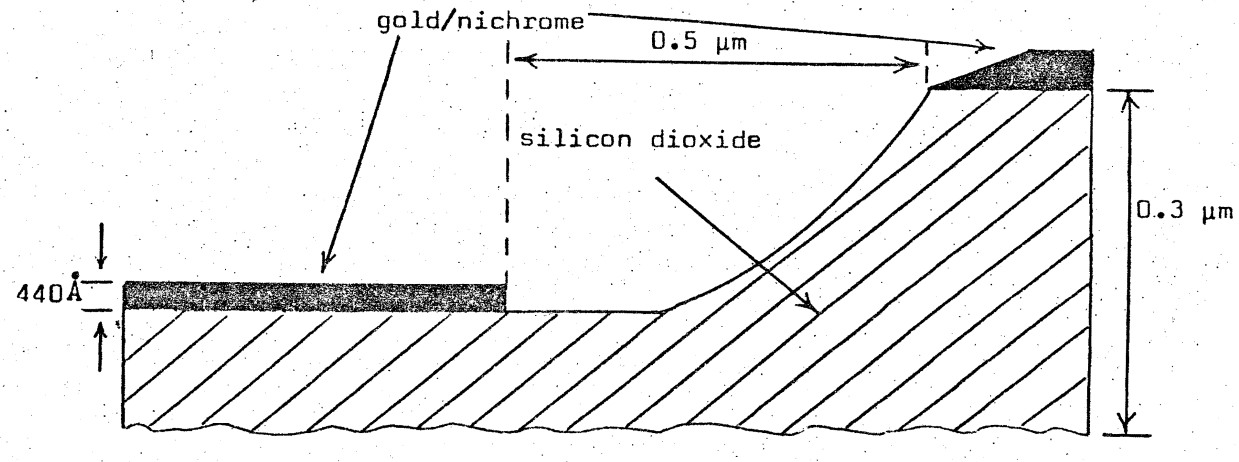

Figure 4. Cross-section of self-aligned gap in gold/nichrome film.

tion 60° to the normal, as in Fig. 3; however, unlike the aluminium situation, the gap was 0.5 μm as expected. The gap in the gold/nichrome film is so well defined that we are confident that gaps at least as small as 0.3 μm could be fabricated by this technique. The minimum gap which can be reliably formed using aluminium is approximately 0.5 μm.

The gold/nichrome metallisation procedure does, however, suffer from the disadvantage that in order to achieve good adhesion of the metal to the SiO_2, the substrate has to be heated to approximately 400°C during the evaporation. This implies that gold/nichrome metallisation cannot be used in processes (such as the bi-directional C.C.D. described later) requiring an evaporation onto a slice partly covered with photoresist, since 400°C exceeds the melting point of the resist. However for structures where the only concern is for a very closely spaced metallisation pattern in only one direction, gold/nichrome has a significant advantage over aluminium.

THRESHOLD VOLTAGE CONSIDERATIONS

In a two-phase charge-coupled device the charge carrying capability is directly proportional to the difference in threshold voltage, V_{TH}, between the thick and thin oxides. With too small a differential only a small amount of charge can be stored beneath the lower electrode; on the other hand a large differential implies a high V_{TH} for the thick oxide, and hence

large clock voltages. V_{TH} is a function of oxide thickness and the fixed interface stage charge Q_{SS}; however the selection of oxide thickness to give both reliable gap formation and a suitable threshold voltage differential (say 5V) is not straightforward since Q_{SS} is itself a function of oxide thickness (ref 4). As a result of experimental work we concluded that oxide thicknesses of 0.1 μm and 0.6 μm grown on 5 Ω.cm n-type <111> material would give satisfactory threshold voltages; in order to obtain suitable values of Q_{SS} the slice is removed rapidly (< 2s) from the high temperature (1200°C) dry oxidation furnace.

C.C.D. FABRICATION RESULTS

In order to demonstrate the feasibility of C.C.D. fabrication using the self-aligned gap technique, several 32-bit C.C.D. shift registers have been fabricated. A photomicrograph of one such shift register is shown in Figure 5(a) and a close-up of the interelectrode structure in Figure 5(b); the total gap perimeter in this shift register is 0.64 cm.

Using a recently developed technique (ref 5), we have determined the frequency response of these C.C.D.'s and have found that they have a typical transfer inefficiency of 10^{-3} at 1 MHz. This rather high transfer inefficiency is attributed to the existence of a large number of fast surface states since no low temperature oxide anneal was performed to effect their removal. However, this in no way affects the validity of the fabrication technique. A suitable oxide anneal has recently been adopted in our laboratory, and will be incorporated in our C.C.D. processing schedule in future.

The input and output waveforms of a 32-bit C.C.D. operated at 500 kHz using an on-chip reset sensing M.O.S.T. and amplifier are shown in Figure 6. A single '1' is entered into the register at the far left of the picture and appears at the output (bottom trace) 32 bits later.

DEVELOPMENT OF THE SELF-ALIGNED GAP TECHNIQUE FOR BI-DIRECTIONAL ARRAYS

The charge shifting direction of a two-phase C.C.D. is built into the structure and using the self-aligned gap fabrication technique the interelectrode gaps are formed in such a way that charge can be shifted only in the direction opposite to that in which the metal was evaporated (see Fig. 2). However, in large memories a serpentine motion of charge flow is required and in imaging arrays one needs orthogonal motion. To achieve this capability using the self-aligned gap fabrication technique, an additional evaporation and two masking stages are required.

Consider the problem of fabricating two 2-phase C.C.D.'s parallel to one another in which information is to be transferred in opposite directions. In order to fabricate such devices (we shall refer to them as CCD1 and CCD2) the castellated oxide structure of both C.C.D.'s is first formed and then evaporated with aluminium from one direction (the right, say). The metallisation pattern for CCD1 is then etched out together with all the aluminium covering the CCD2 register; charge can then be moved from left to right along CCD1. A layer of positive photo-resist is now defined over CCD1 but leaving the interconnections between registers unprotected (Figure 7(a)). The slice is then evaporated with aluminium from the left so that the gaps formed in the shadows of the thick oxide of

CCD2 will cause the charge in this register to move from right to left (the interelectrode gaps of CCD1 have, of course, been protected from this second metallisation by the layer of photo-resist). The metallisation pattern of CCD2 including the interconnections to CCD1 is now defined and the surplus metal including that on top of the photo-resist covering CCD1, is removed. The photo-resist covering CCD1 and defining CCD2 is then dissolved away leaving two parallel C.C.D. registers that will transfer charge in opposite directions (Figure 7(b)).

We have successfully fabricated C.C.D. structures similar to that shown in Figure 7, and so established that our self-aligned gap technique can be used for bi-directional arrays.

Despite the two extra masks involved in fabricating a bi-directional C.C.D. array, the self-aligned gap technique is still simpler than many others for producing sub-micron gaps. A total of seven masking stages, including those for channel confinement and diffusions, are required for a bi-directional array; five masks are needed for a uni-directional shift register.

CONCLUSIONS

A technique has been developed whereby 2- or 3-phase C.C.D.'s with closely spaced metallisation patterns can be fabricated using oxide steps or a thick metal film to produce shadows in the beam of metal vapour when this is deposited obliquely to the plane of the slice.

The feasibility of the technique has been established by the fabrication of several C.C.D. shift registers. Using aluminium, interelectrode gaps as small as 0.5 μm can be formed while, with gold/nichrome, even smaller gaps can be made. Using aluminium the technique can be extended to bi-directional 2-phase structures. The complexity of the process compares favourably with others that have been proposed for producing C.C.D. structures with sub-micron gaps.

ACKNOWLEDGEMENTS

This work is supported by the Science Research Council and Southern Television Limited.

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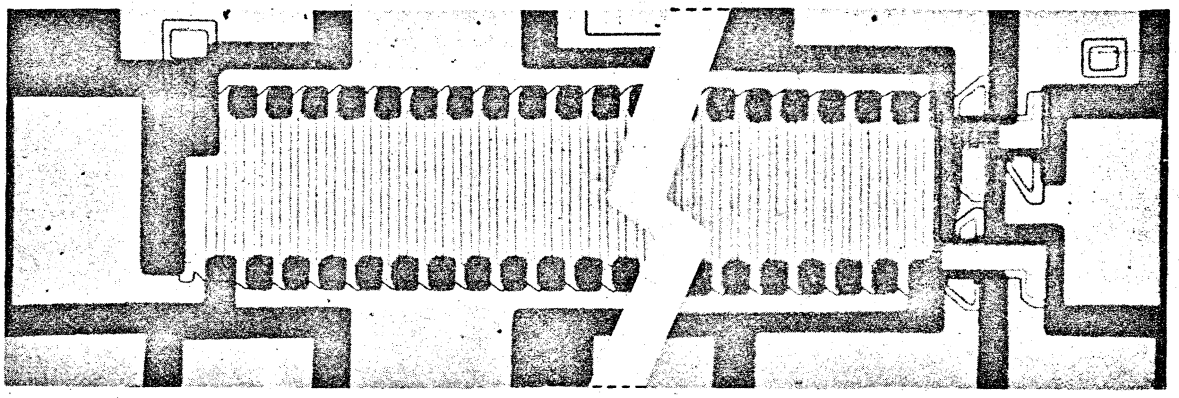

Figure 5(a). Photomicrograph of a 32-bit C.C.D. shift register.

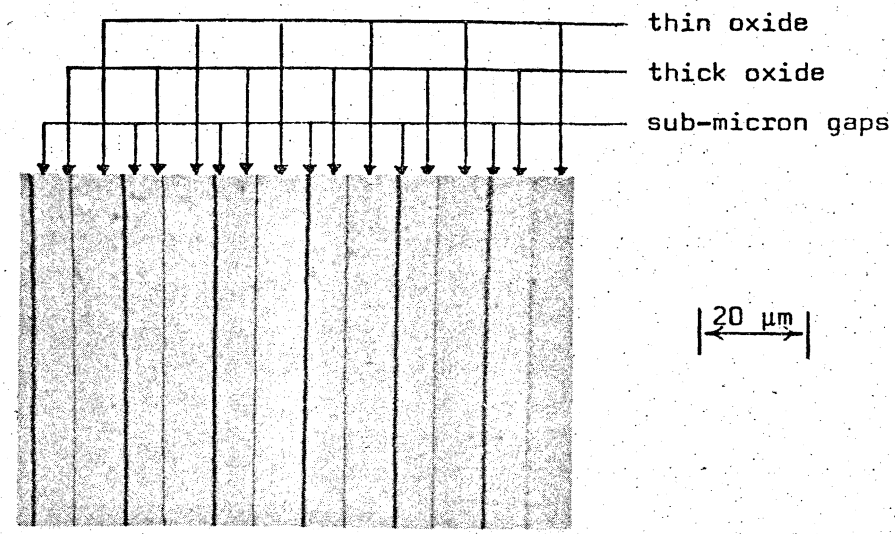

Figure 5(b). Close-up of part of the C.C.D. shift register showing the interelectrode structure.

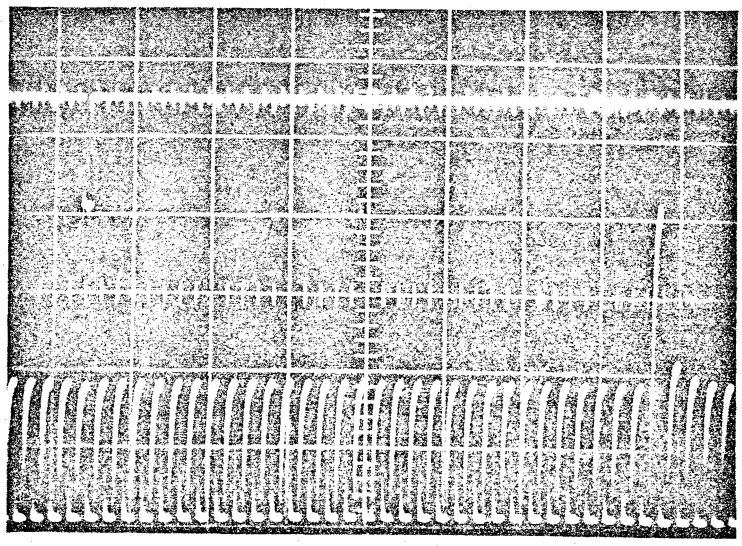

Figure 6. 32-bit C.C.D. operated at 500 kHz showing a single '1' delayed by 64 shifts. Vertical scale: 2V/div.

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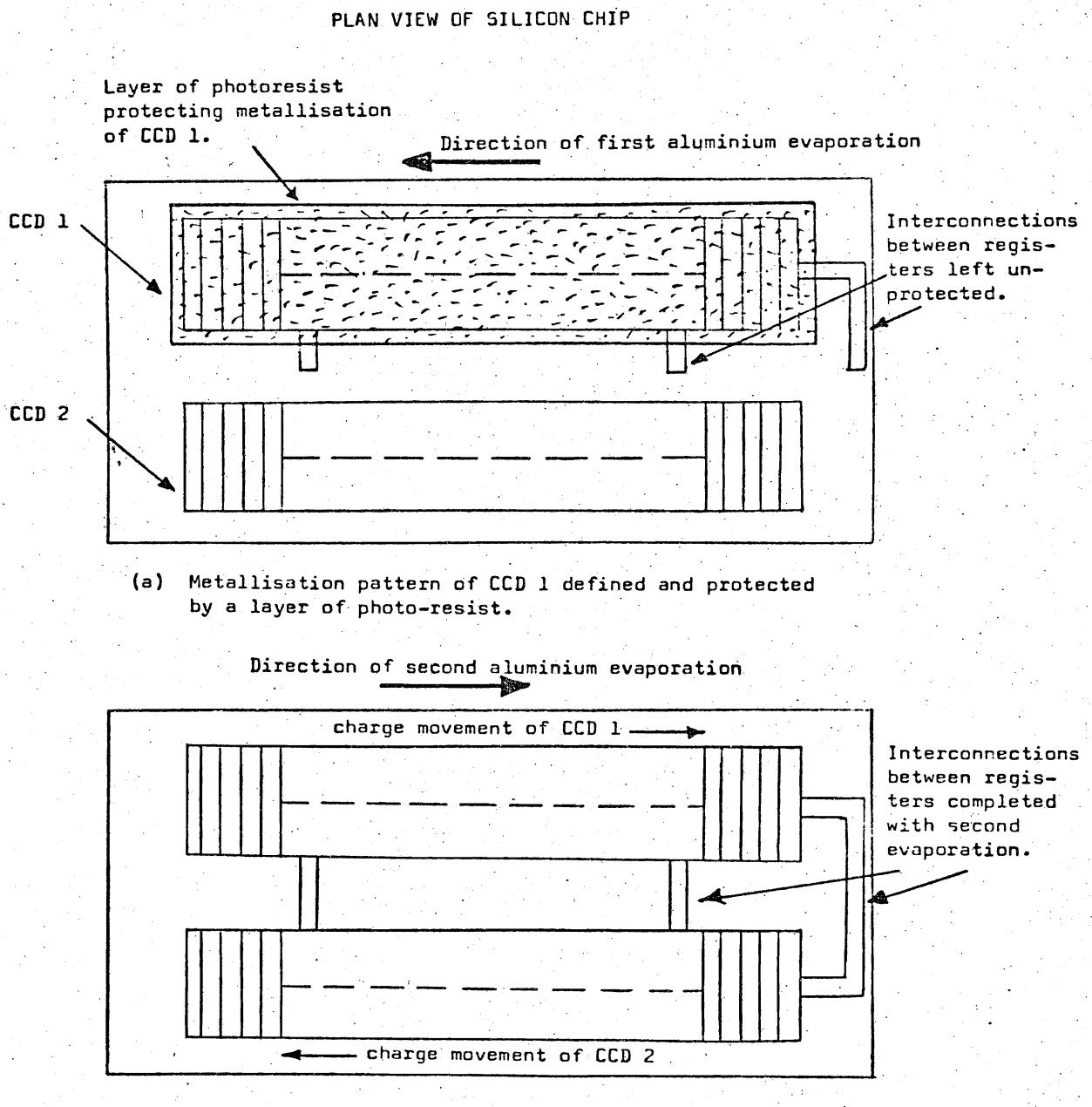

Figure 7. Fabrication of bi-directional arrays using the self-aligned gap technique.