INTERFACE STATES IN Si-SiO_2-INTERFACES

A. Goetzberger [x]

ABSTRACT

Interface states in Si-SiO_2 interfaces are reviewed. Basic concepts, models for the origin of interface states are discussed. There seems to be a number of different effects causing states. Measurements of surface state distributions show a steep increase of density towards the band edges. Electron capture cross sections decrease in the same range.

Present day technology permits growth of oxides with extremely low interface state densities.

Stressing at negative bias and moderate temperatures increases surface state density noticeably.

1. INTERFACE STATES: GENERAL CONCEPTS

Interface states, or surface states as they are also called are generally assumed to reside in the plane of the interface between a semiconductor and an insulator. The bulk of scientific and technical work to date has been applied to the Si-SiO_2 interface which will be dealt with exclusively in this article.

The definition of a surface state is illustrated in Fig. 1A.

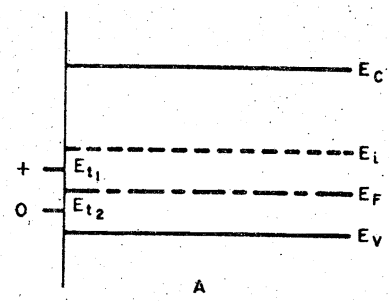


Fig. 1A: Definition of surface states. E_{t1}, E_{t2} are surface state levels, E_F = fermi energy

x Institut für Angewandte Festkörperphysik der Fraunhofer Gesellschaft 7800 Freiburg, Eckerstrasse 4

The surface state is an allowed level within the forbidden gap at the surface. In contrast to surface charges which retain their state of charge surface states can exchange charge carriers with the bulk. The probability of finding the level in its more positive state is given by the fermi function,

$$f = (1 + g \exp(E_F - E_t)/kT)^{-1} \qquad (1)$$

where E_F is the energy of the fermi level, E_t the energy of the surface state and g the spin correction factor. A donor type surface state changes its charge from 0 to +1, an acceptor type state from -1 to O when passing through the fermi level. According to equ(1) the surface state level is more positively charged when it is above the fermi level. In Fig. 1 A two donor states at energies E_{t1} and E_{t2} are shown. E_{t1} is above the fermi level E_F and therefore positively, E_{t2} is below and therefore uncharged.

Fig. 1B shows a greatly simplified equivalent circuit of a surface state

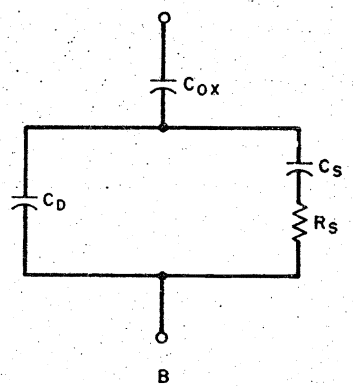


Fig. 1B: Equivalent circuit of MOS capacitance

in an MOS structure. C_{ox} is the oxide capacitance, C_D the depletion capacitance, C_s the surface state capacitance and R_s the surface state resistance. C_s and R_s can be understood as follows:

Since a surface state can accept charge it is represented as a capacitance. Charging and discharging of the state is associated with various degrees of time delay leading to a time constant $\tau = R_s C_s$. The time constant is also related to the capture cross section σ for carriers by

$$\sigma = \frac{1}{\sigma_n \bar{v} n_{so}} \qquad (2)$$

where $\bar{v}$ = average thermal electron velocity, n_{so} = equilibrium electron

sity at the surface. Equ(2) is expressed for electron capture. Surface e quantities of practical and scientific interest are density per cm^2, ergy level, and capture cross section. In practical surfaces the surce states are not all at the same energy level but distributed throughout the energy gap. Therefore one has to determine density and capture oss section in dependence of energy.

2. MEASUREMENT TECHNIQUES

A large number of measurement techniques for interface states have been devised. Only the most widely used ones can be discussed here. The most straightforward technique is measurement of the surface state capacitance. Of all capacitance techniques the slow ramp technique (ref 1, 2) is most widely used because it gives surface state densities over a broad range of the gap in very short time. The ramp technique uses a linear voltage ramp to measure MOS capacitance at an extremely low equivalent frequency. This is necessary because the response time of minority carriers is very long in good samples. In addition to this measurement capacitance is measured at a high frequency beyond the response time of the surface states. The difference between the two capacitance voltage curves is then the contribution of surface state capacitance. If the equivalent circuit of Fig. 1B is evaluated surface state density N_{ss} is obtained.

$$N_{ss} = \left[\frac{C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{HF}}{C_{ox}-C_{LF}} \right] \frac{C_{ox}}{qA} \qquad (3)$$

where C_{LF}, C_{HL} = low frequency, high frequency capacitance respectively. A = area of capacitance, q = elementary charge.

Besides surface state density one has to determine surface potential or band bending at the surface. This is usually done by converting the voltage variable to surface potential. The well known dependence of space charge capacitance C_D is used for this purpose. The second technique to be discussed here is the conductance technique. It measures mainly R_s, the surface state resistance together with the C_s. The conductance technique (ref 3, 4) is much more time consuming but it yields not only surface state densities but also capture cross section. It is therefore required when information about dynamic surface state behavior is desired. The conductance technique has shown that the equivalent circuit of Fig. 1A is much too simplified. The surface state branch consisting of R_s and C_s is paralleled by an infinite number of RC branches leading to a dispersion of time constants. This effect can be of great magnitude and has to be considered in evaluation of surface state density.

The reason for this time constant dispersion is a fluctuation of surface potential caused again by statistical fluctuation of charge at the interface (ref 3). This charge consists of the positive surface state charge and charge in interface states. Fig. 2 shows how charge fluctuation leads to fluctuation of field and potential at the surface. Even small charge fluctuations cause large fluctuations of time constants because τ is exponentially

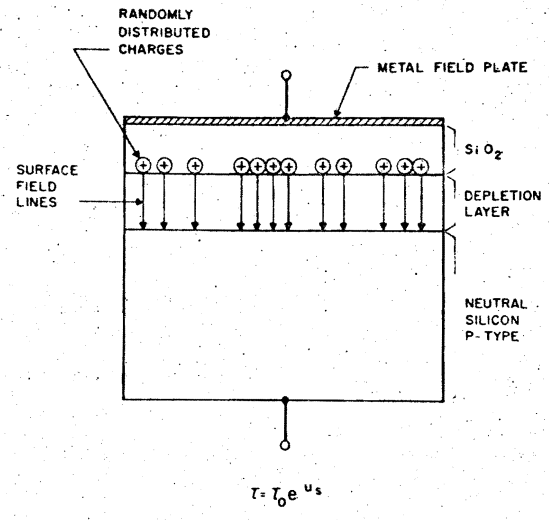


Fig. 2: Randomly distributed charges at interface cause fluctuations of surface potential

dependent in surface potential u_s as shown at the bottom of Fig. 2.

3. ENERGY DISTRIBUTION OF SURFACE STATES AND CAPTURE CROSS SECTIONS

About distribution of surface states densities the following facts are known: (i) surface state density is lowest around the middle of the gap and increase strongly towards the band edges. (ii) Although surface state densities can vary over many orders of magnitude dependent on oxidation technique, annealing, crystal orientation etc. this general shape remains unchanged. (iii) Very often smaller peaks emerge at certain energies from the broad distribution. The features just mentioned are illustrated in Fig. 3 (ref 5). It should be noted that the sample of Fig. 3 was made

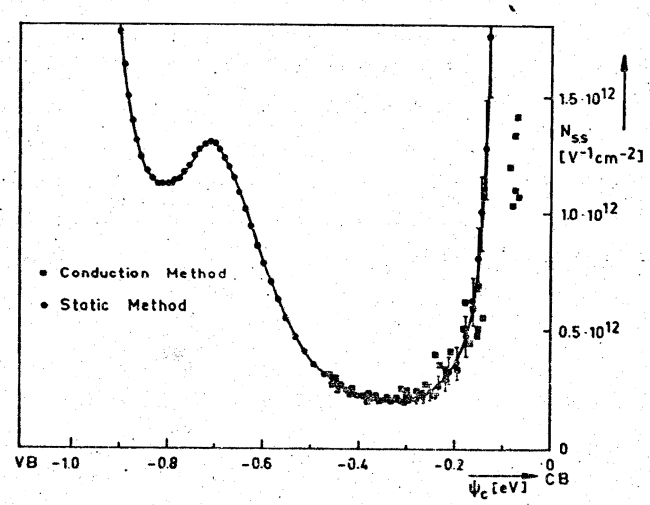


Fig. 3: Typical distribution of interface states across bandgap of silicon.

on < 111 > silicon and under conditions giving a high surface state density. This was necessary because samples made with the best technology have such a low surface state density that their distribution is very hard to measure. The following relevant features are observed in this curve: (i) The minimal surface state density is in the upper half of the gap. (ii) There is a peak at 0.74 eV from the conduction band. (iii) Interface state density is higher towards the valence band edge than towards the conduction band edge. Although only few such extensive measurements are known it seems that those features are quite common. The small peak in the lower half of the gap is quite likely caused by some common impurity or structural defect. Nothing can be said about the origin of the other features. For a long time it was believed that surface state densities go down towards the band edges as illustrated in Fig. 4 (ref 6). It has now become apparent that this drop may have been an artifact of the measurement. The drop towards the band edges is only observed if the

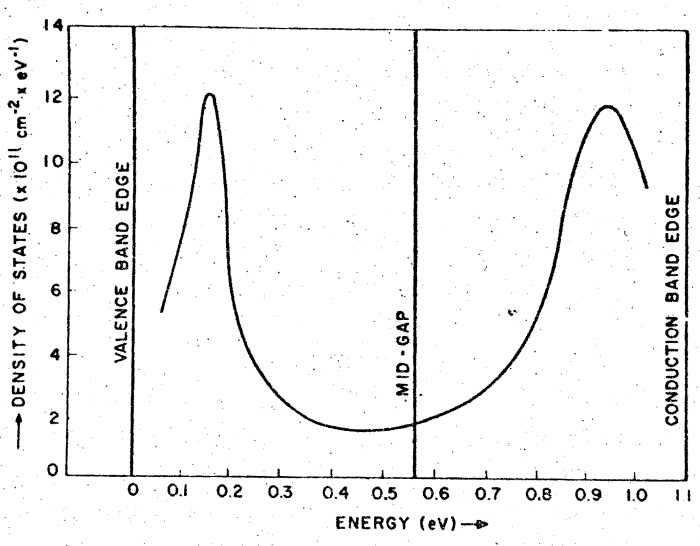


Fig. 4: Surface state density at band edges as measured by Gray-Brown technique

Gray-Brown Technique (ref. 7) is used. Boudry (ref 8) has shown that an increasing surface state distributing in conjunction with a decreasing capture cross section can result in a very low apparent surface state density if the Gray-Brown Technique is used. Other measurement techniques which have since been developed all show a continously increasing surface state density close to the band edges.

Utilizing the conductance technique mentioned above the majority carrier capture cross sections can also be determined. Majority carrier cross section means that electron capture cross sections in upper half of the gap can be obtained in n-type material and vice versa. Such results are seen in Fig. 5 (ref 9). Electron capture cross sections tend to very low values towards the conduction band. Hole capture cross sections on the other side do not show this behavior. Some care should be excercised

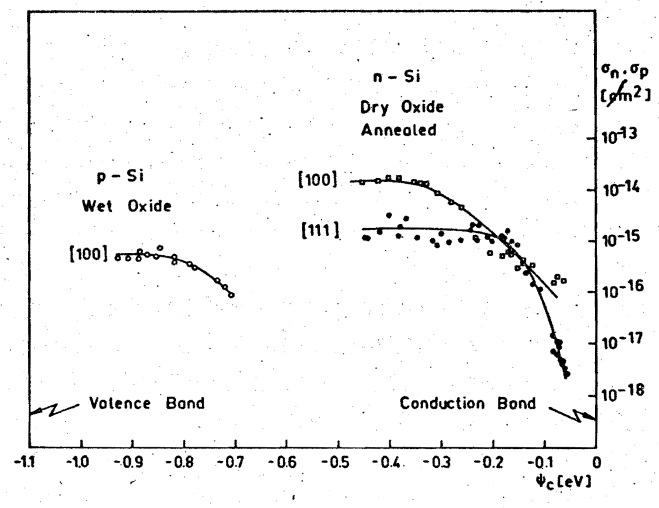


Fig. 5: Capture cross sections for interface states as obtained by conductance technique

in interpreting the hole capture cross sections because they may be associated with the impurity peak of Fig. 3 and not with the general background surface state levels.

4. SURFACE STATE MODELS

Although a thorough understanding of surface states is still lacking, it appears likely now that surface state phenomena cannot be attributed to one single common cause. There are probably at least three sources for surface states, namely structural imperfections, charges in the oxide and chemical impurities also microcracks (not present in epitaxial layers)

The importance of the structure of the interface can best be seen by the extreme sensitivity of interface state density against annealing conditions. If an oxide is grown in dry oxygen surface state density is high. It can be reduced drastically either by high temperature annealing in inert ambients or by low temperature annealing in hydrogen or water vapor. One can only speculate about the chemical reactions going on at the interface. One fact has been established, namely that hydrogen is only effective when present as atomic hydrogen (ref 10). Another possible reason for interface states are charges in the oxide. It can be concluded from rather basic quantum mechanical concepts that the potential well of a charge in the oxide should act as a trap for the opposite type of charge (ref 6).

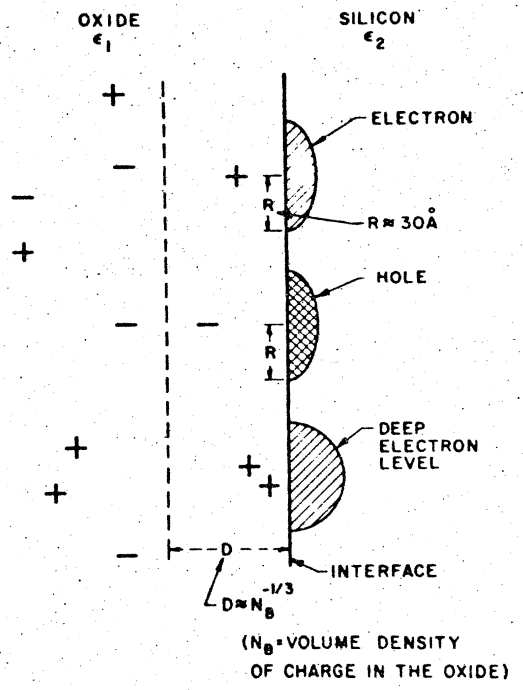
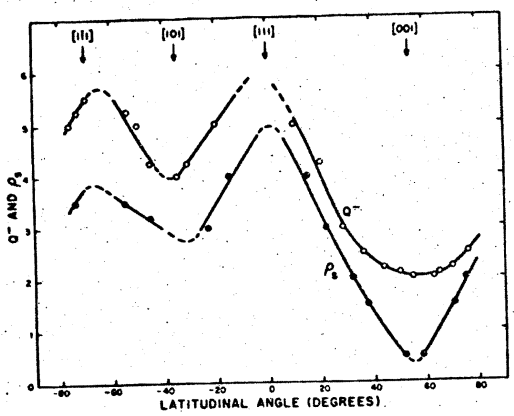


Fig. 6: Schematic diagram of correlation between surface states and surface charge

A single charge should cause a shallow level around 0.1 eV for electrons. Double charges within the radius of an electron wave function should give a level at four times this energy, e.g. around midgap. Statistical phenomena might very well smear out these effects to give continuous surface state distributions.

The body of experimental evidence linking surface charges and surface states is very extensive. Only one example is shown in Fig. 7 (ref 11) It shows the dependence of surface charge (Q) and surface state density ($\mathcal{S}_S$) on crystal orientations. The correlation of the two curves is quite evident. The third cause of surface states, chemical impurities has only recently been established (ref 12). Ion implantation has been used to implant various chemical elements into the Si-SiO_2 interface of an MOS structure. Fig. 8 shows the distribution of implanted ions. The samples are briefly annealed at 500°C to remove most of the radiation damage. For many different implanted elements clear, reproducible peaks can then be seen in the surface state distribution. From Fig. 8 it can be seen that every element having levels in the forbidden gap of silicon can cause a surface state level in the same energy range. If the penetration X_I of the ions is small compared to the width of the space charge layer W at a given surface potential the ions will be all at the same potential namely the surface potential. Most of the ions will on the other hand be far enough away from the surface to have their bulk properties. This means that in this manner bulk levels can be measured as surface states.



E. Arnold, J. Ladell, and G. Abowitz
Appl.Phys.Letters, 13, 413, (1968)

Fig. 7: Orientation dependence of interface charge and interface state density

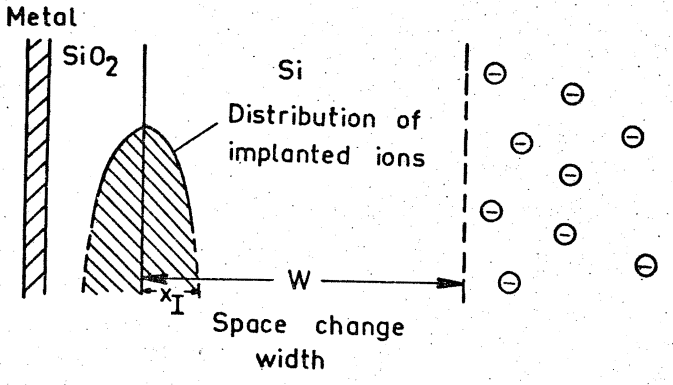


Fig. 8: Distribution of implantation in Si-SiO_2 interface.

Fig. 9 is a compilation of levels measured in this way. Many of the elements tested have a very low solubility in silicon and tend to accumulate at the interface. All these elements are especially likely to cause surface states when present as impurities. In those cases the ion incorporated directly into the interface will have an energy level different from that of the bulk because the oxide has a different dielectric constant. In the particular case of beryllium this phenomenon leads, after slight annealing, to a very sharp energy level (ref 13) (Fig. 10). This level has properties approaching those

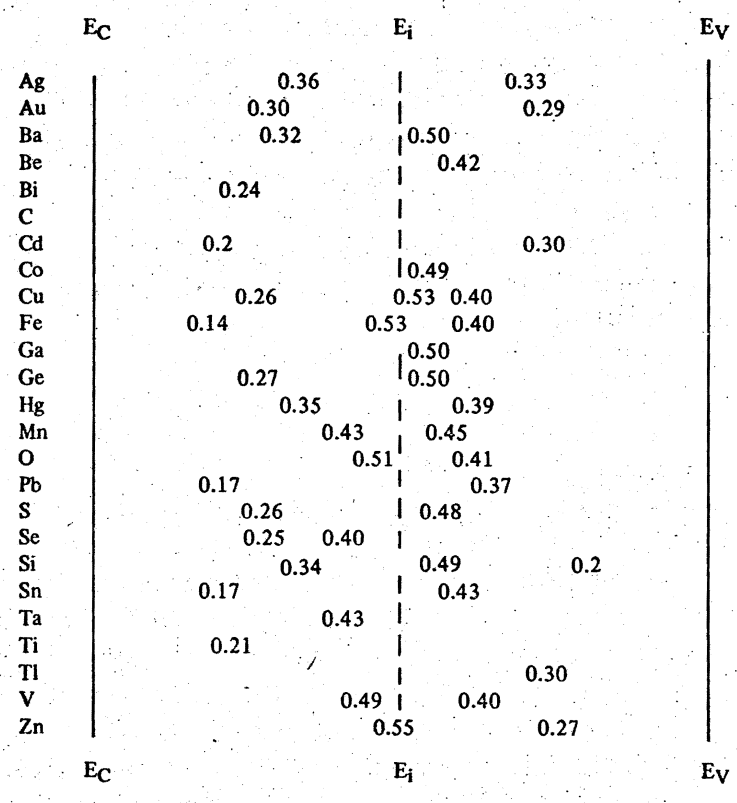


Fig. 9: Interface state levels for implanted impurites. Energy values are given in electron volts with respect to the conduction or valence band, respectively.

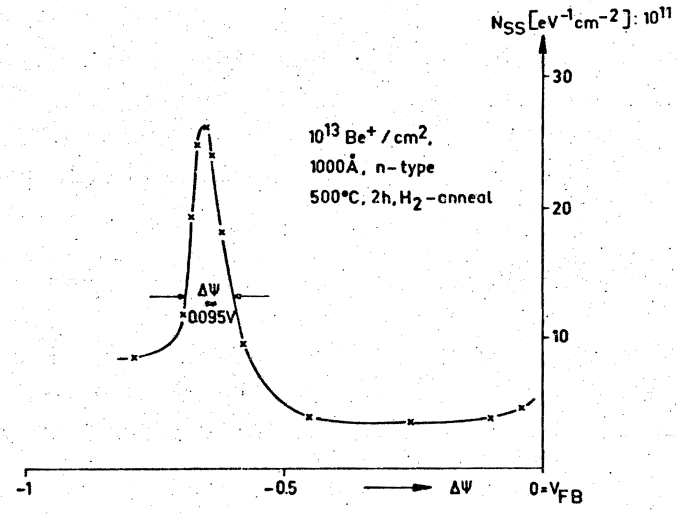


Fig. 10: Surface state peak due to implanted beryllium

but it serves as an example for the effects of many of the elements in Fig. 9.

In conjunction with surface state models a word should be said to the question whether surface states are really in the plane of the interface. A great many experiments show that the bulk of the states are indeed at the interface (ref 9) but there is also evidence that some fraction of the surface states are distributed within a thin layer of SiO_2 adjacent to the Si. In this case capure cross sections decrease exponentially with distance from the interface because the carriers interact with the states by tunneling (ref 14,15). This leads to very long time constants. The so-called tunneling states are too slow to respond to the usual surface state measurements but they can be recognized by a voltage hysteresis effect of the MOS characteristics.

5. PRACTICAL ASPECTS

It was mentioned above that surface state density is strongly dependent on oxidation technology. Today it is no longer a great problem to achieve extremely low surface state densities. Requirements are very clean processing and furnaces. Particularly alkali metals have to be kept away from the surface. For oxidation furnaces double wall quartz tubes or tubes from polycrystalline silicon are recommended. The oxidation has to be carried out under very dry oxygen. This results in a very high surface state density which is, however, readily reduced by annealing either at elevated temperature around $1000^{\circ}C$ in inert ambient (He, N_2, H_2) or by annealing in an ambient containing hydrogen around $400^{\circ}C$. This last step is mostly sufficient particularly since it is the only annealing step that can be carried out with aluminium contacts in place. Contact evaporation usually has a deteriorating effect on interfaces. This is particularly so for electron gun evaporation which is accompanied by radiation damage but even normal filament evaporation increases surface density. Low temperature annealing restores a very low density of states.

Using the best available techniques it is possible today to obtain densities of around $10^{10}\ cm^{-2}$ in the middle of the gap (ref 16,17). This corresponds to one surface state per 10^4 silicon atoms in the surface. It is obvious that the ideal $Si\text{-}SiO_2$ interface which should be without surface state (ref 18) is practically achieved.

Under normal operating conditions surface state densities do not change in devices. The two conditions which increase surface state densities are energetic radiation of all kinds and high electric field particularly in conjunction with elevated temperature. Radiation phenomena are too complex to be discussed in this contect but some results on stress aging will be given here.

It has been found that application of negative bias increases surface state densities (ref 19). At room temperature voltages have to be close to breakdown voltage to cause any appreciable effect but at a temperature of $300^{\circ}C$ and application of a field of $10^6\ V/cm$ for 30 min pronounced effects occur. In Fig. 11 surface state density of an n and a p-type sample before and after this stress is shown. Densities before stress

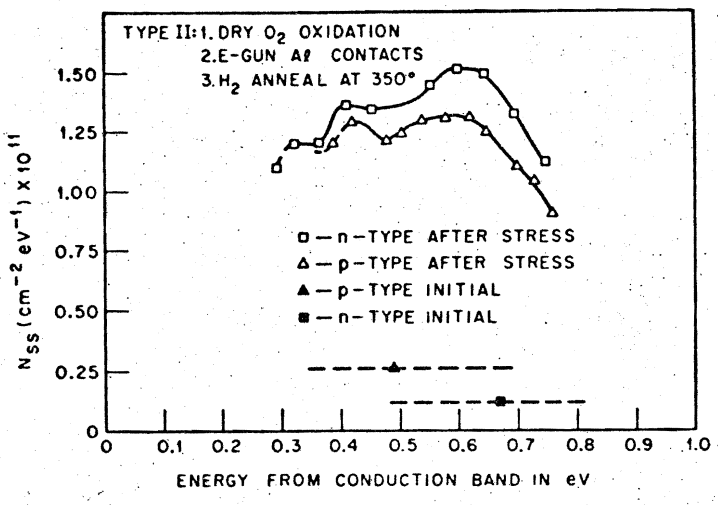


Fig. 11: Effect of negative bias stress (10^6 V/cm and 360°C) on surface state density.

are very low and only one point is shown in the lower part of the graph. After stress under the conditions given above surface state densities are about 10 times higher in the n-type sample. It is remarkable that the structure of the stressed curve is very similar for n- and p-type. This structure differs for various oxidation and contacting procedures but is quite reproducible if conditions are kept constant. It would be premature to speculate about the reasons for this behavior.

Since oxides made in different ways behave differently in this stress recommendations can be made for optimum stability. It appears that the most stable oxides are those consisting of a double layer SiO_2 + Al_2O_3. The worst are steam oxides.

CONCLUSION

Surface states are not yet theoretically fully understood but technologically well under control. The fact that surface states can be reduced beyond detection has diminished practical interest in this phenomenon. In the field of CCD's surface state properties at the band edges are of great importance. It seems that in this regions densities become very high while capture cross sections at least for electron become very low.

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