NUMERICAL AND ANALYTICAL STUDY OF CCD OPERATION

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ABSTRACT

The results of a theoretical study of the electrostatic and dynamics of overlapping gate CCD's is presented. Both buried channel and surface channel CCD's are included. Numerical results based upon an accurate approximation to the charge transfer efficiency including in the case of surface channel an estimate of surface state losses are presented for a number of different clocking schemes. The charge transfer process is shown to divide into three distinct stages. In the first stage, the charge confined under the storage gate spreads itself according to the rapidly changing clock voltages and supplies charge to "wet" the area under the transfer gate. During the second stage, the charge transfer occurs in a manner analogous to the operation of a surface or buried channel IGFET. The storage electrodes act as source and drain, and the transfer electrode acts as the control gate. In the final stage, the charge transfer process is characterised by transfer of charge from under the storage gate by combined process of diffusion and fringing field induced decay.

A simple capacitance network model for the electrostatics and optimal doping profiles for the buried channel CCD are described. Analytic approximations to the various stages of the charge transfer dynamics are given in summary and compared with the detailed numerical results.

Preliminary results of the electrostatic analysis of the recently proposed buried channel structure using Schottky barriers on GaAs are presented.

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