A COMPARISON OF CCD ANALOG INPUT CIRCUIT CHARACTERISTICS

H. Wallinga[x]

Abstract: The electrical input section of a surface CCD usually consists of a diffused region with two adjacent gates. In this paper, different control modes of such an input circuit are investigated both theoretically and experimentally. On account of the required linearity of the introduced charge packet with the input signal and the desire of minimum complexity of the control circuits a choice can be made among the different configurations of the input section. The most promising input control modes are studied in detail. The different modes are compared to each other with respect to relevant properties.

I INTRODUCTION

In analog signal processing applications, the CCD operates with discrete analog charge packets. The amounts of charge contained in the charge packets represents samples of the input signal. The charge packets are introduced into the first stage of the CCD by the electrical input section (ref. 1).

In the delay section of the CCD, the charge packets are shifted along the interface by applying appropriate gate pulses (ref. 2,3).

Finally in the output section, the charge packets are translated into a signal that can be processed by ordinary electronic circuits. That means, that the amount of charge in the charge packet is translated in a current or voltage (ref. 4). The sections are indicated in fig. 2.

The purpose of the analog input section is to transform the magnitude of an input signal into the magnitude of a charge packet. Probably due to the large effort in image sensing applications of CCD's, little has been published about the characteristics of electrical input sections.

In this paper a number of ways to control the electrical input circuit is investigated. In section II, the function of the input circuit is described in terms of a sampling circuit, and its different possible approaches are mentioned. In section III, the actual input configuration is described and related to the basic sampling circuits. In section IV, the merits and demerits of the various input control methods are considered, and in section V, the conclusions are summarized.

[x] Twente University of Technology, Department of Electrical Engineering, P.O.Box 217, Enschede, The Netherlands.

II THE SAMPLING CIRCUIT

The input circuit of a CCD is basically a sample and hold circuit. A signal source is sampled and the samples are stored on a hold capacitor. The main difference with conventional sample and hold circuits is, that here the information is stored as an amount of charge, rather than as a voltage, on a hold capacitor. This leads to various approaches for the sampling circuit. In fig. 1 three different basic circuits have been represented. The three configurations are referred to in this paper as SHC1, SHC2 and SHC3.

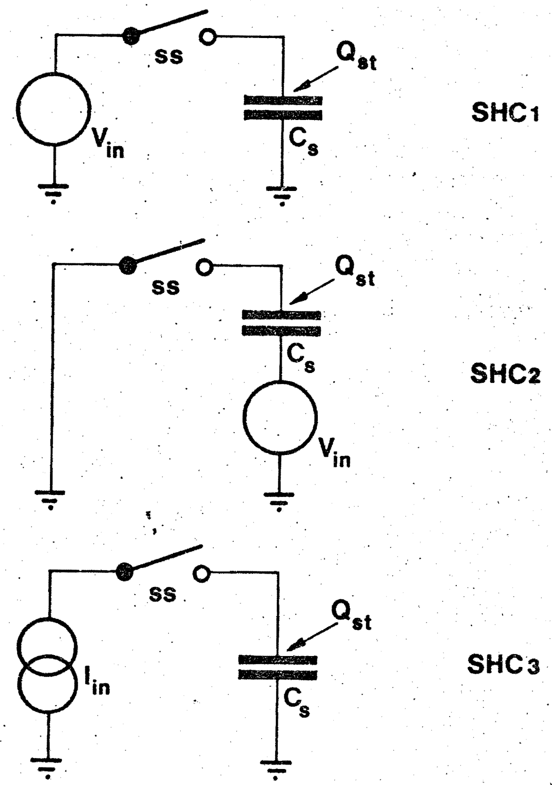


Fig. 1
Basic sample and hold circuit configurations

V_{in} = voltage source = V_s

I_{in} = current source = I_s

C_s = storage capacitance

ss = sampling switch

Q_{st} = stored charge

t_a = aperture time

SHC1 : $Q_{st} = V_{in}.C_s$

SHC2 : $Q_{st} = -V_{in}.C_s$

SHC3 : $Q_{st} = t_a.I_{in}$

In SHC1 and SHC2 the stored charge Q_{st} is a linear function of the voltage V_{in}, provided that C_s is constant. In the circuit SHC3, the stored charge is a linear function of I_s if the sampling time t_a is constant, or a linear function of t_a if I_s is constant.

III THE ACTUAL INPUT CIRCUIT

Theory and measurements have been performed on a 4-phase CCD with overlapping gate electrodes. The input section consists of a diffused region with two adjacent gates. Every input electrode can be separately controlled. The delay section is 16-bits (64 gates) long. The output section consists of a floating diffused region, which is connected to a reset MOST and to the gate of an output MOST. See fig. 2.

The lower level gates are in poly Silicon, the upper level gates are in Aluminium. There are additionally teststructures on the same chip. The technological parameters are listed in table I. A photograph of the device is shown at the final page of this paper.

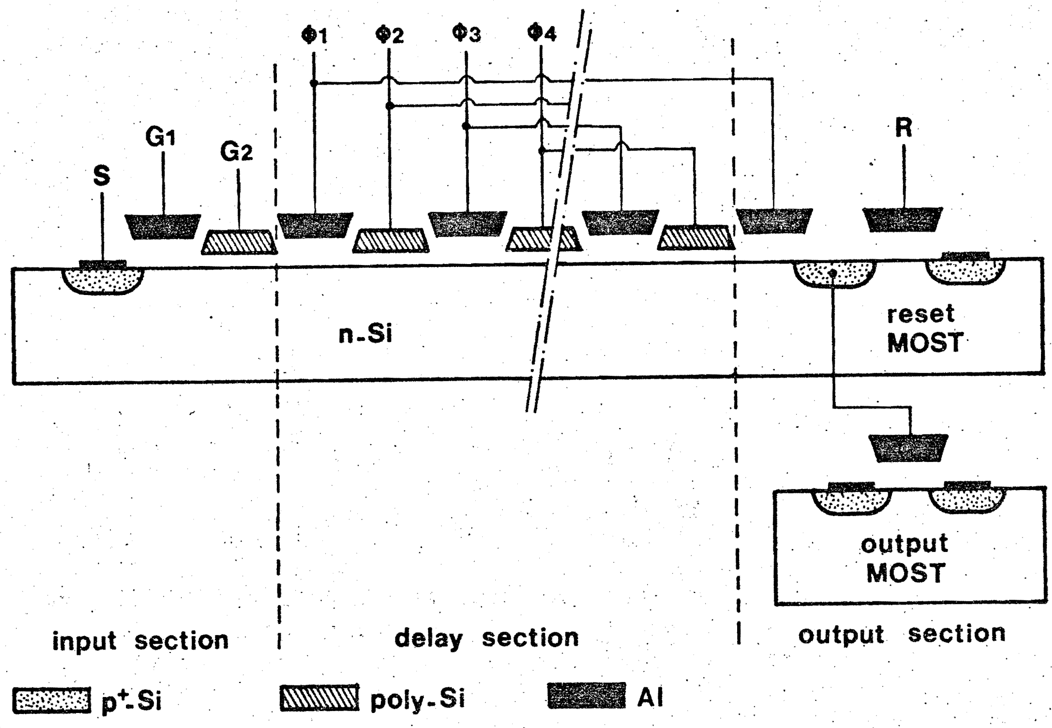


Fig. 2. Cross-sectional view of the CCD

Table I. The technological parameters of the CCD P 7405 A.ˣ

	upper level gates	lower level gates	Units
oxide thickness	$d_1 = 0.18$	$d_2 = 0.10$	μm
oxide capacitance	$C_{ox1} = 1.88\ 10^{-8}$	$C_{ox2} = 3.4\ 10^{-8}$	$F\ cm^{-2}$
gate material	Al	Poly Si	
turn-on voltage	$V_{T1}(0) = -0.8$	$V_{T2}(0) = -2.1$	V
gate length	$L_1 = 13.5$	$L_2 = 11.5$	μm
gate area	$A_1 = 3.4\ 10^{-5}$	$A_2 = 2.8\ 10^{-5}$	cm^2

ˣThe substrate is n-Si with a Phosphorus dope concentration of $N_D = 5.10^{14}\ cm^{-3}$.

Fig. 3 shows the relation between the turn-on gate voltage V_T and the related diffused region voltage V_S for the lower and upper level gates.

From fig. 3 the charge density in an inversion layer can be determined graphically, with the aid of equations (1) and (2) as will be seen later on in this section.

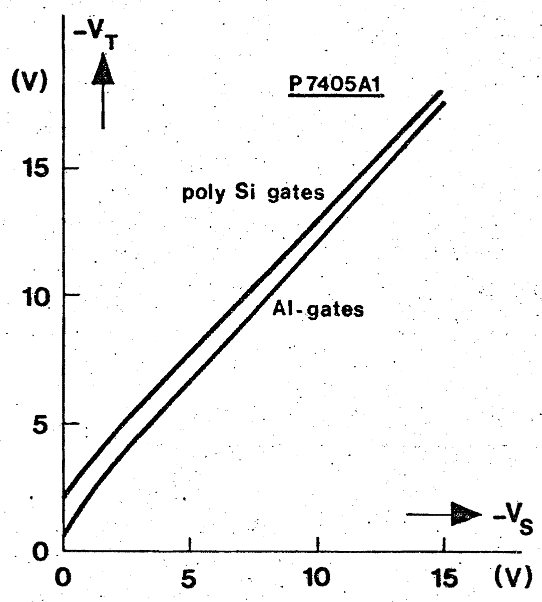


Fig. 3. The turn-on gate voltage V_T as a function of the diffused region voltage V_S, as obtained by MOST channel conduction measurements.

Let us now examine the input section, with the electrodes S, G1 and G2 (fig. 2). The purpose of the input circuit is to determine a fixed amount of inversion charge below the second gate G2. The hold capacitor here consists of the oxide capacitance $A_2\ C_{ox2}$ in parallel with the depletion layer capacitance $A_2\ C_{dep}$, where C_{dep} is the depletion layer capacitance per unit area. When the surface potential below G2 equals the external applied voltage V_S, the stored charge Q_{st} below G2 is

$$Q_{st} = A_2\ C_{ox2}\ \left(-\ V_{G2} + V_{T2}(V_S)\right) \qquad (1)$$

From this equation, it is clear that both S and G2 may be used as a signal input electrode. The switch function is then provided by a sample pulse on G1. In this way 2 different control modes are possible, which will be described in section IV, as the methods A and B respectively. A is of the type SHC1 and B of the type SHC2 (fig. 1).

The surface potential below G2 may also be controlled by the voltage V_{G1} of G1. Therefore first the inversion layer below G2 has to be charged by switching V_S to a sufficiently low negative value, and afterwards to a high negative potential. Now S functions as the drain and the inversion layer below G2 as a capacitively loaded source of a source follower. The surface potential of the inversion layer will equal the diffused region saturation voltage $V_{sat1}(V_{G1})$, which is a function of V_{G1} (fig. 3).

The stored charge below G2 is then

$$Q_{st} = A_2\ C_{ox2}\ \left(-\ V_{G2} + V_{sat1}(V_{G1})\right)V_{t2} \qquad (2)$$

Here the sample pulse is applied to S and the signal voltage may be applied to either G1 or G2. These modes are described as the methods C and D in section IV. C is of the type SHC1, while D is of the type SHC2.

The input circuit is of the type SHC3, if V_{G1} acts as a gate voltage of a MOST in the saturation mode with S as source and the inversion layer below G2 as drain. This is the case when the surface potential below G2 has a suffuciently negative value. The stored charge is now

$$Q_{st} = t_a . I_s \qquad (3)$$

where t_a is the aperture time, during which the current flows and I_s is the saturated MOST current. I_s may be controlled by either the electrodes S or G1. I_s obeys the well known squared saturated MOST current law, and because a linear characteristic is one of the requirements, this control method is not considered in detail within this paper.

IV INPUT CIRCUIT PROPERTIES

In this section the merits and demerits of the various input control modes are investigated. The control modes have been mentioned and appointed as A, B, C and D in section III. They are summarized in table II.

Table II. Summary of the various control modes.

applied signal \ control mode	A	B	C	D
signal voltage	S	-	G1	-
signal pulse	-	G2	-	G2
sample pulse	G1	G1	S	S
constant voltage	-	S	-	G1
control pulse	G2	-	G2	-
sample and hold type (fig.1)	SHC1	SHC2	SHC1	SHC2

The requirements for an electrical input circuit are:
- linear dependence of introduced charge packet on input signal
- short time constant
- sharply defined aperture time
- high dynamic range
- simple external control circuitry.

If the geometry of the input section of the CCD is of the same order of magnitude as the CCD delay stages, both the time constant and dynamic range will be limited by the delay section of the CCD (ref. 5). Therefore these properties will be only important for special purposes. For instance if signal processing is performed within the input section, an extremely short time constant may be important and current source modes have to be investigated.

Here we shall emphasize the linearity, the aperture time definition and the simplicity of the control circuitry. The latter appears roughly from table II, if we recall that directly applied signal voltages require less complex circuitry than pulsed signal voltages. So with respect to the simplicity of the external control, methods A and C are in favour.

The linearity of the input circuit is best examined by the variation dQ_{st}/dV_{in} of the sampled charge packet with the input signal. The aperture time should be within well defined time marks. In the following we discuss those aspects for the various control modes:

-A Differentiation of eq. (1) with respect to the input signal voltage V_S gives

$$\frac{dQ_{st}}{dV_S} = A_2\, C_{ox2}\, \frac{dV_{T2}}{dV_S} \tag{4}$$

which leads to

$$\frac{dQ_{st}}{dV_S} = A_2\, (C_{ox2} + C_{dep}) \tag{5}$$

This is expected because the capacitance of the inversion layer below G2 is the parallel capacitance of oxide and depletion layer capacitances. C_{dep} is voltage dependent and it disturbs the linearity. However, if like here, C_{ox2} is larger than C_{dep}, so if the oxide is thin, the bulk dope concentration is low and if a reverse bias is applied, dQ_{st}/dV_S is constant within a few percent. This is also obvious from equation (4) and fig. 3.

A more important distortion is caused by the following complication. When the gate G1 is switched off, the channel will discharge to the source and drain. On the capacitively loaded drain, the extra charge is added to the signal charge. This error is the more serious because the division of charge between the source and the drain storage node depends in a non-linear way on both the rise time of the trailing edge of the pulse on G1, and the original channel charge (ref. 5,6). Fig. 4 shows the introduced charge as a function of the input voltage for three different slopes of the trailing edge of the sampling pulse on G1.

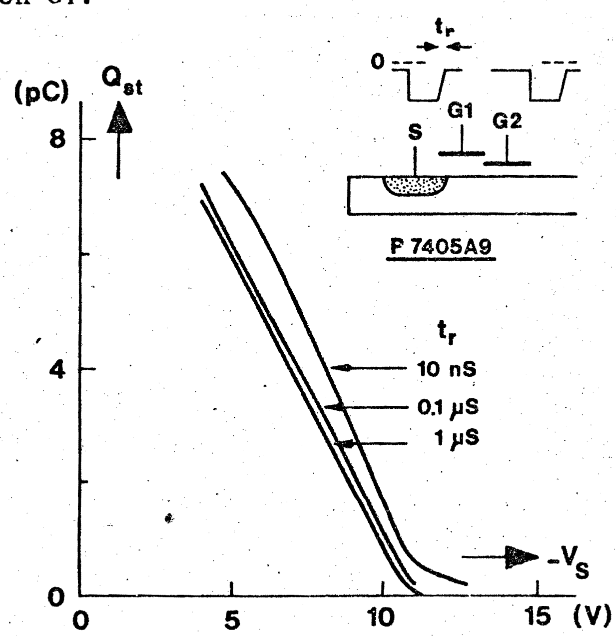


Fig. 4. Experimental results obtained with control mode A. The input signal is applied to the diffused region S. Sampling occurs at the gate G1. The rise time t_r of the trailing edge of the sampling pulse is a parameter.

-B In this mode differentiation of (1) leads to

$$\frac{dQ_{st}}{dV_{G2}} = - A_2 C_{ox2} \tag{6}$$

This promises a linear characteristic. Although the switching-off of G1 disturbs the stored charge also described above in A. This error is not voltage dependent because the channel charge below G1 is independent of the signal voltage. This is the advantage of the sample hold circuit SHC2.

The disadvantage is that the input signal has to be pulsed, or chopped on G2. This can be avoided, if a large dynamic range is not required. In that case the constant applied signal voltage V_{G2} should be small enough to allow complete charge transfer towards the first delay gate of the CCD during pulse ϕ_1 (fig. 2).

-C In the modes C and D the sampled charge obeys equation (2). Differentiation gives in mode C:

$$\frac{dQ_{st}}{dV_{G1}} = A_2\ C_{ox2}\ \frac{dV_{T2}\left(V_{sat1}(V_{G1})\right)}{dV_{G1}} \tag{7}$$

which leads to

$$\frac{dQ_{st}}{dV_{G2}} = A_2\ C_{ox1}\ \frac{C_{ox2} + C_{dep}}{C_{ox1} + C_{dep}} \tag{8}$$

So the deviation from linearity depends on the difference between C_{ox1} and C_{ox2}. Equal oxide capacitances provide linearity. There are no problems with the switching off of the sample pulse. Experimental results are shown in fig. 5.

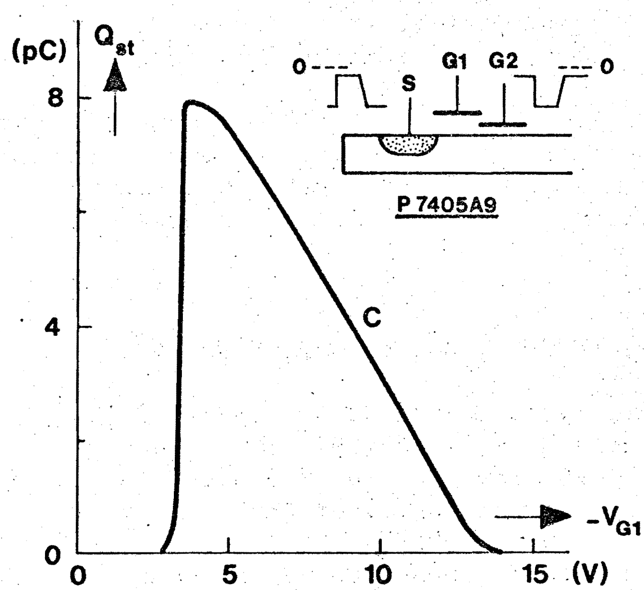


Fig. 5. Experimental results obtained with control mode C. The input signal is applied to G1. Sampling occurs at the diffused region S. In the part with positive slope the input is in the current mode.

The disadvantage of this method is that the aperture time is not defined sharply. When in the store mode $|V_{G1}|$ increases, Q_{st} will increase, due to the source follower action. Decrease of $|V_{G1}|$ has no influence on Q_{st}. This means that the sampled charge will be a function of the most negative value of V_{G1} within the hold time, that is the time between the trailing edge of the sample pulse and the trailing edge of V_{G2}.

-D In mode D, the variation of the stored charge with the input channel is just like in method B, eq. (6). So the linearity is very good. This mode has the same disadvantage as mode B with respect to the complexity of the external control, and the disadvantage of mode C with respect to the aperture time.

Although the control modes are described separately, it is obvious that mixed control is possible. For instance, the control modes C and D may be applied simultaneously, which causes an analog add or substract function, as follows from eq. (2).

V CONCLUSIONS

The merits of a number of control modes of the input section of a 4-phase CCD have been investigated. In table III the properties are summarized.

Table III. Review of input control modes.

property \ control mode	A	B	C	D
linearity	−	+	□	+
aperture time definition	+	+	−	−
simplicity of control	+	−	+	−
high frequency properties	−	□	□	□

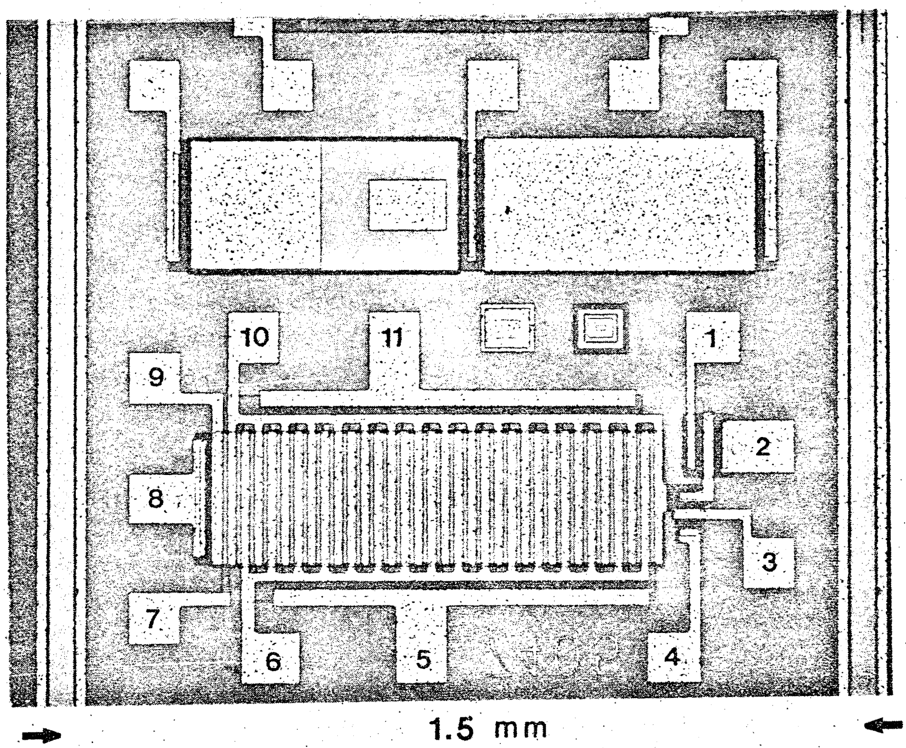
\+ good □ fair − poor

It depends on the application, which properties are crucial. With the aid of table III a proper choice among the various control models can be made.

Acknowledgements: The author likes to thank A. Kooy for the preparation of the devices, O.W. Memelink for his support and the other members of the Solid-State Electronics Group for their help and interest in this work.

References:

1. M.F. Tompsett and E.J. Zimany, IEEE, J. Solid-State Circuits, Sc-8, 151 (1973).
2. W.S. Boyle and G.E. Smith, Bell Syst. Techn. J. 49, 587 (1970).
3. M.F. Tompsett, J. Vac. Sci. Technol. 9, 1166 (1972).
4. W.F. Kosonocky and J.E. Carnes, RCA Rev. 34, 164 (1973).
5. J.L.M. van Ruyven, Internal Rep., Twente Univ. of Techn., Doct. Verslag, Kenm. 1217.1303, (1974).
6. F.G. Jonkman, Internal Rep. (in Dutch), Twente Univ. of Techn., Bacc. Verslag, Kenm. 1217.1025, (1973).



Photograph of the CCD P 7405, and the test MOS transistors.

1, 2 source and drain of output MOST
3 reset gate
4 drain of reset MOST
5,11 poly-Si gates
6,10 Al gates
7 second input gate G2 (poly-Si)
8 input diffused region S
9 first input gate G1 (Al)