USING CHARGE-COUPLED DEVICES FOR ANALOG DELAY

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ABSTRACT. Some aspects of using CCD's for analog delay are discussed in this paper. In particular the effects of transfer inefficiency and the magnitude of transfer noise are presented. A simple solution to the problem of obtaining a linear, relatively noise-free input to the device is presented and experimentally demonstrated.

I. INTRODUCTION

One attractive field of application for charge-coupled devices (CCD) is that of analog delay.[1] In contrast to alternative approaches, the interface is compatible with integrated circuits and the amount of delay may be readily varied by changing the clock frequency. In addition, multiple taps may be introduced into the device. The object of this paper is to summarize ways of operating CCD's as analog delay lines and the performance that can be obtained from them.

Any single linear CCD acts as a sampling device that takes analog samples at the drive frequency f_0 of the device. If instantaneous samples are made then the theoretical reconstituted frequency response of the output would be flat up to $f_0/2$. In practice there is some finite width to the sampling window, but this will always be significantly less than the period of the drive frequency and the reduction in amplitude at a frequency of $f_0/2$. Since the delay is given by the number of elements N, the maximum ideal delay-bandwidth product of a CCD is given by N/2. This latter statement is true even if multiple charge transfer channels are organized in parallel.

II. EFFECTS OF TRANSFER INEFFICIENCY

In the nonideal case the effects of charge transfer inefficiency ε must be considered. These effects reduce the frequency response of the device from its theoretical value and introduce dispersion into the signal. In the case of a single linear channel the frequency response of a device in which there are n transfers is given by

$$R(f) = \exp\{-n\varepsilon[1-\cos(2\pi f/f_0)]\} \quad (1)$$

where f is the frequency of the input signal. This expression has been plotted[1] for different values of $n\varepsilon$. In many practical devices $n\varepsilon$ can be made less than 0.1 and negligible degradation is introduced from this source. If several transfer channels are used in parallel, then the drive frequency and the number of transfers undergone by each element of charge is reduced by the number p of channels. There are two major advantages in doing this since $n\varepsilon$ in each channel will be reduced by the factor p and the drive frequency will be reduced by the same amount. However, there are two potential disadvantages. One is that the drive frequency now becomes equal to or less than the maximum bandwidth and any pickup from the drive

frequency cannot be filtered out. In addition the frequency response for $n\varepsilon \neq 0$ would cause a frequency response minimum at half the drive frequency. This might be undesirable in some applications. However, with the small values of $\varepsilon(\sim 10^{-4})$ and signal amplification independent of drive frequency that can be obtained, the parallel approach is very attractive in terms of designing compact devices.

III. CHARGE INSERTION

One important aspect in using charge-coupled analog delay devices is that of inserting the charge into the device. Some attention has recently been given to obtaining a method of injecting the charge or sampling that is both linear and adds only a minimal noise component. Several methods have a low noise capability but a trick is required to give linearity over the whole dynamic range of the device.

The surface potential method of setting charge[2] will be described in the context of a surface channel device with a planar three-phase electrode structure using a separate input gate and input diode as shown in Fig. 1.

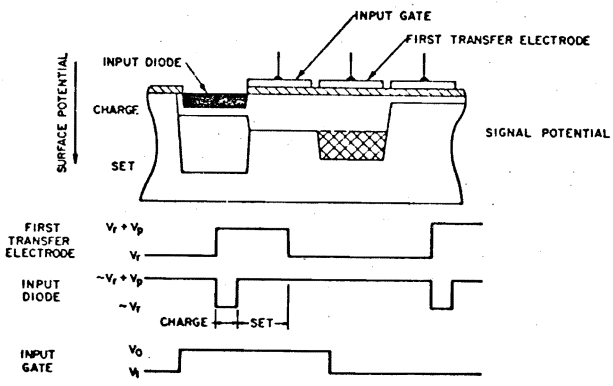

Fig. 1 Illustrating the surface potential method of setting charge in a CCD. Timing diagram is also shown.

The signal voltage is applied to the input gate and a special pulse is applied to the input diode. If the transfer electrodes pulse between voltages of V_r and $V_r + V_p$, then the signal voltage must lie in this range. When the first transfer electrode is pulsed on, the input diode must be at a low value so that charge flows under the input gate and the first transfer electrode. The input diode is then reverse biased and excess charge flows out until the surface potential underneath the first transfer electrode is equal to the surface potential underneath the depleted input gate. Hence the voltage on the input gate controls the amount of charge held back under the first transfer electrode. This charge is then transferred along the device.

The linearity of the relationship between signal charge set by this method and the voltage on the input gate is intuitively obvious but may be easily verified in the following way. The surface potential ϕ_s under an MOS electrode biased into inversion is given by

$$\phi_s = V_0 + V - \left(V_0^2 + 2VV_0\right)^{1/2} \quad (2)$$

where

$$V = V_G - V_{FB} - q_0/C_0, \quad V_0 = \frac{\varepsilon_s q N_B}{C_0^2}$$

V_G = voltage applied to electrode

V_{FB} = flatband voltage

q_0 = density of inversion charge

C_0 = capacitance per unit area of electrode

ε_s = dielectric constant of silicon

q = electronic charge

N_B = substrate doping

The condition that defines the magnitude of the charge under the first electrode is that the surface potential

under the input gate with $q_0 = 0$, should equal the surface potential under the first transfer electrode with $q_0 = \frac{Q_s}{A}$, where Q_s is the size of the charge packet and A is the storage area of the electrode. If for the first transfer electrode $V_G = V_R + V_P$ and for the input gate $V_G = V_R + V_P - V_S$, then writing the above condition using Eq. (2) and cancelling the common terms gives

$$V_s = \frac{1}{AC_0} Q_s$$

i.e., V_s is now the input signal voltage which generates a directly proportional signal charge, and has a maximum permissible swing of V_p.

The timing diagram is shown on Fig. 1. Mostly the timing is not critical. The input diode may pulse low as soon as the first transfer electrode is low, but it must return to high sufficiently soon before the first transfer electrode goes low to allow an adequate set time. Preferably the set time would be several times the charge time, which can be as short as a few nanoseconds. The pulse applied to the second gate should go low shortly before the first transfer electrode goes low but after allowing adequate set time.

If an analog input is required, then the input signal is applied to the input gate and the device automatically samples the signal. In this mode of operation the sampling is slightly skewed, since if the voltage applied to the input gate during the period that the first transfer electrode is on, rises, then the input signal is effectively sampled at the end of the set period since the excess charge can flow out. However, if the input voltage falls in this period then it is effectively sampled at the beginning of the set period since no additional charge can flow into the potential well. Since the set time is relatively short compared to the period of the transfer pulses, this effect is small but could be eliminated with sample and hold in the input circuit if required.

IV. NOISE

There are primarily three sources of noise in a CCD used with electrical input. Input noise, transfer noise and amplifier noise. The uncertainty involved in setting the size of the charge packet under the first transfer electrode of area A and capacitance C_0/unit area is the input noise Q_s and is given[3] by

$$\overline{Q_s^2} = \frac{2}{3} kT\, AC_0 .$$

As an example of typical values, for an electrode with a large effective area A = 2000 μm^2 on 1000 Å thick silicon dioxide, the root mean square equivalent noise would be equivalent to approximately 300 electrons in a surface channel device. For a maximum value of V_s = 5 V, the number of electrons in a charge packet is 2×10^7 and the ratio of peak signal power to mean square noise generated at the input would be 86 dB.

Transfer noise is related to trapping effects that occur either at the interface or in the bulk as the charge packets move along the device. For a uniform density of interface states N_{SS} across the band, the frequency power spectrum S(f) of the transfer noise is given by

$$S(f) = \frac{4kT}{q} \ln(2) n f_0 A N_{SS} (1 - \cos 2\pi f/f_0).$$

In a surface channel device N_{SS} is approximately uniform across the bandgap and in good devices is 2×10^{10} cm^{-2} eV^{-1}. The amount of noise is also independent of the size of the charge packet.

As an example of typical values and using the same device parameters as before with $N_{SS} = 2 \times 10^{10}$ cm^{-2} eV^{-1}, after 200 transfers a peak signal to RMS noise ratio in a surface channel device of 66 dB can be expected.

The magnitude of amplification noise has been presented elsewhere and will not be discussed here.

V. EXPERIMENTAL RESULTS

The surface potential method of setting charge has been used with a 64-element surface channel CCD. The results of setting fat ZERO's and a group of ONE's are shown in Fig. 2(a). The transfer inefficiency

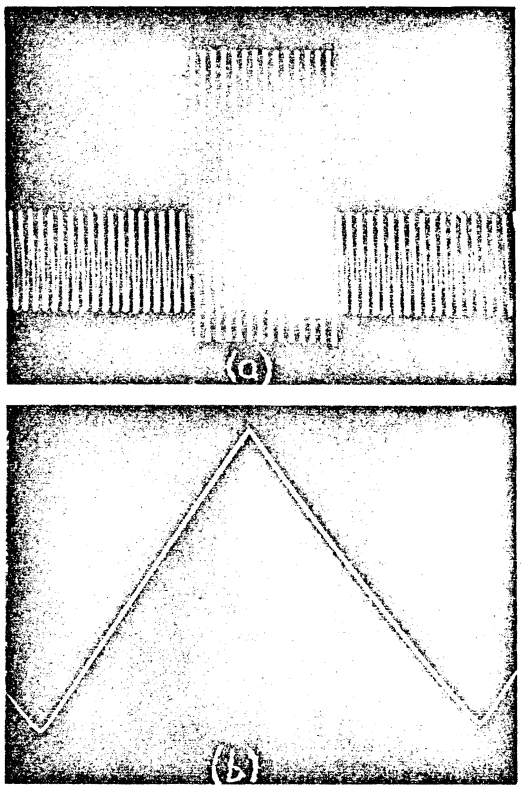

Fig. 2 Output signals obtained from a 64 element surface channel CCD using surface potential method of setting charge at the input.

of the device used is very low so that the transfer inefficiency product for the complete device is < 0.1, and the transition from all ZERO's to all ONE's and vice versa is seen to be very sharp.

The result of applying a triangular waveform to the input gate of the device is shown in Fig. 2(b). A filter has been used in the output circuit so that the individual current spikes are smoothed. In Fig. 2(b) the reproduction of the original waveform is seen to be extremely good. As an indication of the linearity of the complete system the harmonic distortion of a pure sinusoidal signal passed through the device was measured. The intensities of the second and third harmonics were both found to be 40 dB lower than that of the fundamental signal frequency. The amplitude of the transfer pulses used in the device was 15 V and the amplitude of the input signal was chosen to give half the maximum possible with full charge packets.

VI. DISCUSSION

It is now clear that CCD's have a role to play in obtaining analog delay, although the high frequency (> 10 MHz) and low frequency (< 1 kHz) ends of the spectrum have not been extensively explored yet. This paper is predominantly concerned with the problem of setting the signal level in the CCD and a simple, linear and relatively noise-free solution is proposed and demonstrated. The addition of transfer noise as the charges move along the device is also discussed and evaluated.

BIBLIOGRAPHY

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