An Electrically Programmable LSI Tranversal Filter for Discrete Analog Signal Processing (DASP)*

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ABSTRACT

This paper discusses the concept of discrete analog signal processing (DASP), to permit the realization of Fourier transformers, matched filters and correlators, and adaptive filters. The CCD shift register provides the analog delay function, the MNOS programmable non-volatile conductance is the analog weighted tap, and pulse sampling techniques minimize voltage drift and bias drift errors. We present a basic LSI building block, which combines CCD and MNOS technologies to provide an electrically programmable transversal filter. We discuss the fabrication and electrical characteristics of the basic cell in the filter, and preliminary measurements to demonstrate the feasibility of DASP.

*Supported in part by U.S. Army ECOM contract No. DAAB07-73-C-0337
W.B. Glendinning, technical officer

I. DISCRETE ANALOG SIGNAL PROCESSING (DASP)

The charge coupled device (CCD) and metal-nitride-oxide-silicon (MNOS) technologies may be combined to provide discrete analog signal processing (DASP) in contrast to conventional digital signal processing (DSP). In DASP, analog data samples are stored, transferred, and operated upon by analog means, whereas in DSP, digital or quantized samples are handled with binary logic. A major advantage of DSP is retained by DASP, namely the precise transport delay--particularly in relation to coherent processing. The dynamic range of an analog bit in DASP may be thought of as composed of 6 dB equivalent DSP digital bits. We have measured a 60-80 dB dynamic range in CCD, 2ϕ, shift-registers and transfer efficiencies in excess of 99.99 percent at mHz data rates.[1] For example, a 64 bit, 2ϕ CCD serial shift register will provide a minimum 60 dB dynamic range and an overall loss less than 1 percent at 1-2 mHz data rates, which is equivalent to 640 bits of digital shift-register memory. Thus, a signal charge analog packet can shift through typical CCD memory devices nearly unattenuated, limited by the size of the holding wells and the minimum detectable output signal. A gated charge integrator and on-chip electrometer amplifier with high g_m/C ratio provides a low-noise output signal[2] which may be double sampled in a bit time, to remove on-chip noise introduced by the reset gate.

There are three requirements in DASP:

a. a low-loss, non-dispersive, wide dynamic range analog delay line such as CCD's, with an electrically alterable delay

b. an accurate analog multiplier such as an electrically-programmable, non-volatile MNOS conductance

c. a method to compensate for offsets caused by voltage drift and bias errors. For example, the use of a reference signal in the CCD register and appropriate sample/hold techniques.

Random variations of either the CCD register tap gains or of the reference signal conductance matrix produce sidelobes in the filter bank. These errors add generally in a non-coherent manner and the effect of individual error is reduced by the correlation gain of the conductance matrix. For example, if the rms gain variation of individual conductances is 3 percent, and the correlation gain is 20 dB, then the average filter sidelobes (for filters far away from the signal frequency) will be 50 dB down. However, for certain combinations of signal frequencies and filters, the individual errors will add nearly coherently. Thus, the peak sidelobe will lie only about 30 dB down. A 3 percent rms overall accuracy appears to be very difficult to achieve on an open loop basis. We have selected an iterative procedure to electrically program a MNOS conductance to the nominal conductance valve, adjusted to the desired value based upon an input calibration signal, and the difference between the measured and calculated output signal. The combination of electrically programmable MNOS conductances and CCD delay lines will permit the realization of Fourier transformers, matched filters, correlators, and adaptive type filters.

II. A TRANSVERSAL FILTER BANK

The elements from two MOS technologies, a charge coupled shift-register and MNOS conductances, can be combined on a single substrate to perform signal processing functions such as a transversal filter bank which serves as a Fourier transformer/cross correlator to provide target identification functions. The signal processing complexity on a single chip may approach the equivalent of hundreds of convolution operations on waveforms which have hundreds of time samples, with only a single input and output analog signal connection. Although the computational accuracy falls short of the equivalent digital mechanizations (DSP), the elemental accuracy is

adequate for target identification functions. Figure 1 illustrates the DASP mechanization providing a discrete Fourier transform (DFT) and cross-correlator.

Signal time histories are transformed into a set of (usually orthogonal) descriptor coefficients. The descriptor coefficients are selected to represent descriptive qualities such as spectral amplitude rather than non-descriptive ones such as phase to classify the signal. The magnitude of the Fourier coefficients feed a second similar device, which correlates the descriptors of the received signal with a repertory of stored descriptors of known signals of interest. The results of this correlation are shifted to a detection algorithm, which determines the classification row with the highest correlation. A measure of confidence can be made based on the relative degree of correlation.

The preferred conceptual organization of the Fourier transformer/crosscorrelator shown in figure 1 makes use of basically the same device for both processing function. Briefly, the operation of each chip is as follows: signal data are shifted into the CCD SR (shift-register), and parallel delivered as voltages to the columns of a programmable conductance matrix. The row outputs from the conductance matrix represent the various filter or crosscorrelator responses, which are parallel loaded into a CCD SR for serial delivery from the chip. The two major advantages for this organization are:

a. On chip processing complexity is not limited by the number of input and output leads and their interface circuitry, since all signal I/O data is serially shifted.

b. The same basic chip design serves both the transform and the correlator functions.

The typical operation of the preferred chip design is describe below. With reference to figure 2, the filter is composed of (1) a serial input, parallel output analog shift-register 10, (2) a conductance matrix 12, wherein unique values of conductance are specified at each column-row intersection, (3) a parallel input serial output, analog shift-register 14, and (4) supporting circuitry, including electrical power, clock,

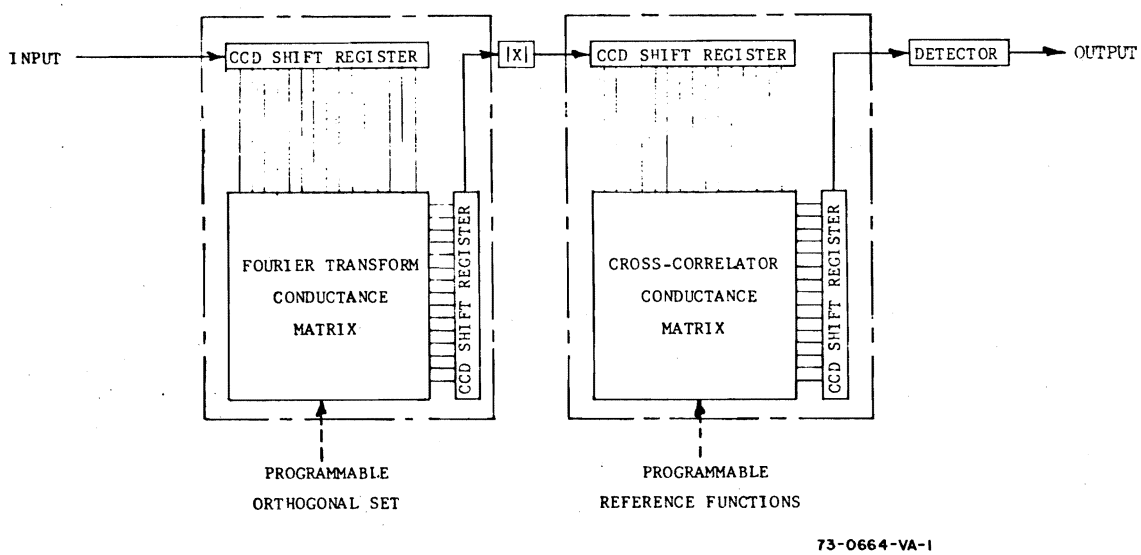

Figure 1. Organization of Processor

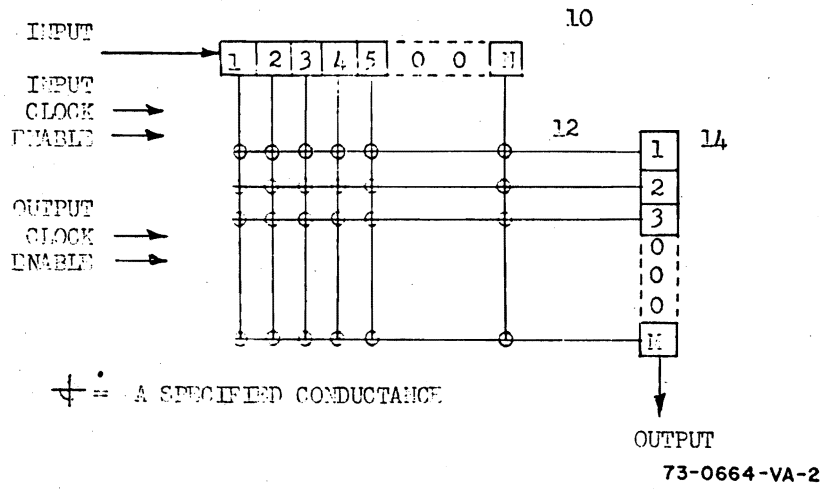

Figure 2. Sample Analog Filter Bank

and control. The shift-registers propagate a set of discrete electrical charges, one position for each clock cycle. Typical of these existing devices are the charge coupled devices capable of shifting analog signal samples over hundreds of storage cells at mHz rates.

The input shift-register is a serial load and parallel output which drives a set of matrix columns. The conductance pattern along each row is matched to a unique waveform such as a weighted sine wave, a phase coded signal, or any arbitrary waveform. The output of each row can be presented as

$$y_j = \sum_{i=1}^{N} a_{ji} x_i \text{ or simply } \underline{y} = A\underline{x} \quad (1)$$

where the conductance matrix A can represent, for example, a weighted discrete Fourier transform. The enable commands load the output shift-register stores with an electrical charge proportional to convolution output y_j, after which the enable is commanded false and the analog data y_j is serially shifted from the output register 14.

The device operation as described above performs a "block processing" function. The same organization can be arranged to perform a convolution operation as well. The convolution operation is described mathematically as

$$y_{ji} = \sum_{h=1}^{N} a_{jh} x_{i-h+1} \quad (2)$$

which is a function of real time. In other words, a useable output occurs on all rows after each data shift in the register occurs, for each input clock. The output from a single row can be delivered through the output SR simply by enabling only the desired output line. The device output circuitry can be designed also to deliver multiple outputs, subject to constraints on package lead count and chip area available for the additional output interface circuitry. Such a device would be useful, for example,

in a system requiring a matched filter for an arbitrary waveform having a wide range of possible doppler shifts. These conditions, however, are somewhat rare, because systems are generally designed to avoid the need for highly redundant processing.

III. A HYBRID DASP MECHANIZATION

Figure 3 shows a block diagram of an analog processor that is well within the reach of present technology. The input signal is passed through a filter that cuts off sharply at 20 kHz and is then sampled at a 60 kHz rate. Input signals at frequencies lower than 40 kHz will produce no aliases. The filter must have sufficient rejection at 40 kHz and beyond to reject aliases by the desired amount. N samples of the input signal are stored in the CCD delay line. The Fourier transform conductance matrix provides sin and cos weightings of these samples and forms N sums corresponding to the complex outputs of N/2 filters. The complex outputs are amplitude-detected and correlated with the desired replica in the cross correlation conductance matrix. Offsets will be introduced at each stage of the CCD delay line. These offsets can be determined by grounding the input and shifting out the data stored in the CCD register. The filter outputs (complex) correspond to the components produced by the offsets. These values are stored on capacitors and subtracted from the outputs produced under the signal conditions.

A more detailed look at the conductance matrix and associated circuitry is shown in figure 4. (More than 16 CCD cells would be required in a practical system). Each of the 16 I or Q (real or imaginary) outputs is the weighted sum of the 16 input samples, X_n.

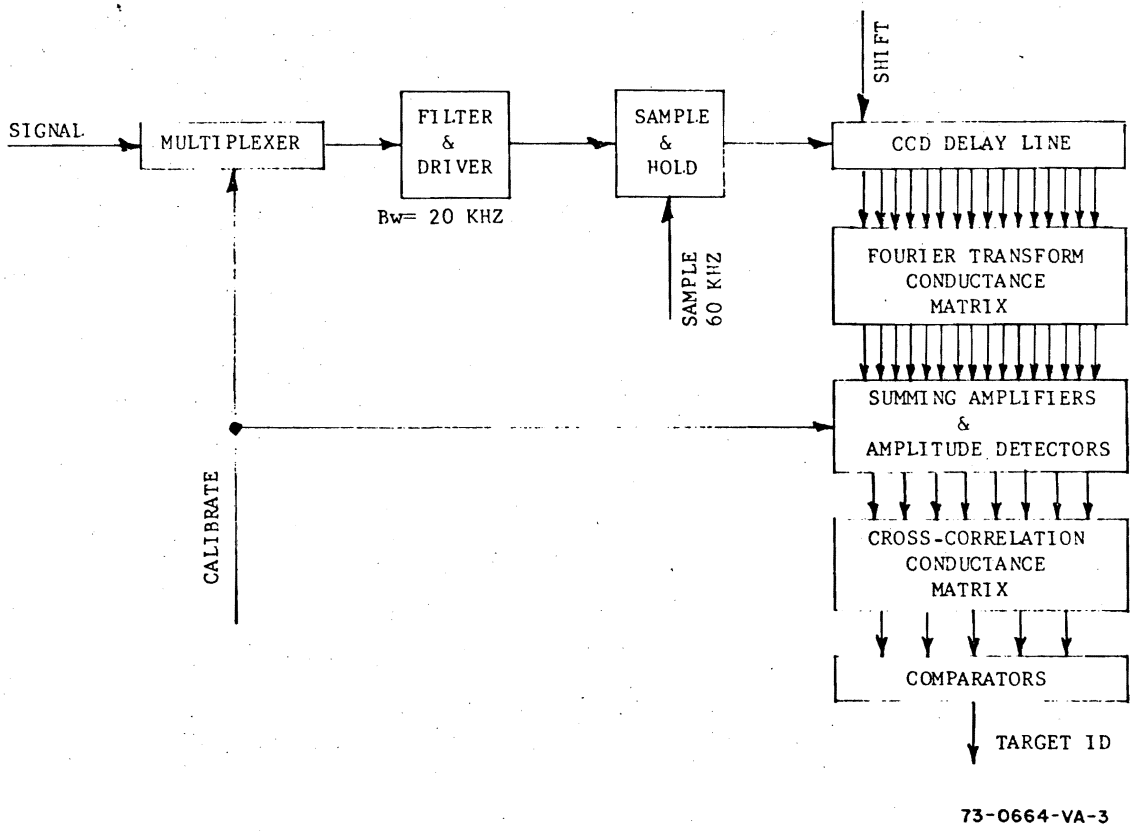

Figure 3. Transversal Filter (DASP)

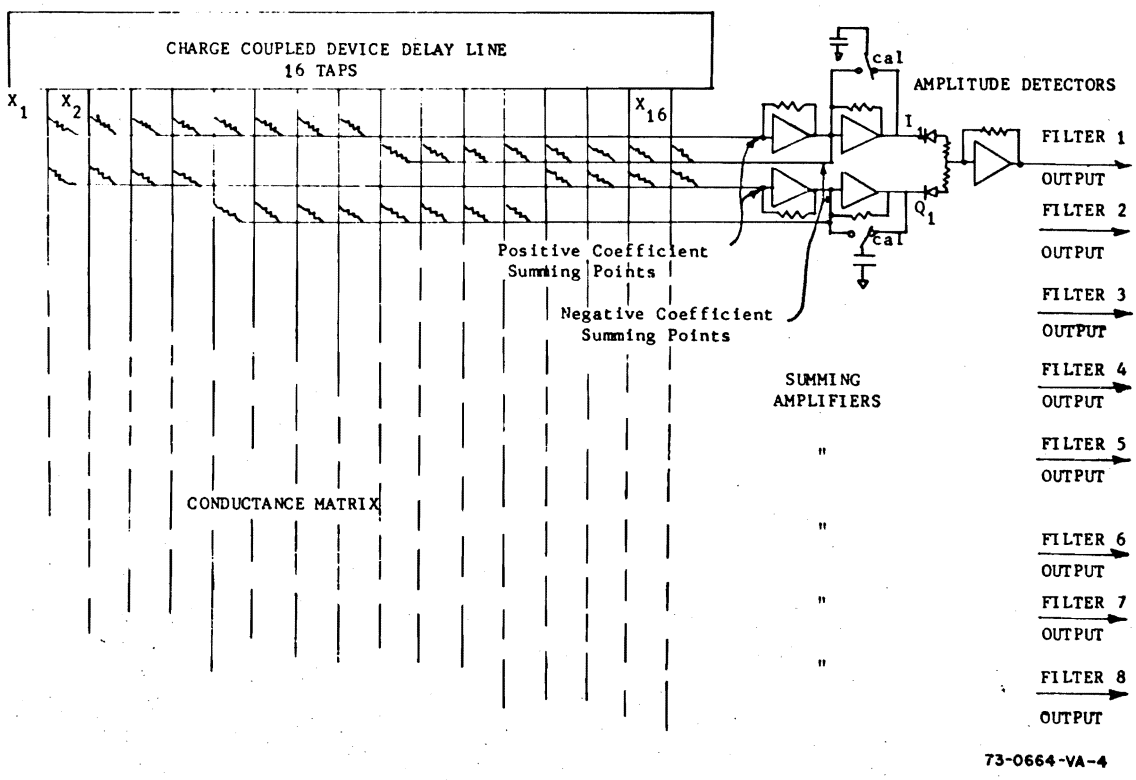

Figure 4. Conductance Matrix and Associated Circuitry

$$I_1 = \sum_{n=1}^{16} A1_n X_n = \sum_{\substack{\text{pos.} \\ \text{coeff.}}} |A_{1n}| X_n - \sum_{\substack{\text{neg.} \\ \text{coeff.}}} |A_{1n}| X_n \qquad (3)$$

The coefficients are the conductance values. There are 16 conductance elements for each I or Q and 32 for each filter. Separate sums are formed for the terms with positive coefficients and the terms with negative coefficients. These sums are then subtracted as indicated in equation (3). During the calibration procedure, the I and Q outputs are produced by the offsets of the CCD register. These values are stored on capacitors connected to the outputs of the summing amplifiers. The capacitors are then switched to the inputs, so that the offset components of the I's and Q's are subtracted out. This calibration procedure will be performed periodically.

IV. A LSI BUILDING BLOCK

The next step is to mechanize a row of MNOS conductance elements, each with two address switches (one for positive and one for negative coefficients) on the same chip as the CCD register.

These conductances will be individually programmable by means of external signals. This device gives two outputs (one for each output switch row bus), which are externally subtracted to give either I_1 or Q_1 component of a single filter [e.g., filter 1]. This is sufficient to determine the effect of the MNOS devices on the response and dynamic range of the filter bank. Some

areas of concern are the stability of the conductance values over time and temperature and the non-linearities in voltage-current transfer characteristic (conductance change with voltage). These problems will be discussed in a later section.

The basic concept involves the use of the programmable threshold voltage of an MNOS FET in conjunction with the non-destructive sensing of the CCD signal via a surface-potential sensing diffusion[3] applied to the gate of a FET. The output needs to be directly proportional to the product of the CCD signal and a parameter set by the MNOS threshold voltage, and must be capable of being summed with many other similar outputs. This last requirement means that the outputs should come from current sources and should be summed in an operational amplifier. Typically, FET's operating in their pentode regions behave like current sources but have a drain current proportional to the square of the gate-to-source voltage decreased by the effective threshold voltage. In one scheme, this squaring characteristic is used to obtain the desired product directly by incorporating the MNOS programmable memory cell within the CCD nondestructive sensing FET. Although the simplicity of the scheme was quite attractive, the desired output current was small compared to a large uncontrollable dc component that also adds into the summing point. Non-linearity was another problem inherent in the simple scheme using FET pentode squaring.

The selected approach is shown schematically in figure 5. The proposed

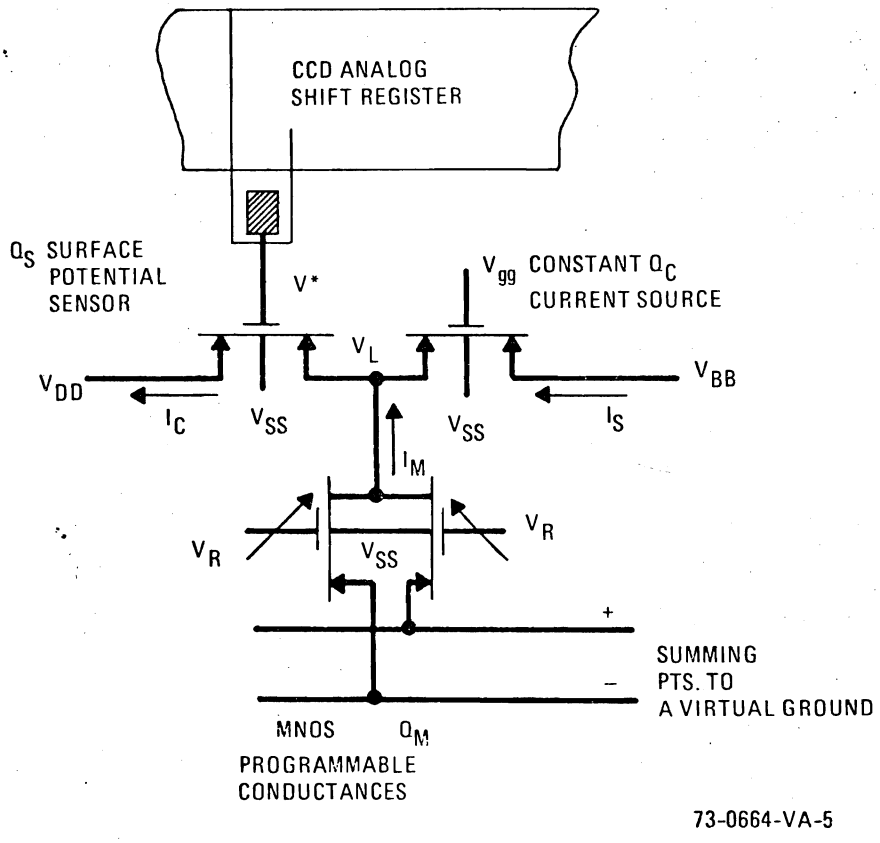

Figure 5. The Non-Destructive Sensing and Programmable Weighting Cell

cell uses a conventional MOS FET source-follower, Q_s, biased by a constant-current generator, Q_c, (another FET) to transform the high impedance associated with the CCD surface potential sensing diffusion into a low impedance voltage node, V_L. A small programmable conductance, the MNOS FET, Q_M (operating in the linear triode region), connects the voltage node, V_L, to the summing point thereby providing essentially a signal current source

$$I_M = -g_{ds_m} \cdot V_L \text{ where } g_{ds_m} = \mu C_M \left(\frac{W}{L}\right)_{Q_M} \cdot (V_R - V'_{TM}) \quad (4)$$

This is directly proportional to the product of the MNOS programmable weight and V_L, the CCD surface potential as transformed by a "unity gain" source-follower. We now show the desired results in somewhate greater detail. For Q_c operating in the pentode region:

$$I_S + I_M = I_C = \mu \frac{C}{2} \left(\frac{W}{L}\right)_{Q_C} \cdot (V_L - V^* - V'_{T_C})^2 \quad (5)$$

$$\text{where } V'_{T_C} = V_{T_C} + V_B \left(\sqrt{\frac{1 + (V_L - V_{SS})}{2\phi_F}} - 1 \right) \quad (6)$$

with V_{T_C} = zero source/substrate bias threshold 2v.
V_B = effective "bulk" potential 0.6v.
ϕF = Fermi potential ≈ 0.3v.
μC_O = 7×10^{-6} mhos/volt for a 2 KA oxide

Combining the two preceeding equations yields:

$$I_S - g_{ds_m} \cdot V_L = \frac{\mu Co}{2} \left(\frac{W}{L}\right)_{Q_C} \cdot \left[V_L^2 - 2V_L \cdot (V^* + V'_{T_C}) + (V^* + V'_{T_C})^2 \right] \quad (7)$$

Letting $\alpha_c = \frac{\mu Co}{2} \cdot \left(\frac{W}{L}\right)_{Q_C}$ we then find:

$$I_S - g_{ds_m} \cdot V_L = \alpha_c \cdot \left[V_L^2 - 2V_L \cdot (V^* + V'_{T_C}) + (V^* + V'_{T_C})^2 \right] \quad (8)$$

Taking the total derivative of this equation gives the tangential gain, G:

$$G = \frac{dV_L}{dV^*} = 2\alpha_c \cdot \frac{(V_L - V^* - V'_{T_C})}{g_{ds_m} + 2\alpha_c \cdot (V_L - V^* - V_{T_C})} \quad (9)$$

Although this is an exact expression for any input CCD surface potential, V*, it is necessary to eliminate the explicit dependence of G on V_L. Hence we find the solution:

$$V_L = V^* + V'_{T_C} - \frac{g_{ds_m}}{2\alpha_c} + \sqrt{\frac{I_S}{\alpha_c} - \frac{g_{ds_m}}{\alpha_c} \cdot (V^* + V'_{T_C}) + \left[\frac{g_{ds_m}}{2\alpha_c}\right]^2} \quad (10)$$

Substituting this exact solution for V_L back into G yields

$$G=1-\left[\frac{1+4\alpha_c}{g_{ds_m}}\cdot\left(\frac{I_S}{g_{ds_m}}-V^*-V'_{T_C}\right)\right]^{-1/2} \quad (11)$$

Typical values are the following:

$I_S = 0.25$ ma $\qquad g_{ds_m} = 40\,\mu$mhos

$\alpha_c = 10^{-5}$ mhos/volts

$V^* = V^*_O = dV^*$ with $V^*_O = -10$ volts.

$G = 1-[1+(60+10-5)]^{-1/2} = 0.88$ (static exact)

Substitution of $I_S = \alpha_s(V_{BB}-V_{gg}-V_{T_S})^2$ and addition of all the currents to the summing point, while ignoring smaller, higher-order terms:

$$I_{\substack{sum.\\pt.}} = \sum_{K=1}^{N} I_{M_K} = I_o + dI \text{ where} \quad (12)$$

$$dI = \sum_{K=1}^{N} W_K \cdot dV^*_K \text{ with } W_K = \alpha M_K \cdot \quad (13)$$

$$(V_R - V'_{TM_K}) \text{ and}$$

$$I_o = \sum_{K=1}^{N} W_K \cdot \left[V^*_{OK} + V'_{T_{C_K}} + \left(\frac{\alpha_s}{\alpha_c}\right)_K^{1/2} \cdot (V_{BB} - V_{gg} - V_{T_{S_K}})\right] \text{ and} \quad (14)$$

K indexes the discrete analog cells along the CCD analog delay line. To obtain the maximum range of weightings, V_R is selected slightly larger than the maximum MNOS threshold in the line. V_{gg} is adjusted to minimize the constant current to the summing point. The positive and negative weighting coefficients are obtained by a selection of the appropriate MNOS conductance in figure 5. In a final LSI chip design, the selection of the desired MNOS conductance sign and position along the CCD shift-register will be accomplished with an address/decode circuit; however, in the initial LSI chip the selection is manual, to simplify the fabrication and evaluation. Figure 6 illustrates a cal-comp plot of the analog weighted tap cell for the programmable LSI transversal filter. The block diagram of the LSI block is shown in figure 7. The input circuit is a stabilized injection circuit to insure uniform charge injection in the surface channel CCD. The output circuit is a gated charge integrator with a correlated double sampling readout technique. The CCD shift-register is a "sealed" surface channel structure composed of a dual nitride/oxide dielectric to provide stability and long endurance under high electric field strengths. The electrodes are formed with aluminum and polycrystalline silicon deposits, and the CCD register operates in a "quasi" 2ϕ, push-clock mode. The entire fabrication sequence consists of 7 photographic mask operations. The MNOS memory conductances have been fabricated with a technology[4] which has been developed for MNOS non-volatile BORAM, CCD non-volatile BORAM, and an electrically programmed meter system.[5]

IV. ADDITIONAL TECHNICAL CONSIDERATIONS

COMPLEX SIGNAL PROCESSING

The conductance matrix is inherently capable of performing complex operations on

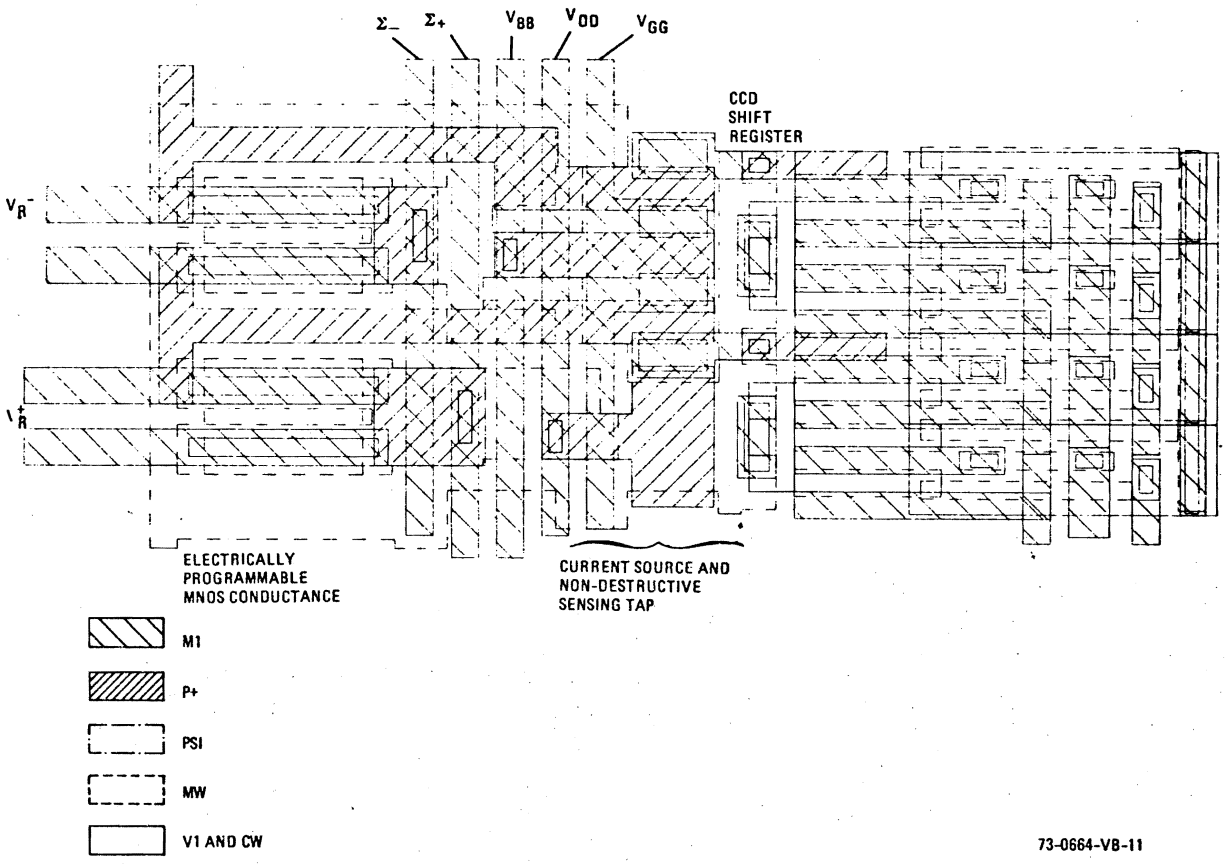

Figure 6. CalComp Plot to Illustrate Composite of 7 Photographic Mask Operations for Programmable Analog Weighted Tap

complex signals. It is only necessary to make the appropriate real and imaginary assignments to the CCD taps and the conductance matrix such as shown in figure 8. In this case the matrix outputs are valid only when the real and imaginary data samples along the SR coincide with the correspondingly defined tap position, i.e., every other clock period.

VOLTAGE DRIFT AND BIAS ERRORS

Figure 9 illustrates a method to compensate for voltage drift and biases in a complex filter, where only every other CCD register cell is tapped, and a 4-to-1 input signal multiplexer sequentially selects the zero reference level for the quadrature (imaginary) channel, followed by the corresponding signal level and then repeating for the inphase (real) channel. Any output in either the inphase or the quadrature channel is an error when the zero reference signals coincide with the CCD register taps. A simple compensation method can be incorporated into the output interface circuitry, as shown by the detail. The switch is placed in the C_o position when the zero

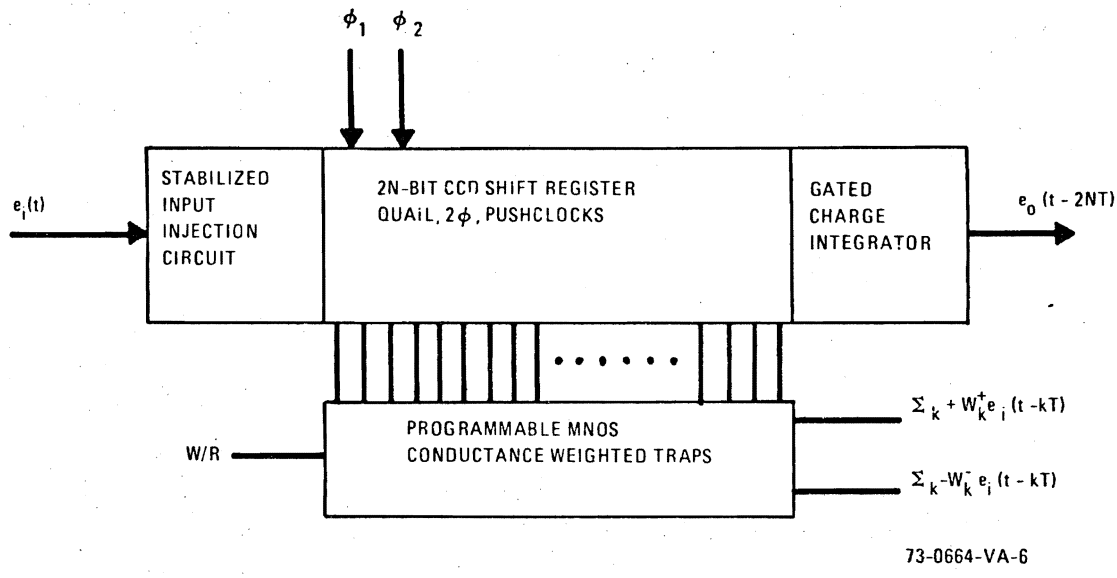

Figure 7. Block Diagram of LSI Programmable Transversal Filter

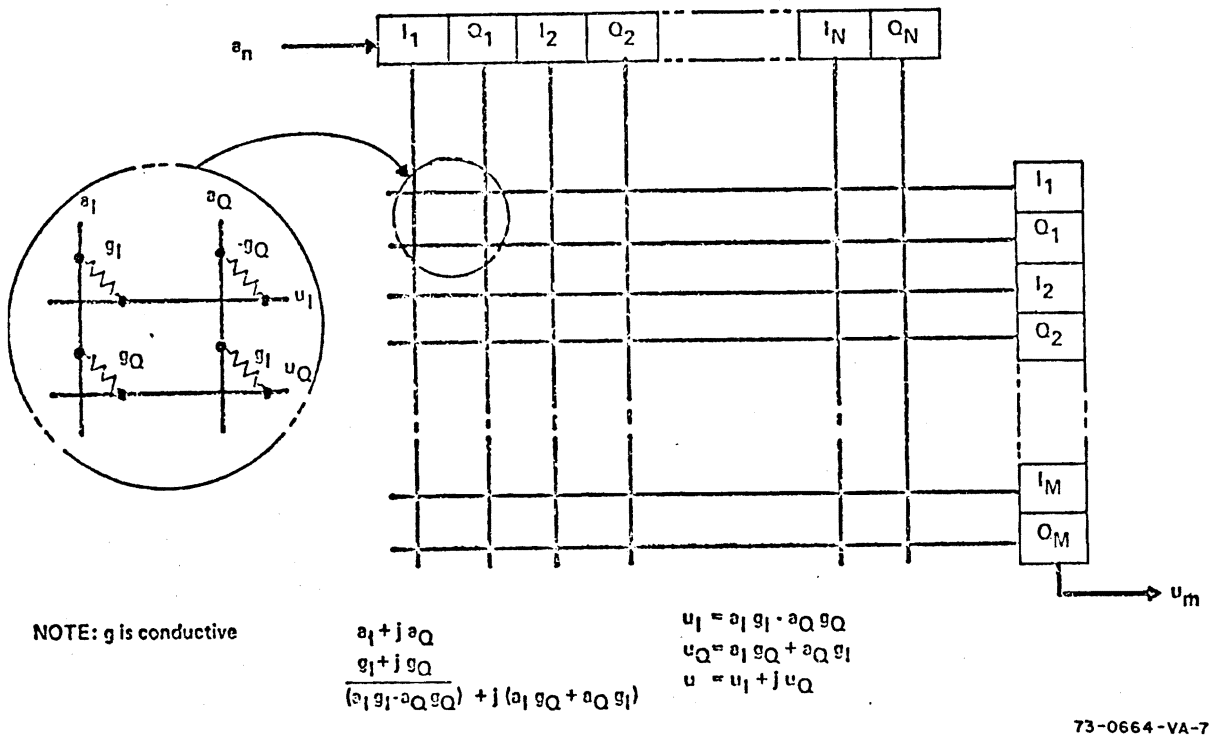

Figure 8. Complex Processing

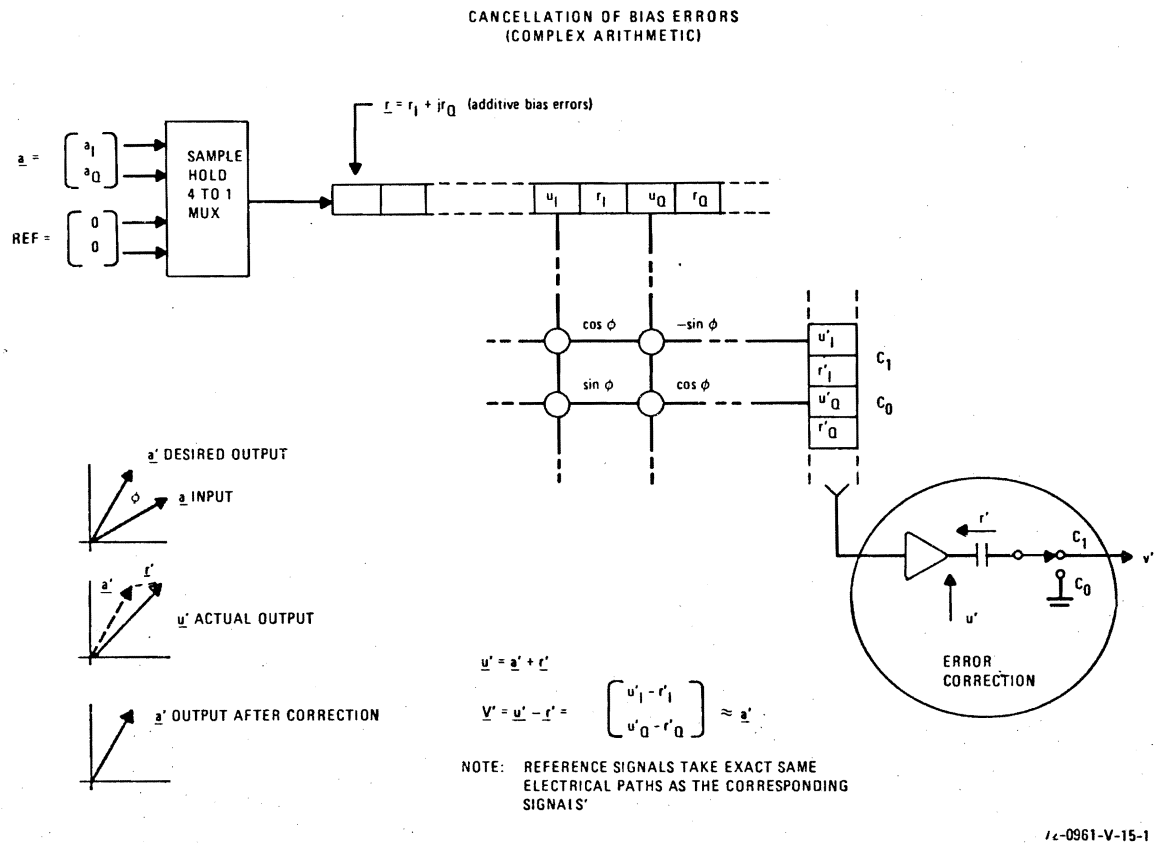

Figure 9. Cancellation of Bias Errors

reference signals coincide with the CCD SR taps, which charges the capacitor with any residual bias errors. The error component is removed from the output signal with the output switch in position C_1 during the clock periods, when the input signal is aligned with the taps as illustrated. This connection is applied sequentially to the inphase and quadrature channels. Thus, to the greatest degree possible, all signals pass through the same elements and the corresponding signal and ground reference levels pass through identical on chip paths. It is likely that the dc bias errors will be slowly varying, such that the zero signal reference need not be interlaced between alternate signal samples but may be injected only occasionally.

MNOS CONDUCTANCE PROGRAMMABILITY AND STABILITY

Measurements, which illustrate the conductance drift immediately following a memory clear and program operation, are plotted in figure 10 over a time history of about 100,000 minutes. The bottom curve plots the source current for the first 20 minutes after programming. This curve approximates the expected linear current vs. logarithm of time characteristics. The deviation from the final value was reduced by a factor of about five when using a bipolar pulse train with a variable duty ratio. Also differential reprogramming (i.e., shifting the conductance by a small increment) using the bipolar method of lower voltage level,

CURVE NO. 4-3: I_M VS. TIME, MNOS IC NO. 1, DEVICE G1Y101
10 0.1 SEC CLEAR PULSES + 26.5V, FOLLOWED BY ONE 1.5 μSEC -26.5V "1" PROGRAMMING PULSE
V_{GS} = -8.188V
V_{DS} = -4.8V
V_{GS} & V_{DS} APPLIED CONTINUOUSLY FOR DURATION OF TEST

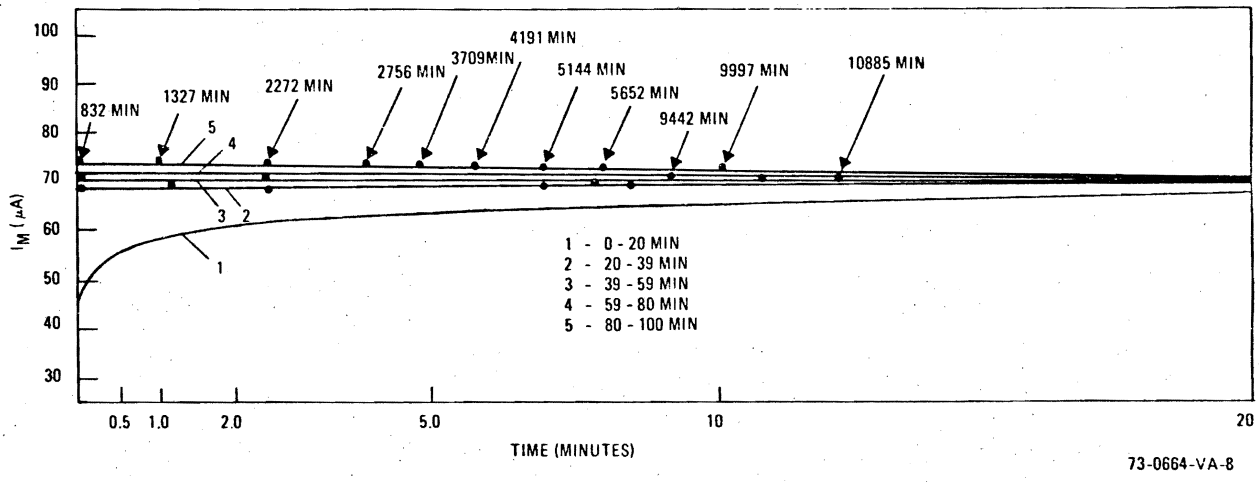

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Figure 10. Conductance Drift vs. Time after Programming

CURVE No 2-68A (DATA FROM RUN 2-68) MNOS IC NO. 2 DEVICES G1Y101, G2Y101, G3Y101, G4Y101
INVERTED CONNECTION - I_D VS TEMPERATURE
V_{DS} = -7.0V, V_{GS} = -11.0V

STEP 1: FULL CLEAR: 20 0.1 μ SEC, +26.5V PULSES AT 2 Hz
STEP 2: PROGRAMMED "1": One 5 MSEC, -26.5V PULSE
STEP 3: APPROXIMATELY THREE (3) HOURS FROM PROGRAMMING, MEASURED I_M AT EACH TEMPERATURE, STARTING AT -20°C.. STABILIZATION TIME AT EACH TEMPERATURE APPROXIMATELY 5 MIN. SEPARATE TEMPERATURE RUN FOR EACH DEVICE.

NOTE: SLIGHT COMPENSATING EFFECT OF DEVICE V_T DRIFT TENDED TO STRAIGHTEN CURVES AT THE TWO HIGHEST TEMPERATURES, ESPECIALLY FOR DEVICE G1Y1D1. THIS MAY BE PARTLY DUE TO SHORTER DELAY BETWEEN PROGRAMMING AND MEASURING FOR THIS DEVICE (1.5 HOURS).

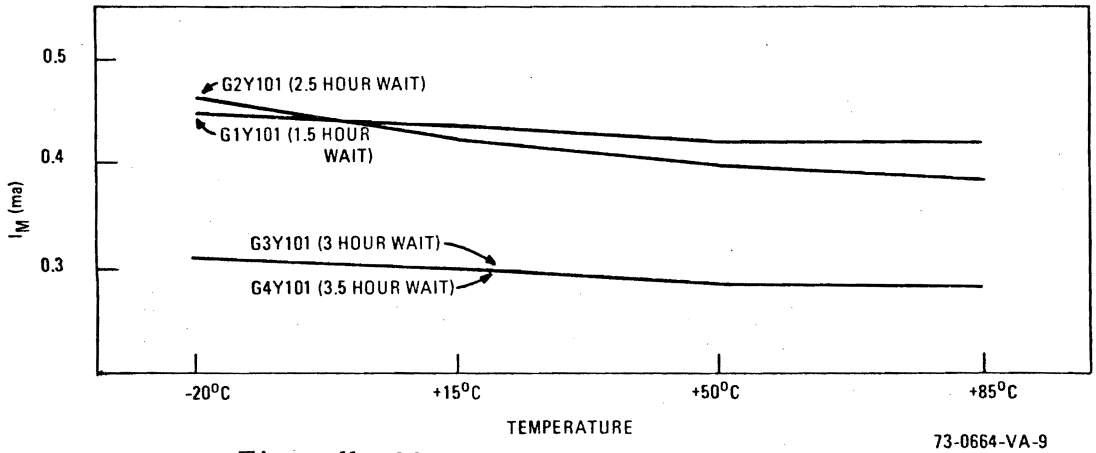

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Figure 11. Memory Current vs. Temperature

did not affect the long term drift rate. This result is particularly important for the final calibration of the matrix and for the use in adaptive processing systems. The effect of temperature for the first 3 hours or programming is shown in figure 11. The linearity of the MNOS device operating as a variable conductance device in the linear mode is plotted in figure 12. Note that operation into the third quadrant is feasible. It was determined that the varying displacements of the curves from the origin are caused by plotter instability. These MNOS devices were fabricated with a thin-oxide X_o = 25Å and were intended for high speed erase/write operation, not the DASP application; however, these devices illustrate the potential of the approach. The programmable weighted tap provides an additional advantage, in that the analog signal is separate from the clock pulses. The analog and digital signals are mixed in the electrode weighting technique.[6]

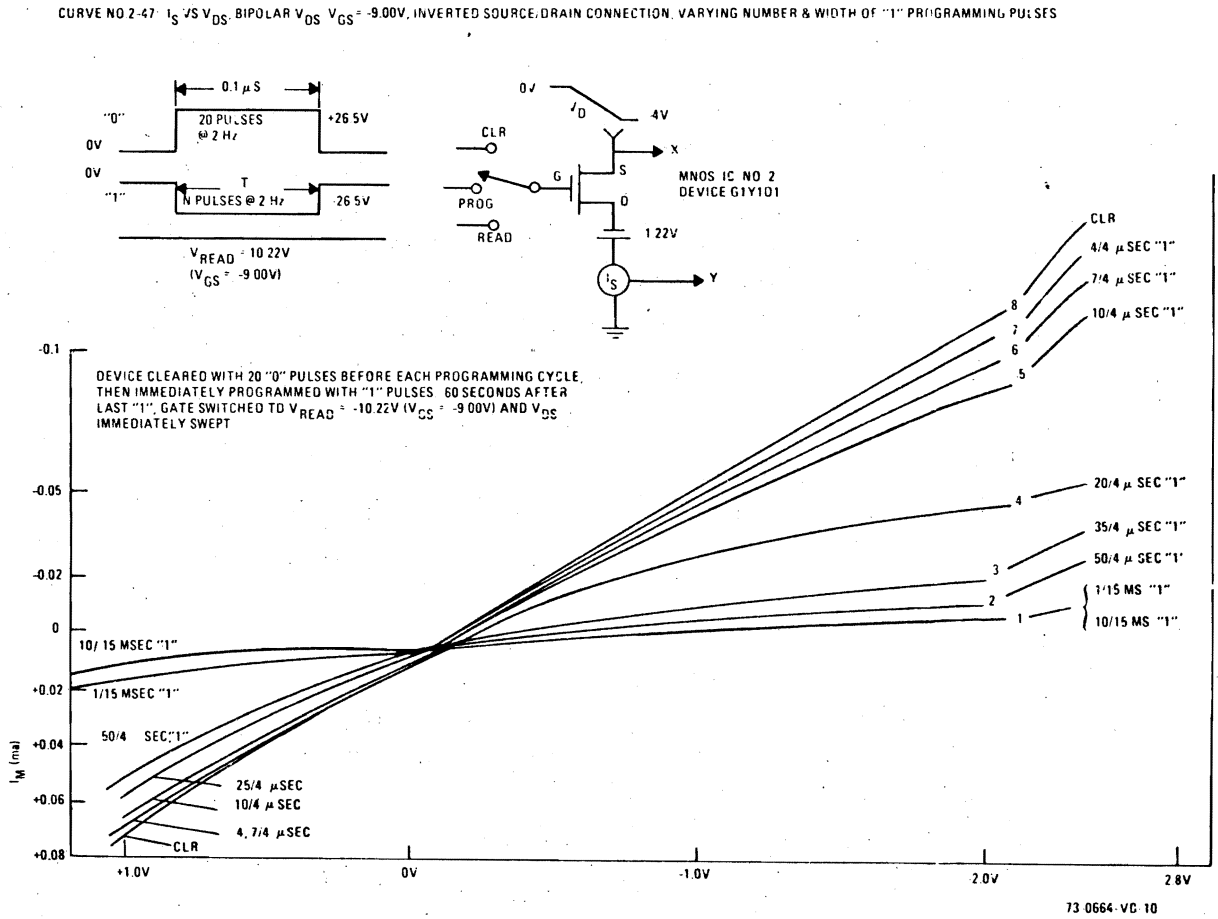

Figure 12. Memory Current vs. Drain to Source Voltage

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