Combining linear and SPAD-mode diode operation in-pixel for wide dynamic range CMOS optical sensing

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June 8, 2020

Oregon State University

Outline

- Motivation & Background
- In-Pixel Wide Dynamic Range Optical Sensor Array
- On-Chip High-Voltage and Low-Voltage Bias Generation

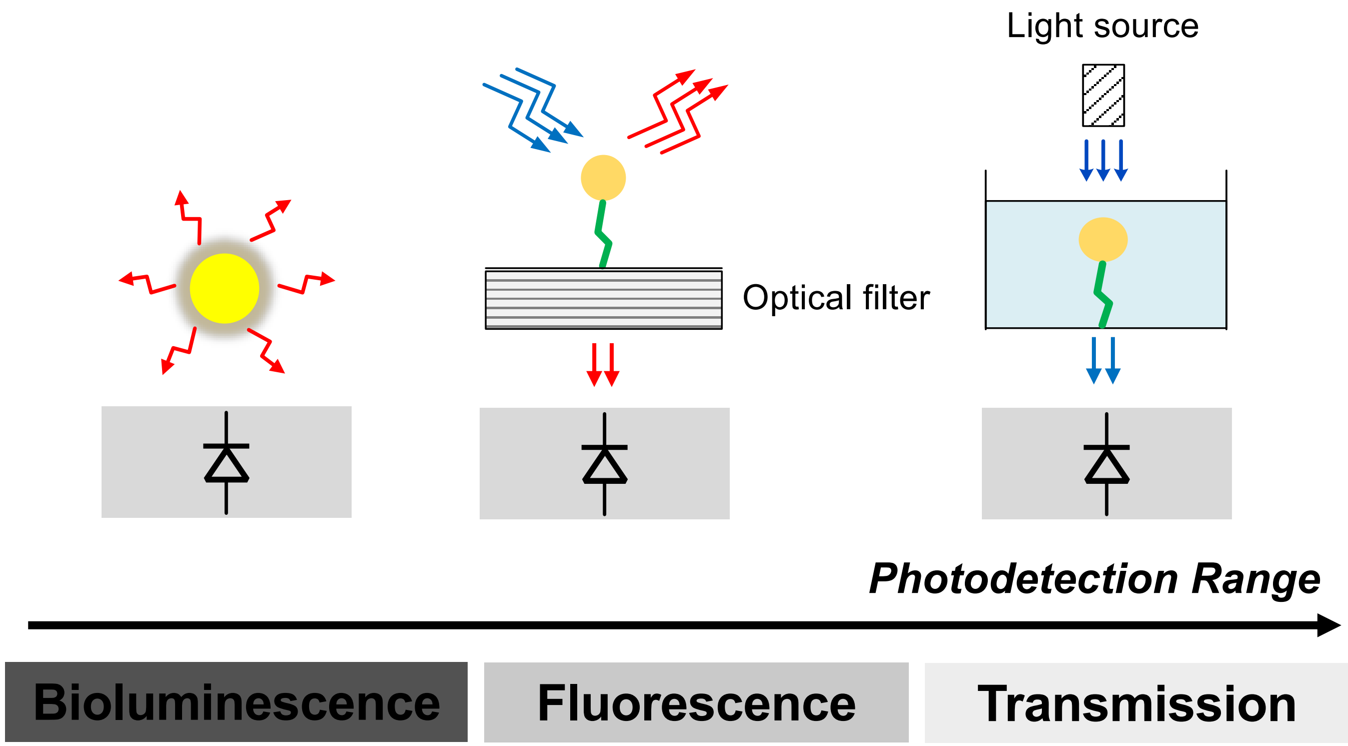
Wide-Dynamic-Range Imaging

HDR image

https://www.easyhdr.com/examples/

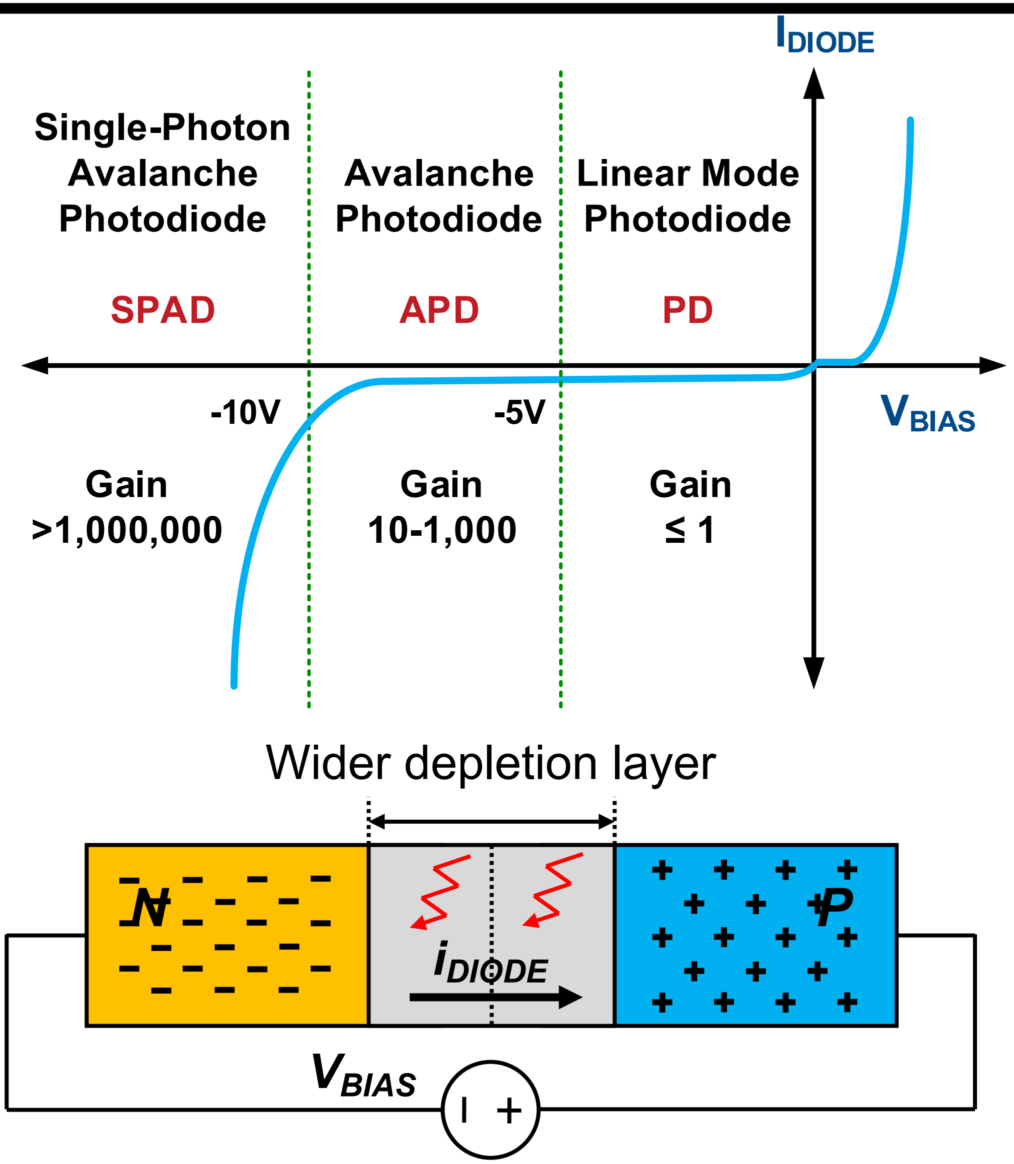
Natural scene: >100 dB
Commercial HDR image sensors: 120 – 150 dB

Biomedical Sensing



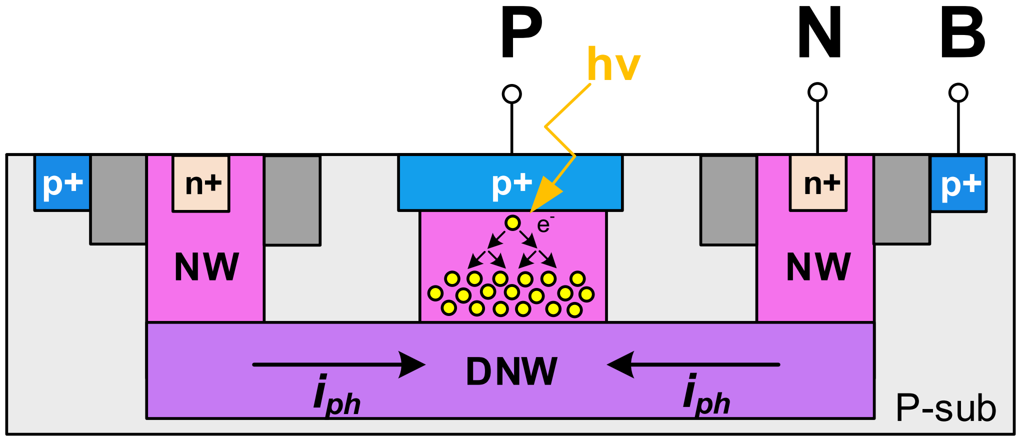
Bioluminescence	Fluorescence	Transmission
~10^5 photons/cm^2/sec	>10^{10} photons/cm^2/sec	>10^{20} photons/cm^2/sec

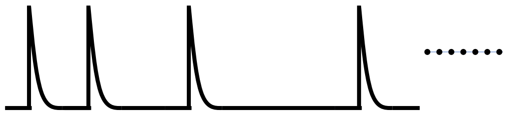
CMOS Photodiode Operational Modes



CMOS Photodiode Operational Modes

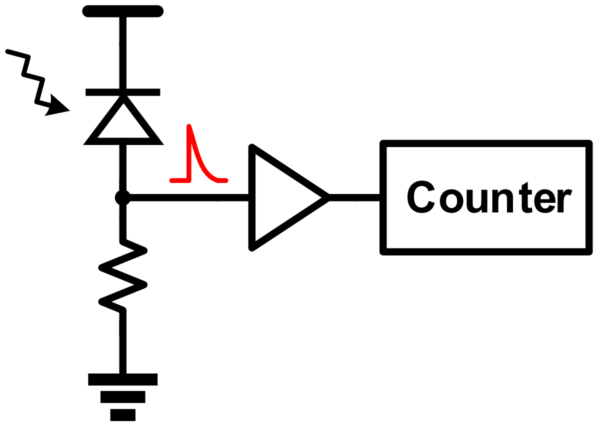
SPAD-mode photodetection



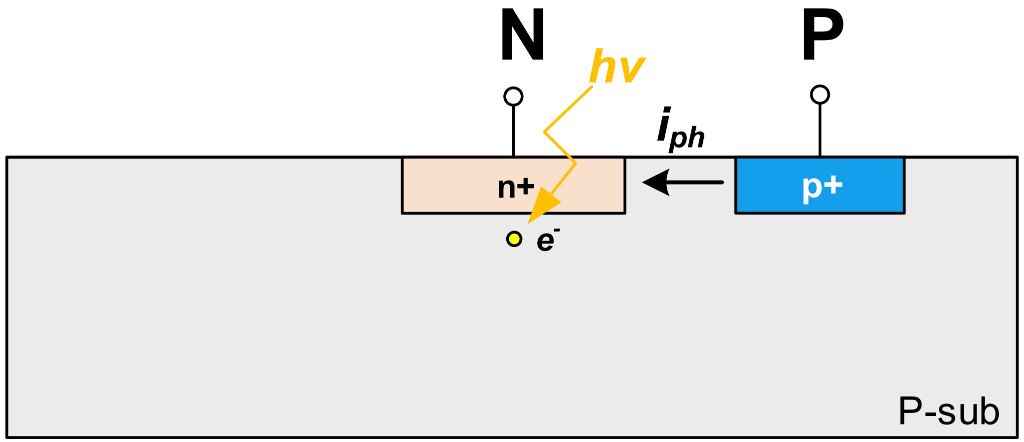


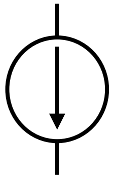
Pulse rate ∝ light

HV bias > V_{BV}



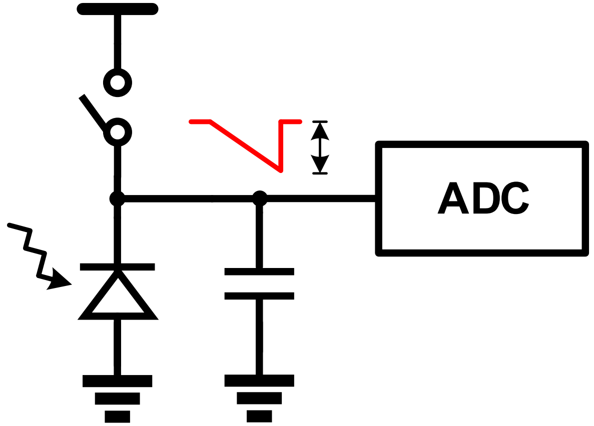
PD-mode photodetection



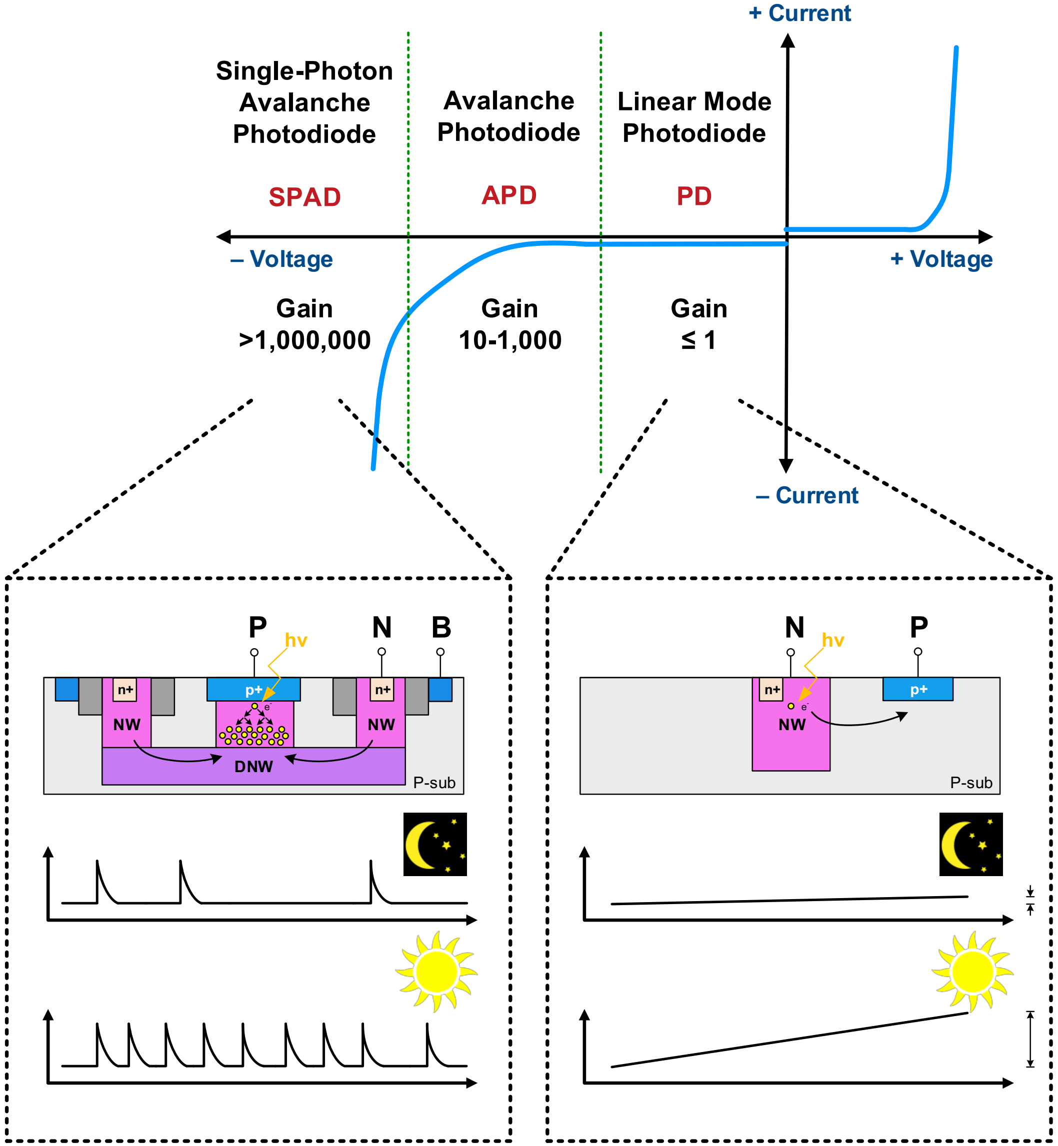


Photocurrent ∝ light

LV bias << V_{BV}



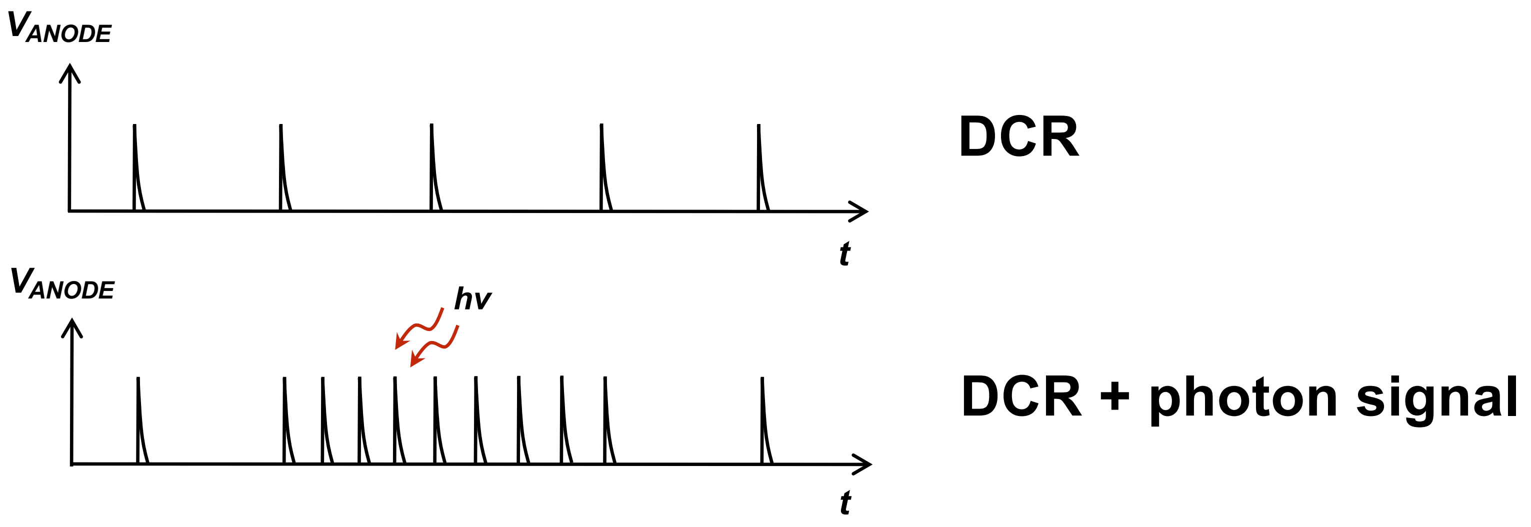
CMOS Photodiode Operational Modes



SPAD Readout Challenges (1)

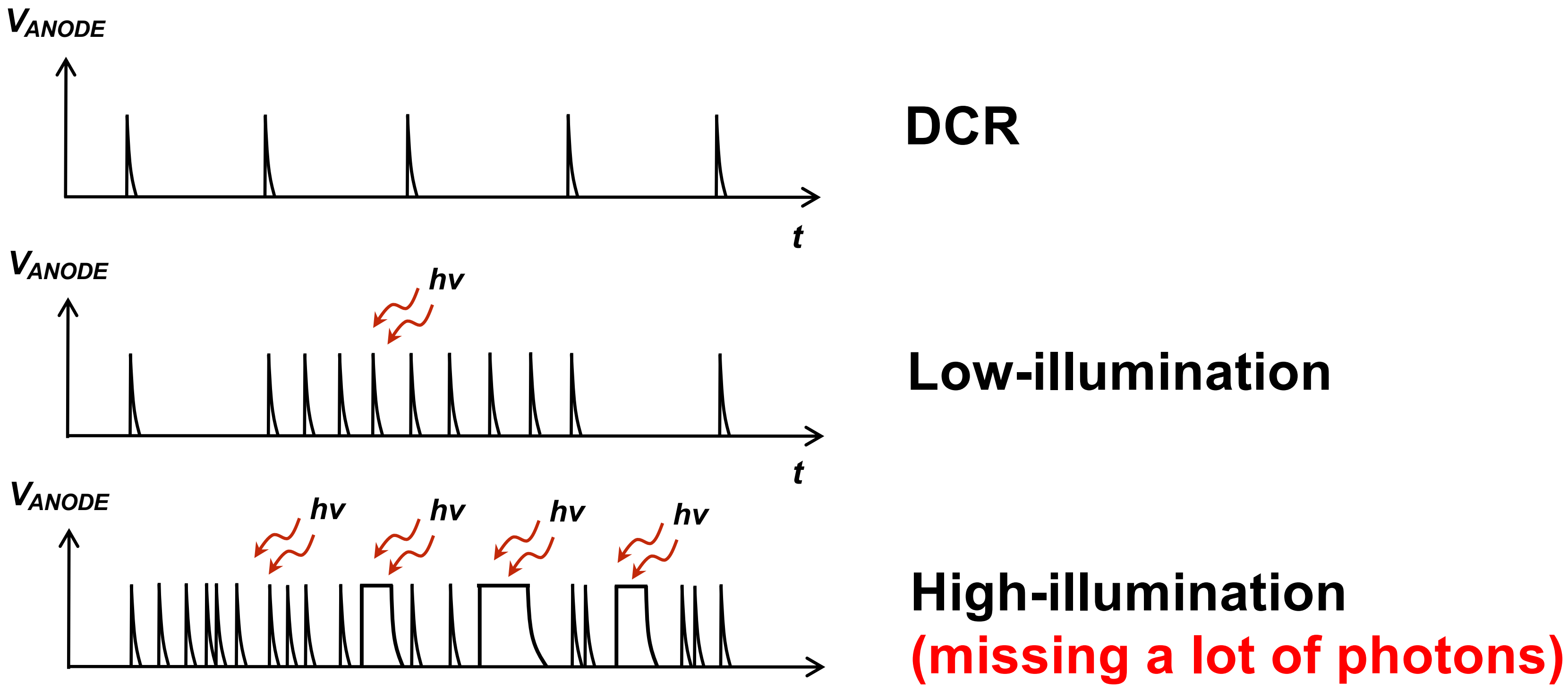
❑ Dark count rate (DCR)

- Thermally excited, trapped carriers and tunneling
- Increases power consumption and decreases sensitivity
- Structure and process dependent



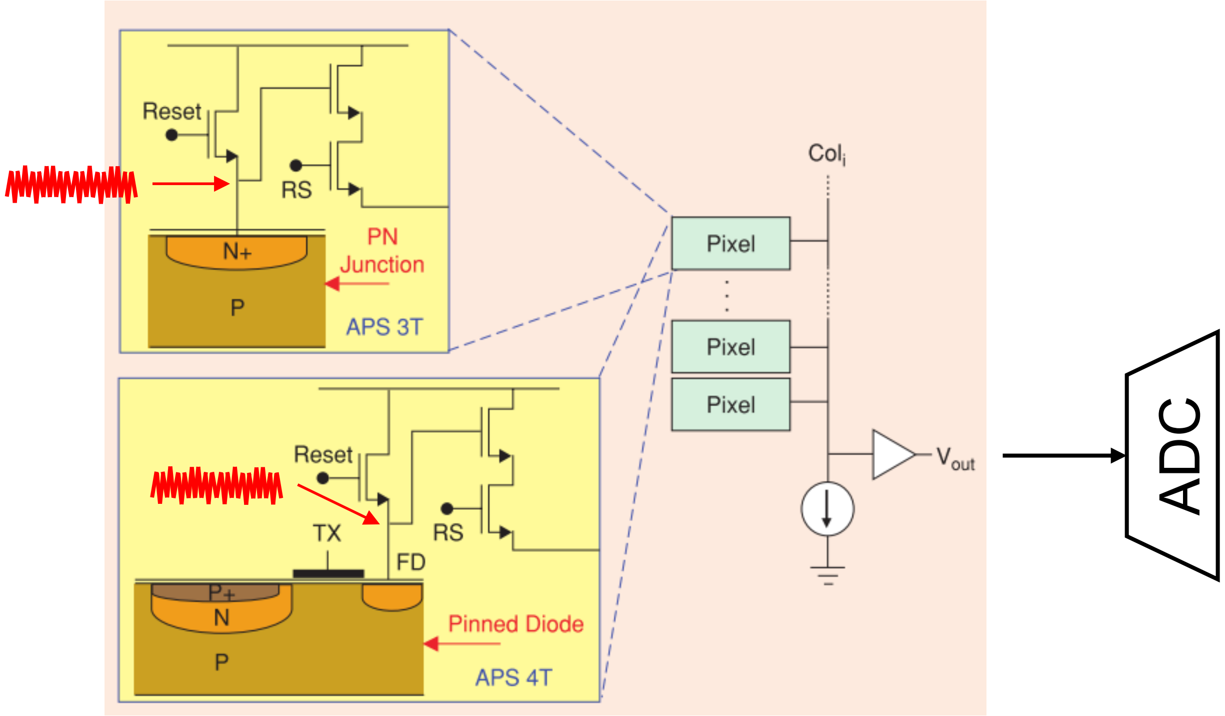
SPAD Readout Challenges (2)

- **Limited dynamic range**
  - Pulse rate is easily saturated at high-illumination
  - Time resolution needs to be significantly high → active circuits burning more power

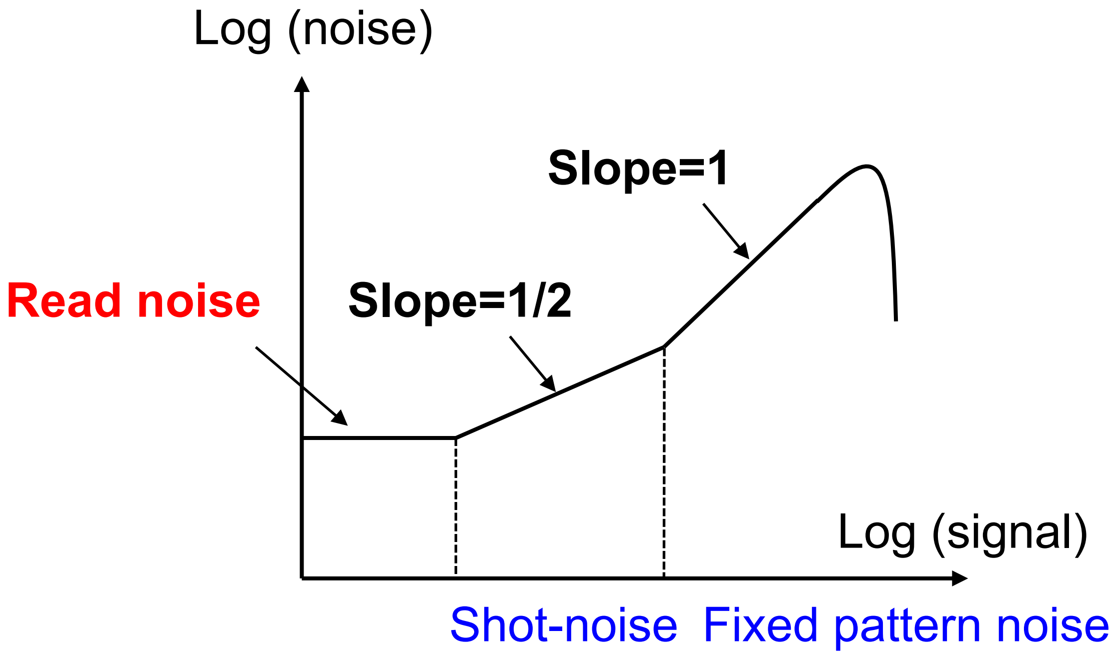


PD Readout Challenges

- **Limited sensitivity**
  - Limited quantum efficiency (no avalanche multiplication)
  - Read noise (circuit noise) limits lowest detectable signal
  - Long integration time

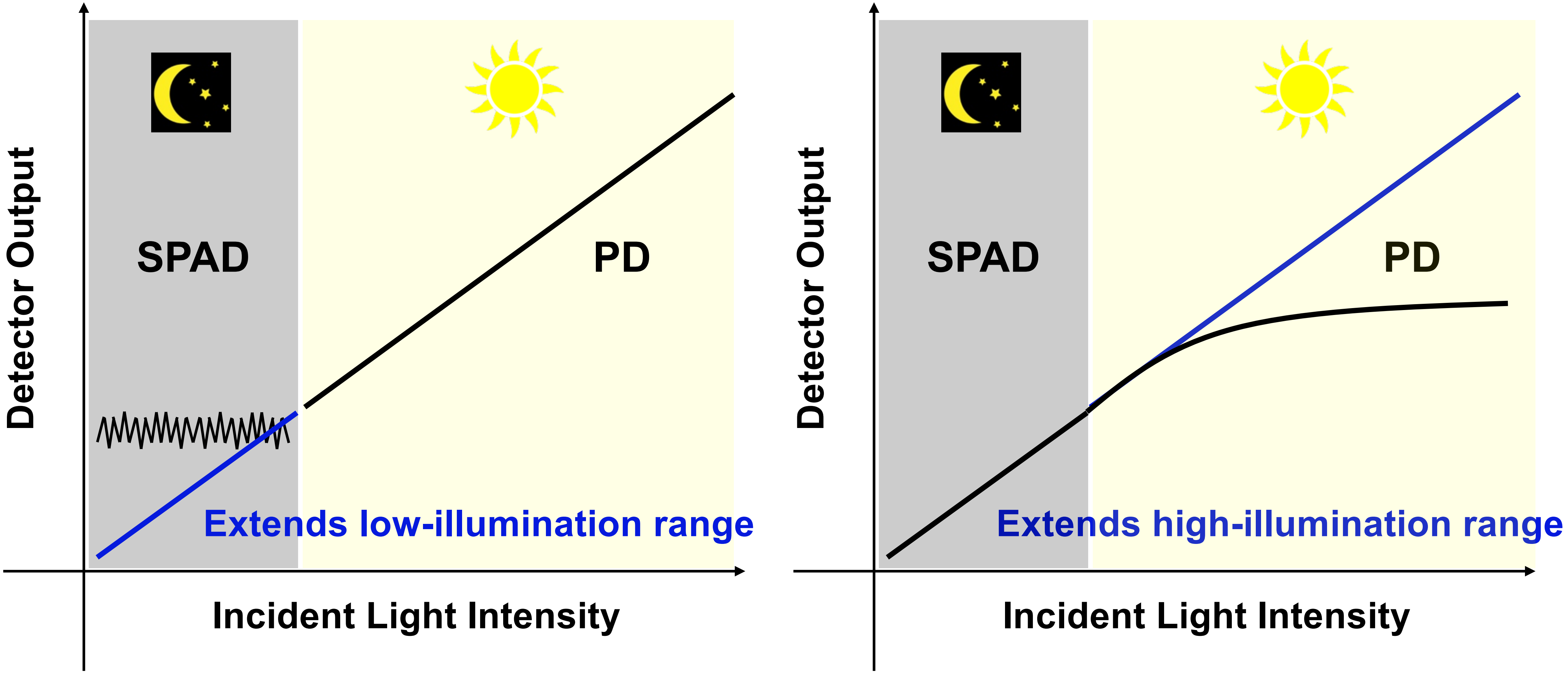


[Gamal et al, *IEEE Circuits and Devices Magazine* (2005)]



Photon transfer curve

Dual-Mode: Dynamic Range Extension

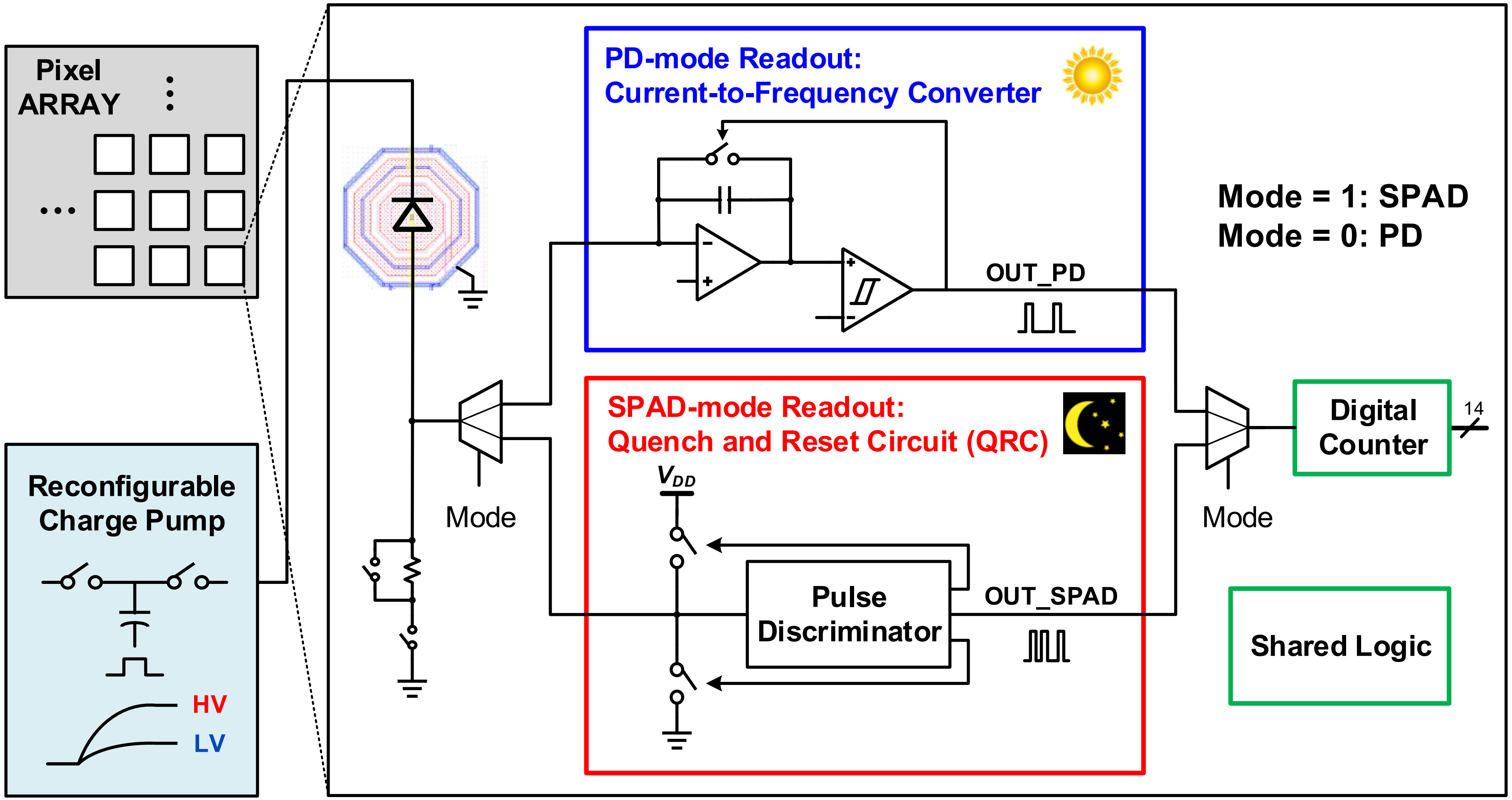


Outline

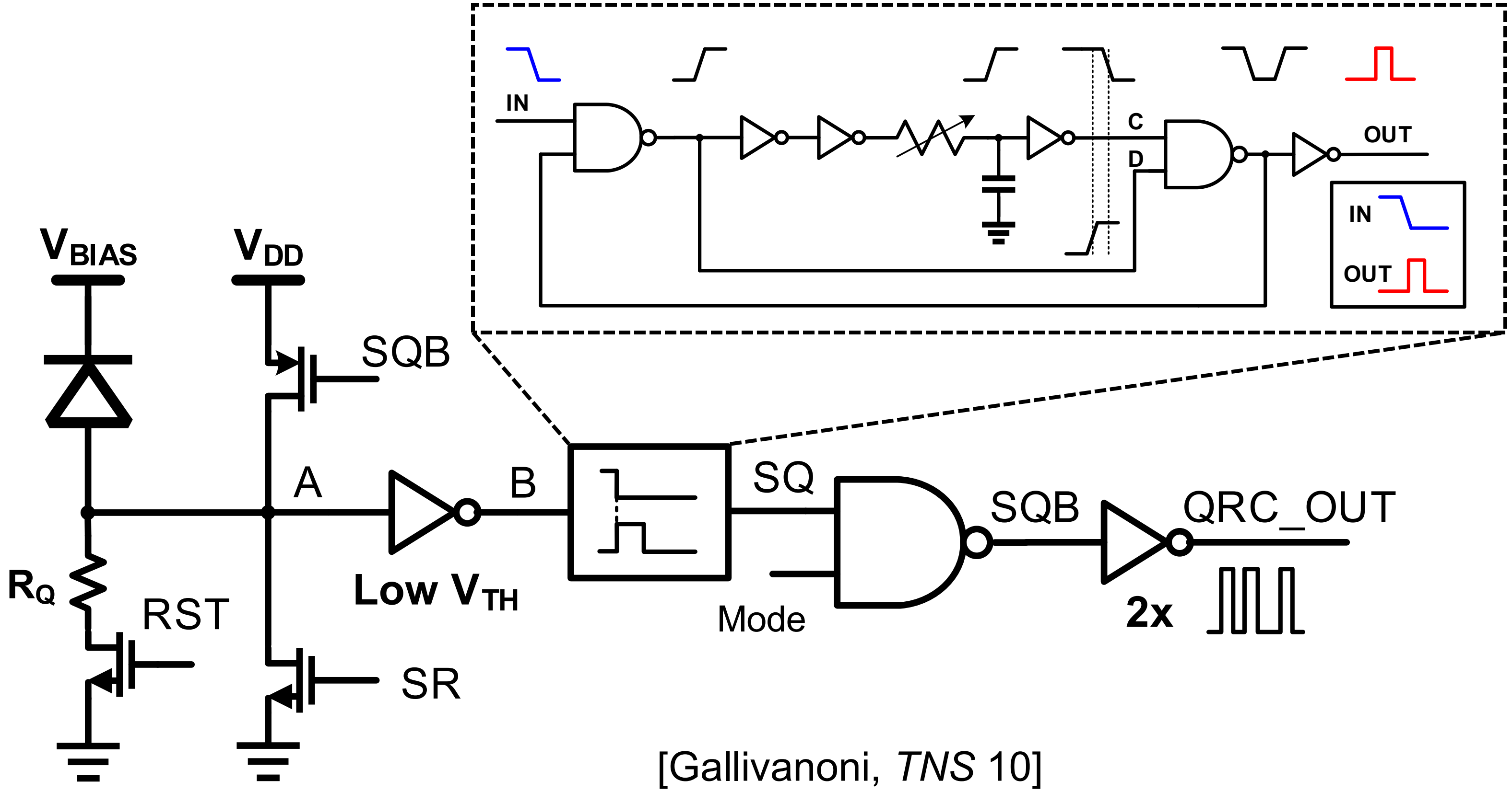
Hyunkyu Ouh
Ph.D. 2019
(Now at Apple)

- ❑ Motivation & Background
- ❑ **In-Pixel Wide Dynamic Range Optical Sensor Array**
- ❑ On-Chip High-Voltage and Low-Voltage Bias Generation

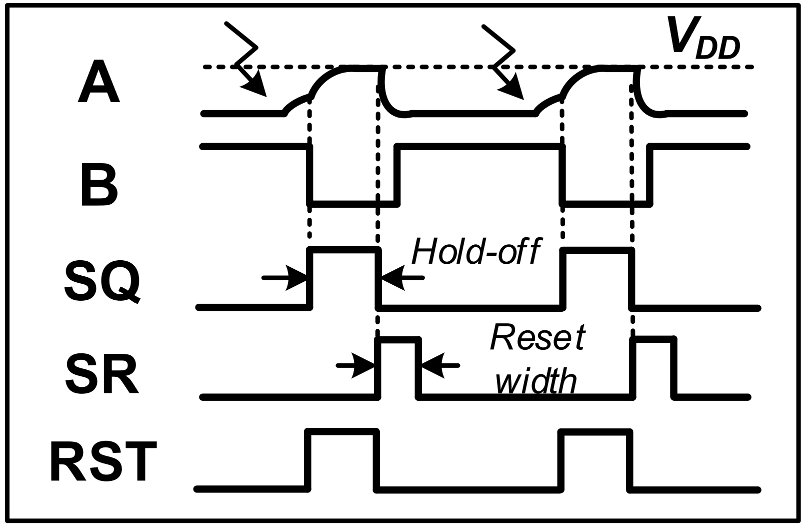
In-Pixel Readout Architecture



SPAD-mode: Mixed Quench-and-Reset Circuit

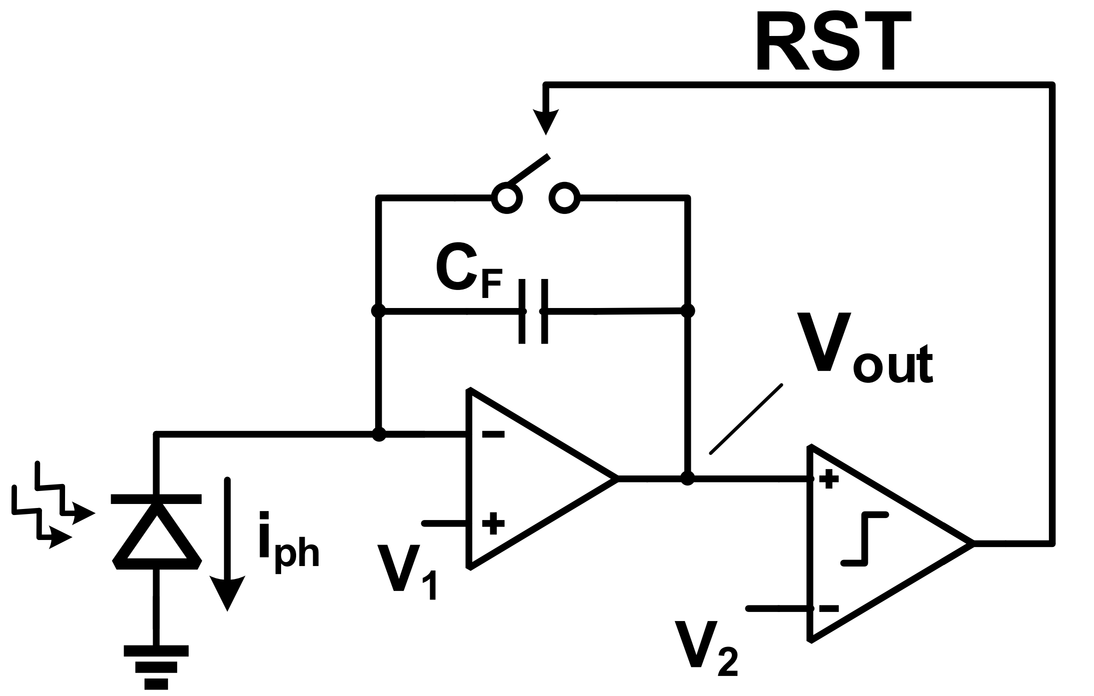


[Gallivanoni, *TNS* 10]

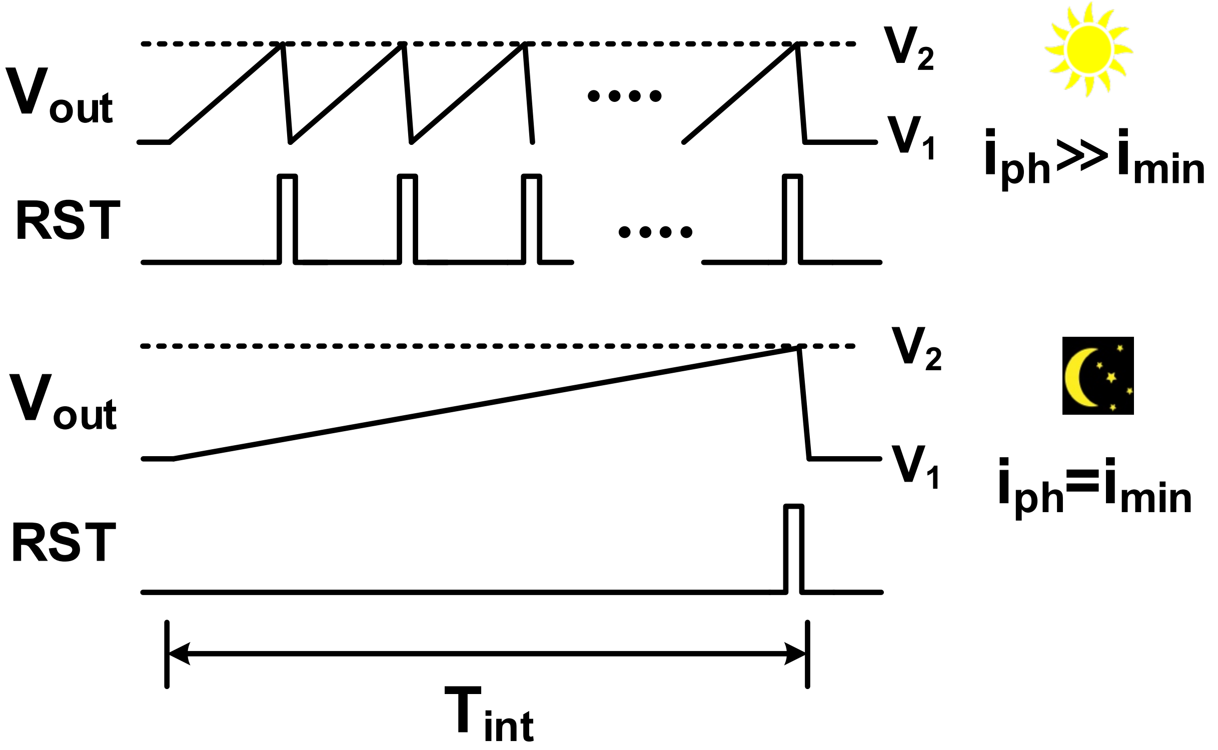


- Mixed quench and active reset; final output is a CMOS digital pulse train
- Hold-off time can be controlled for after-pulse reduction

PD-mode Readout: I-to-F Conversion

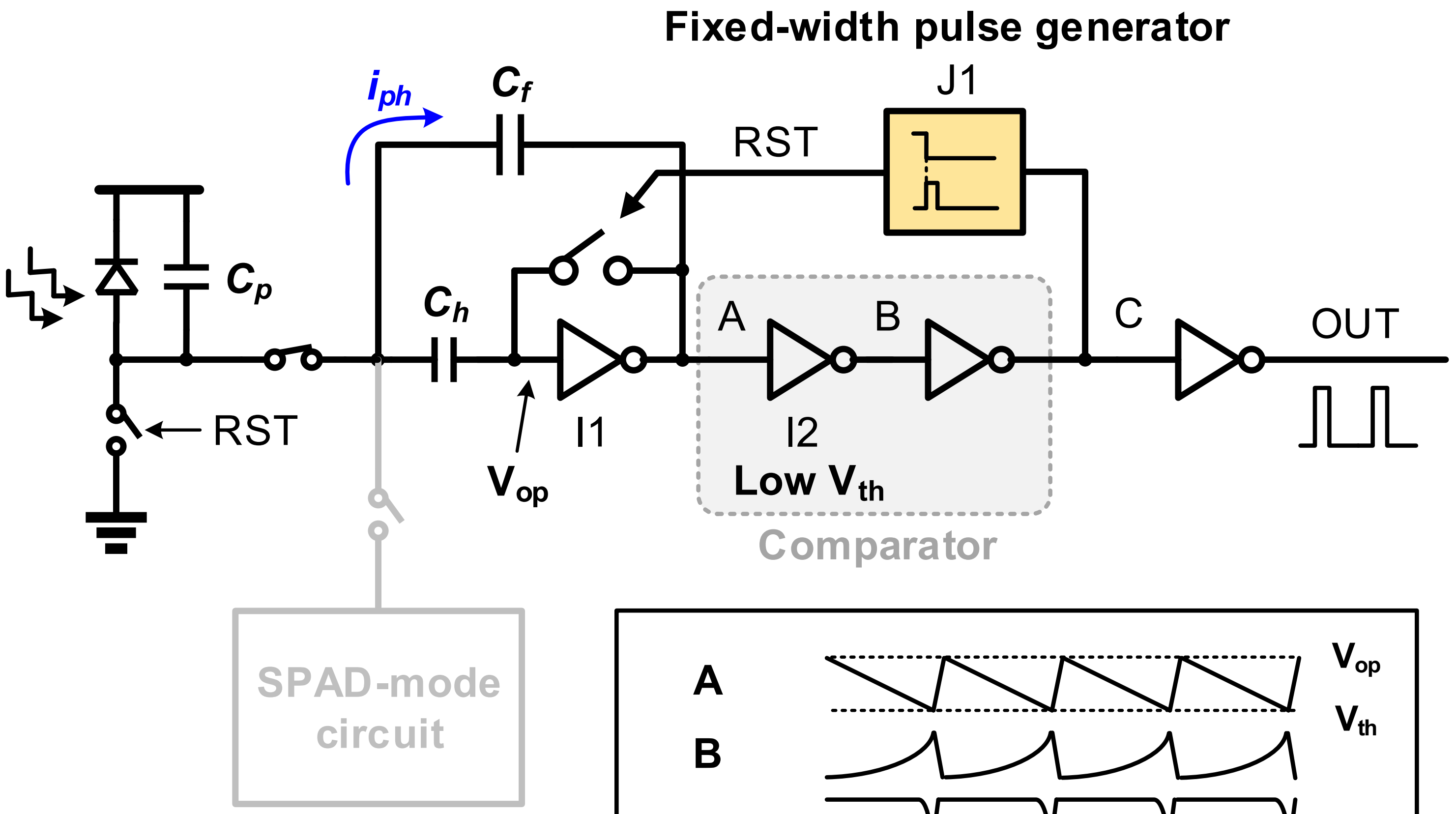


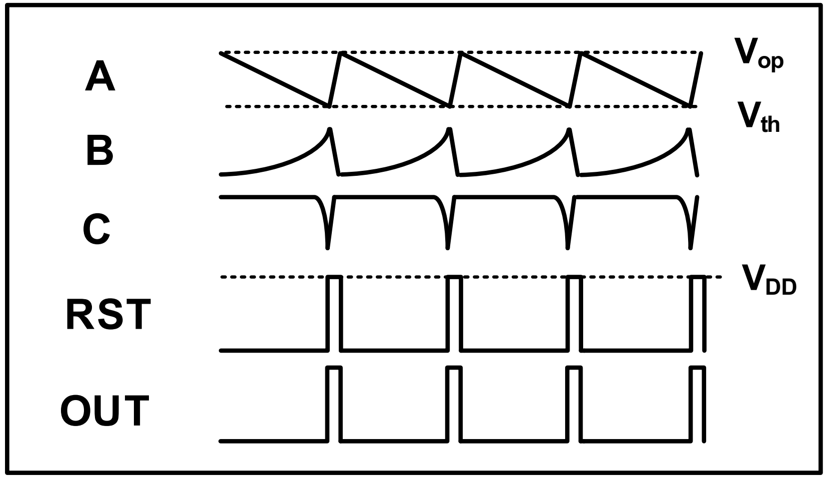
Current-to-Frequency Converter



$$\frac{N}{T_{INT}} = \frac{i_{ph}}{C_F(V_2 - V_1)}$$

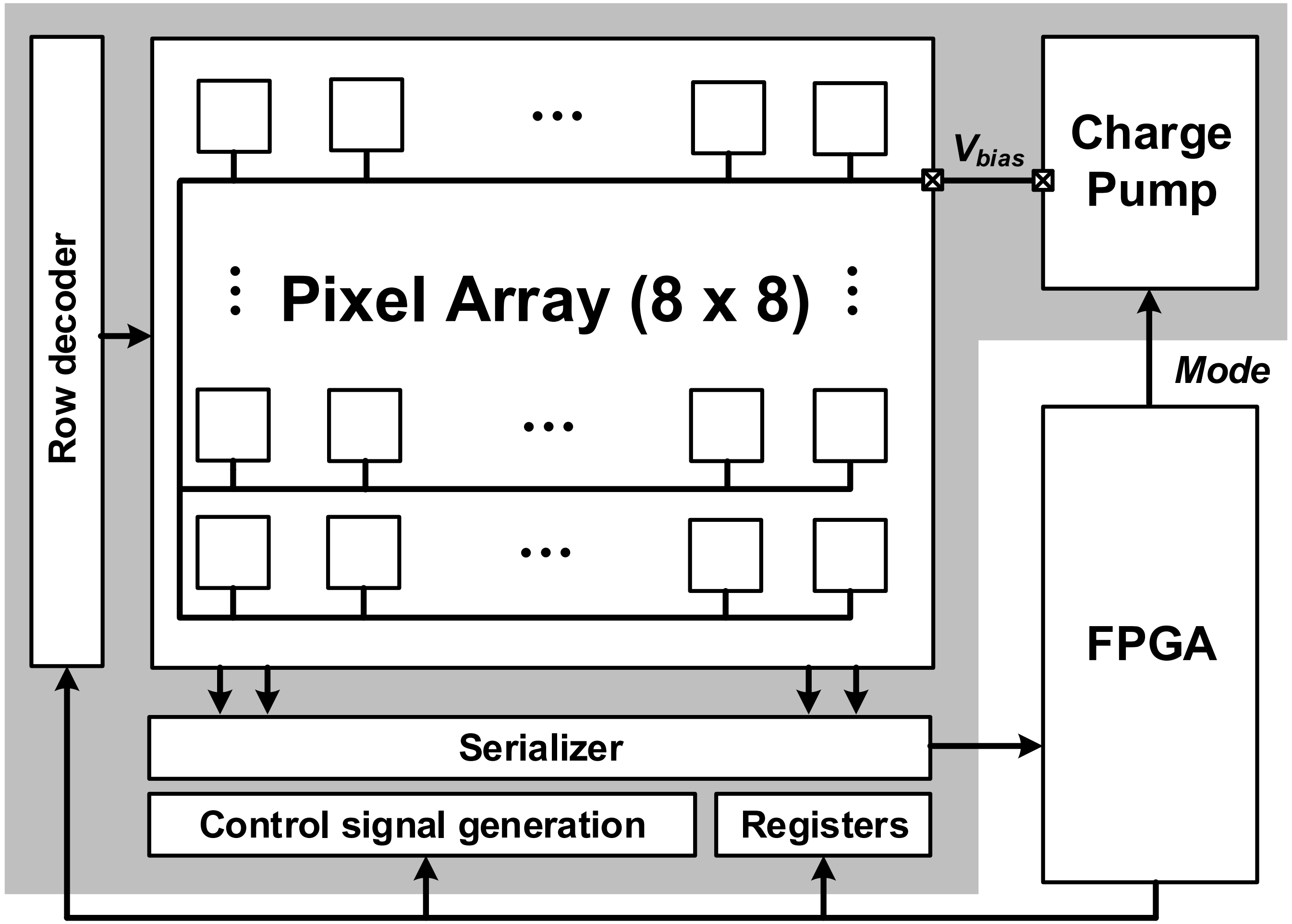
Inverter-based I-to-F Converter





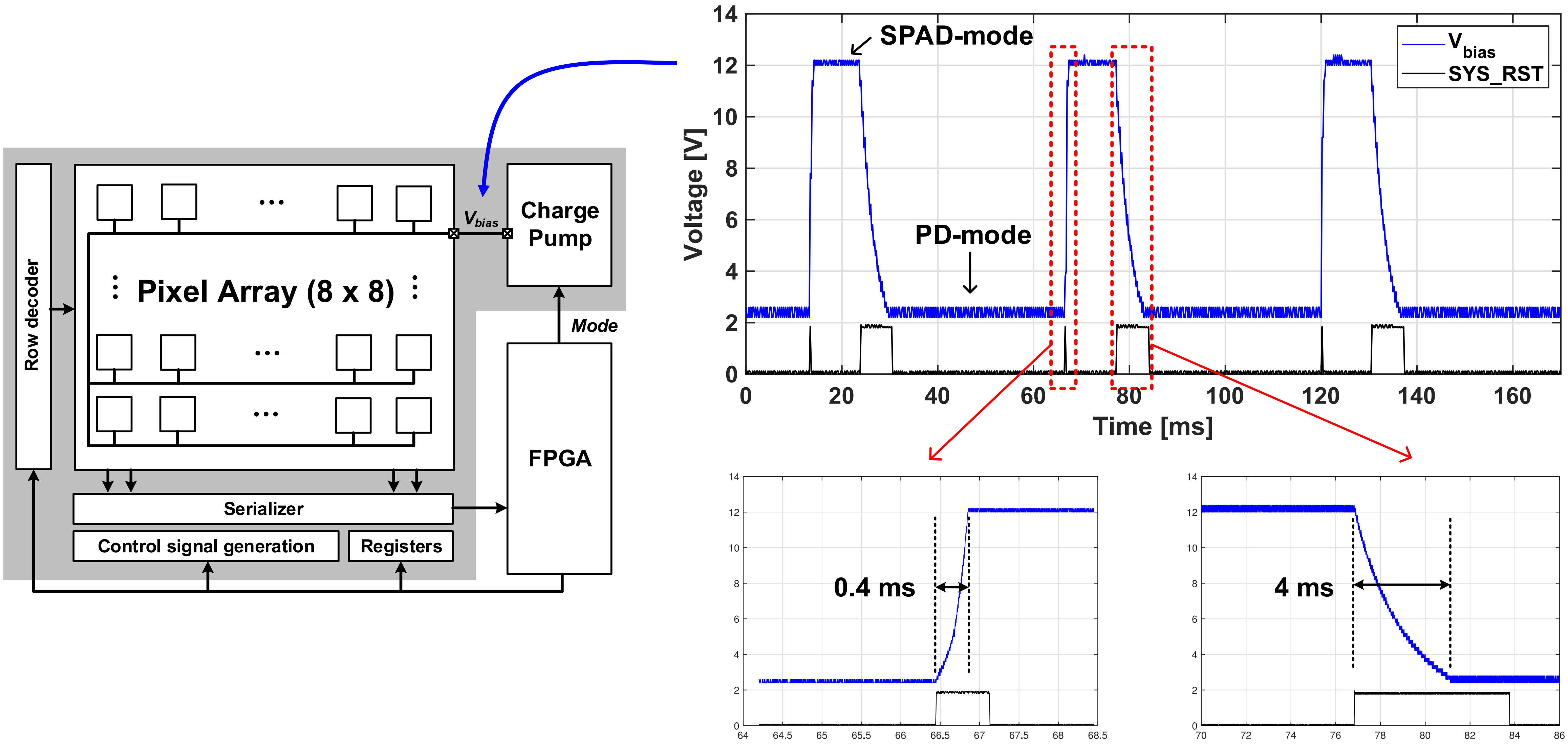
- ☺ Small number of transistors
- ☺ No need for an external bias
- ☺ Wide dynamic range at LV supply

High-level Array Architecture



Fully parallel readout with in-pixel dual-mode detectors

Alternate Dual-Frame Operation



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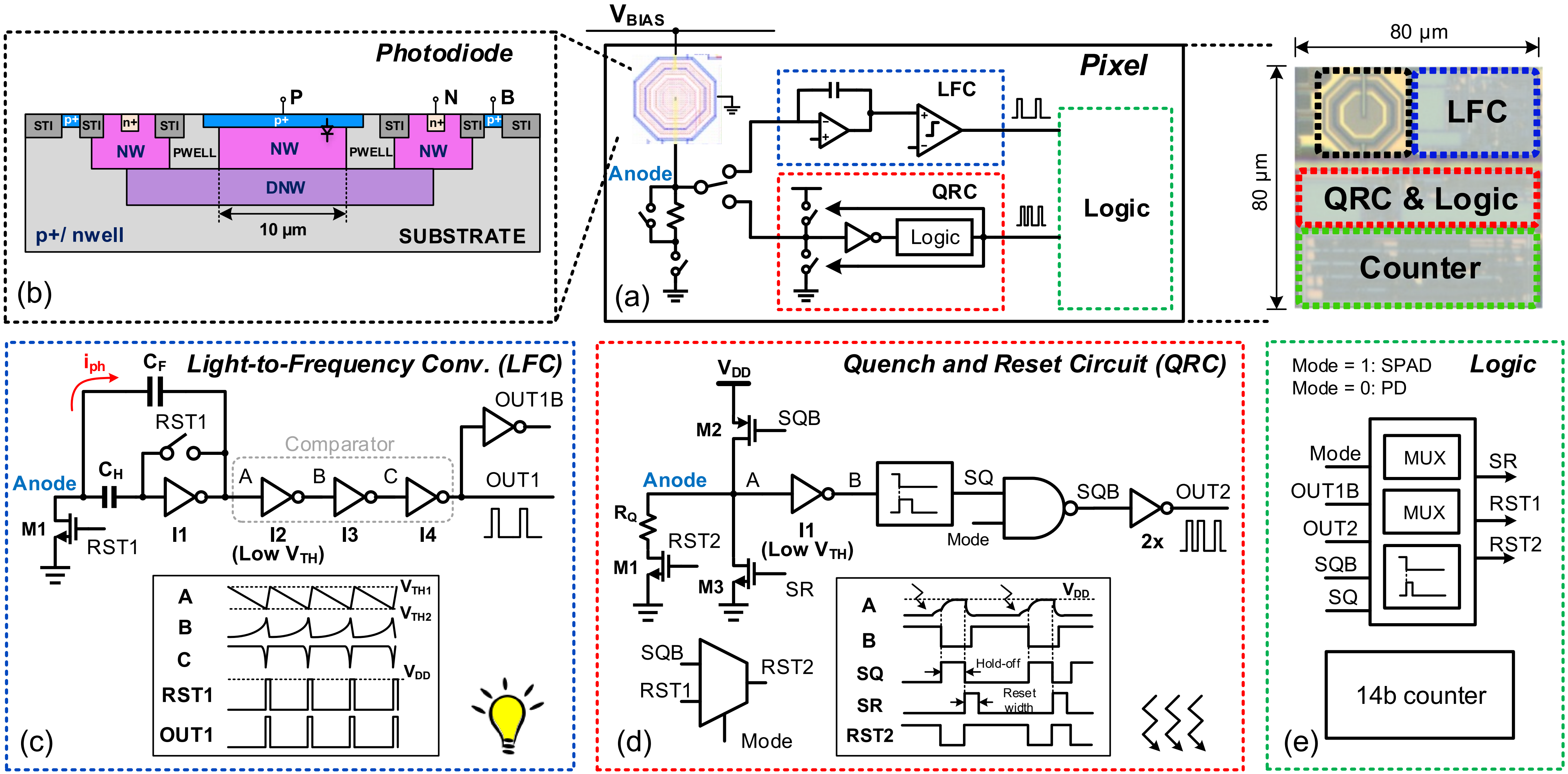
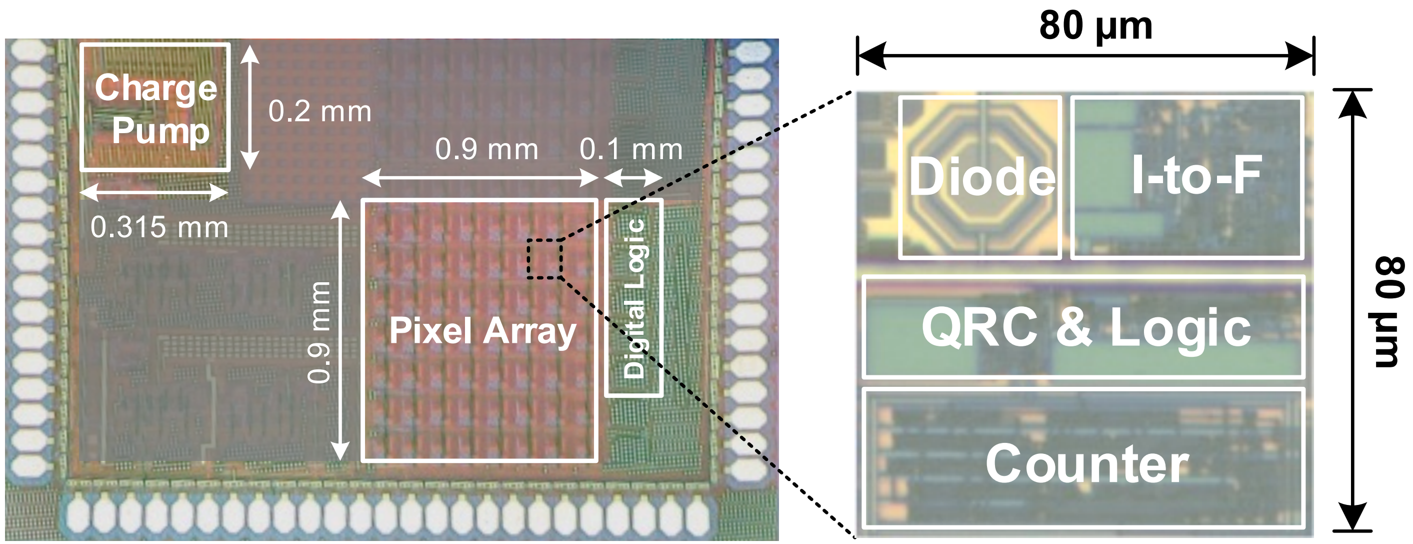
Dual-Mode Geiger/Linear Pixel



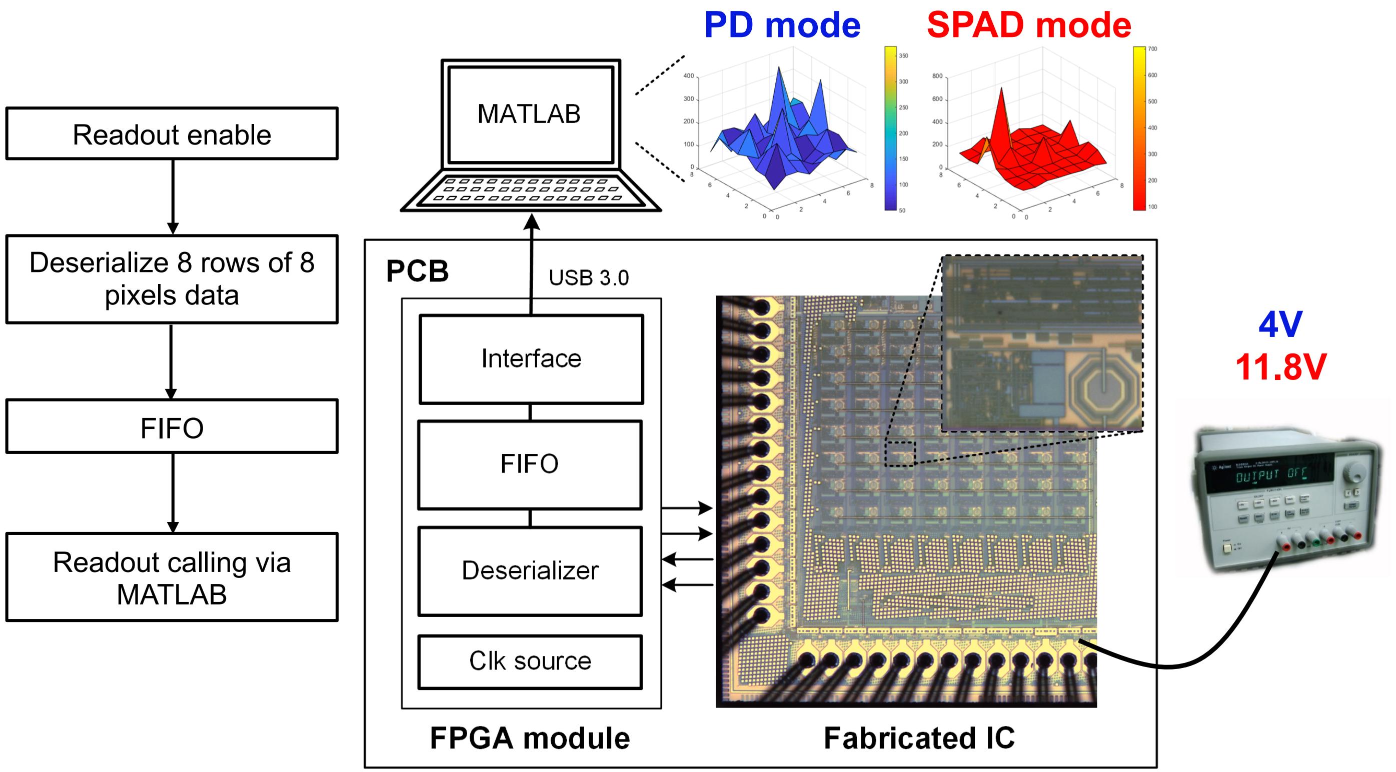
Chip Summary

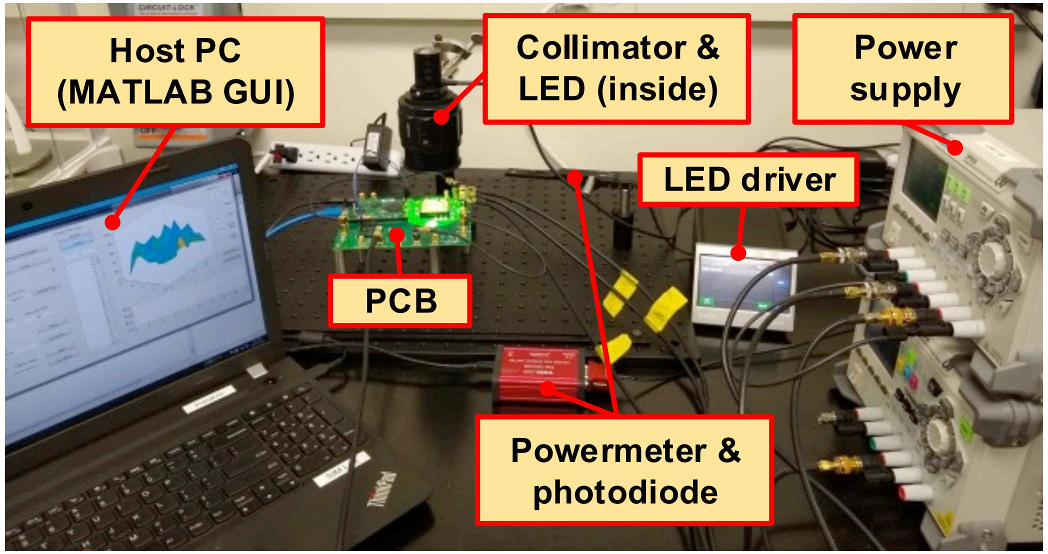


Process	0.18 µm CMOS
Area	0.9 mm^2
Array Dimension	8 x 8
Pixel Area	80 x 80 um^2
Frame Rate	100 fps (SPAD) 30 fps (PD)
Power @ Dark	2.3 mW (SPAD) 2.75 mW (PD)
Core Supply	1.8 V

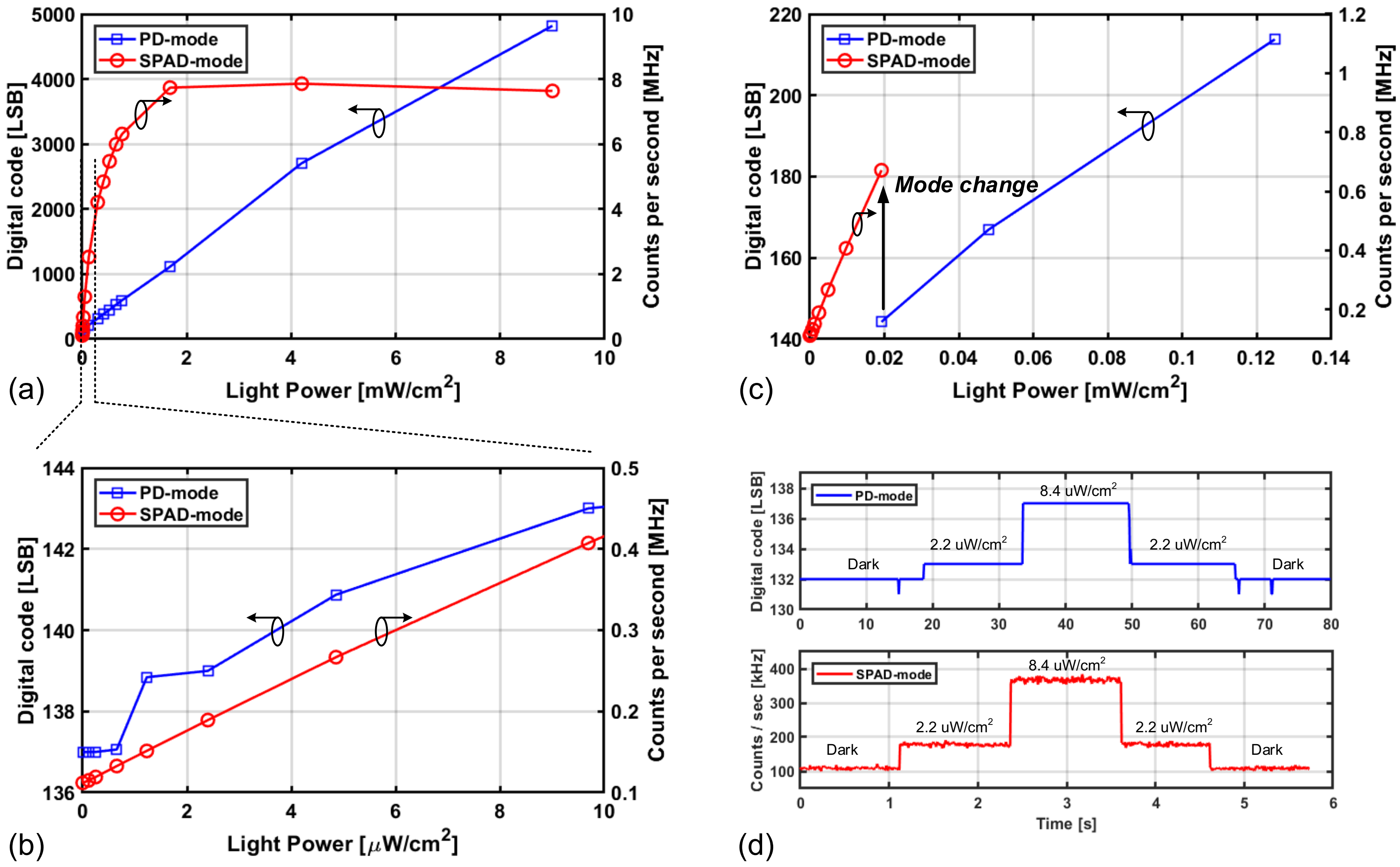
H. Ouh, B. Shen, and M.L. Johnston, "Combined in-pixel linear and single-photon avalanche diode operation with integrated biasing for wide-dynamic-range optical sensing," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 392-403, 2020.

Measurement Setup



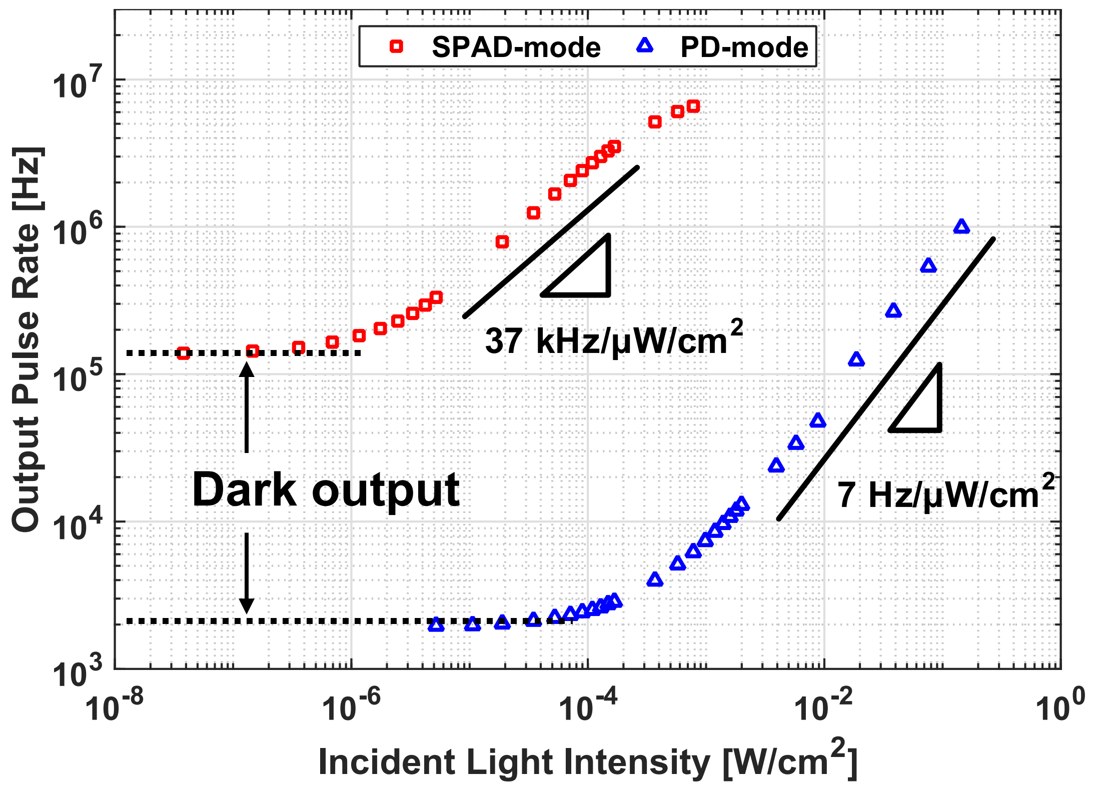


Preliminary Measurements



Optical Sensitivity

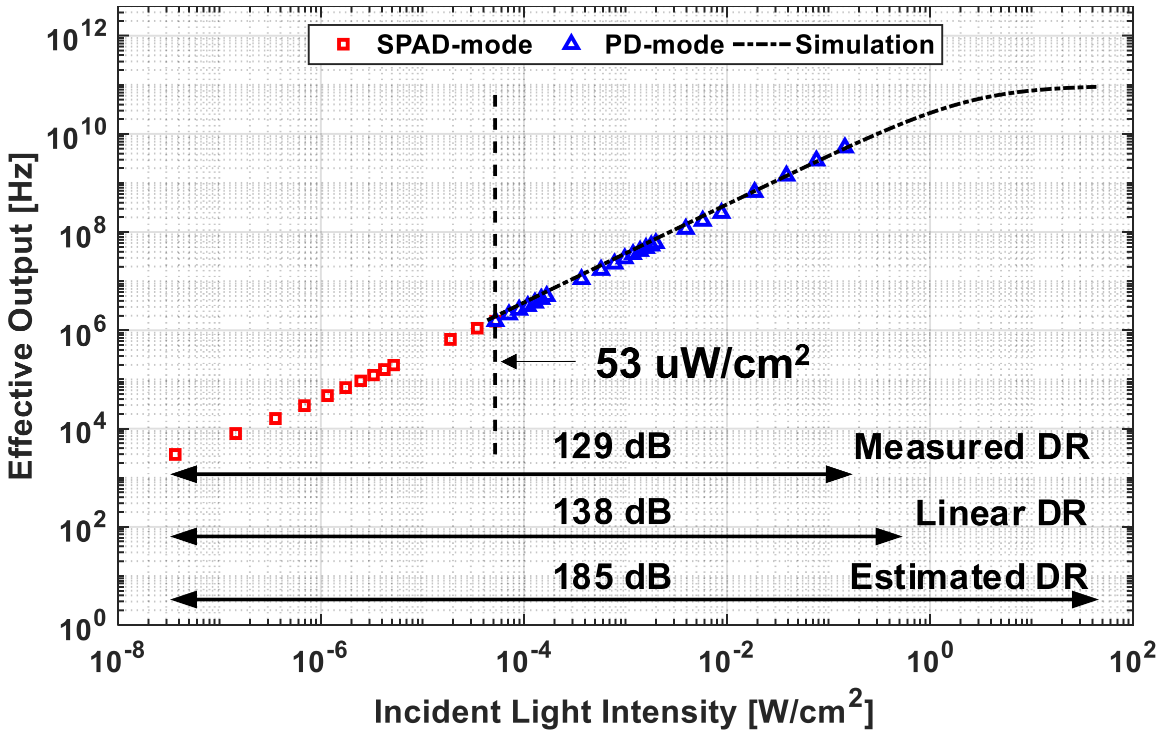
- ❑ **Output pulse rate at each mode for varying light intensity**

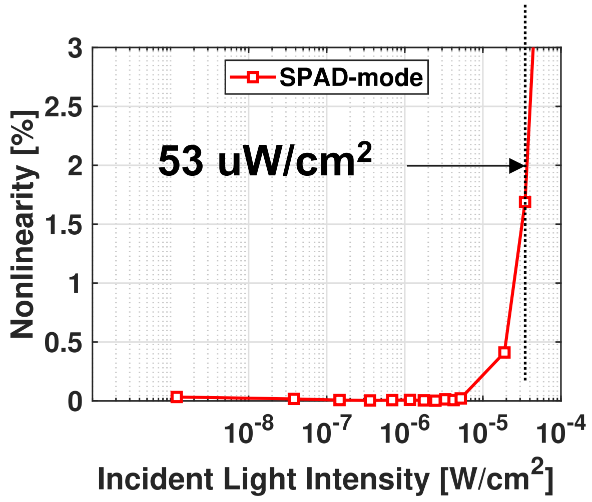


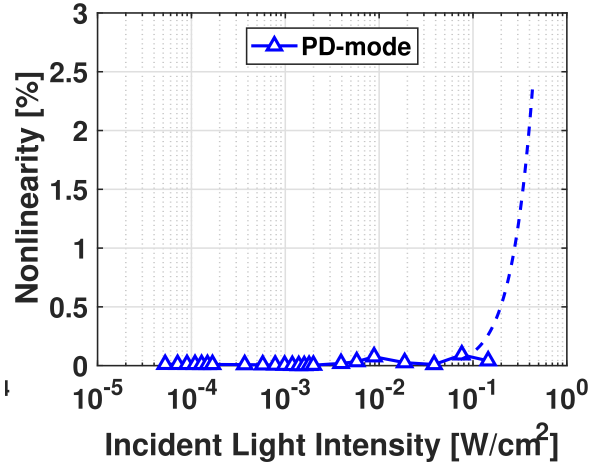
	Sensitivity
SPAD-mode @ 100Hz	37 kHz/uW/cm^2
PD-mode @ 30Hz	7 Hz/uW/cm^2
Gain Ratio	5,400

Dual-Mode Optical Dynamic Range

- ❑ **Combined final output (PD-mode gain adjusted)**

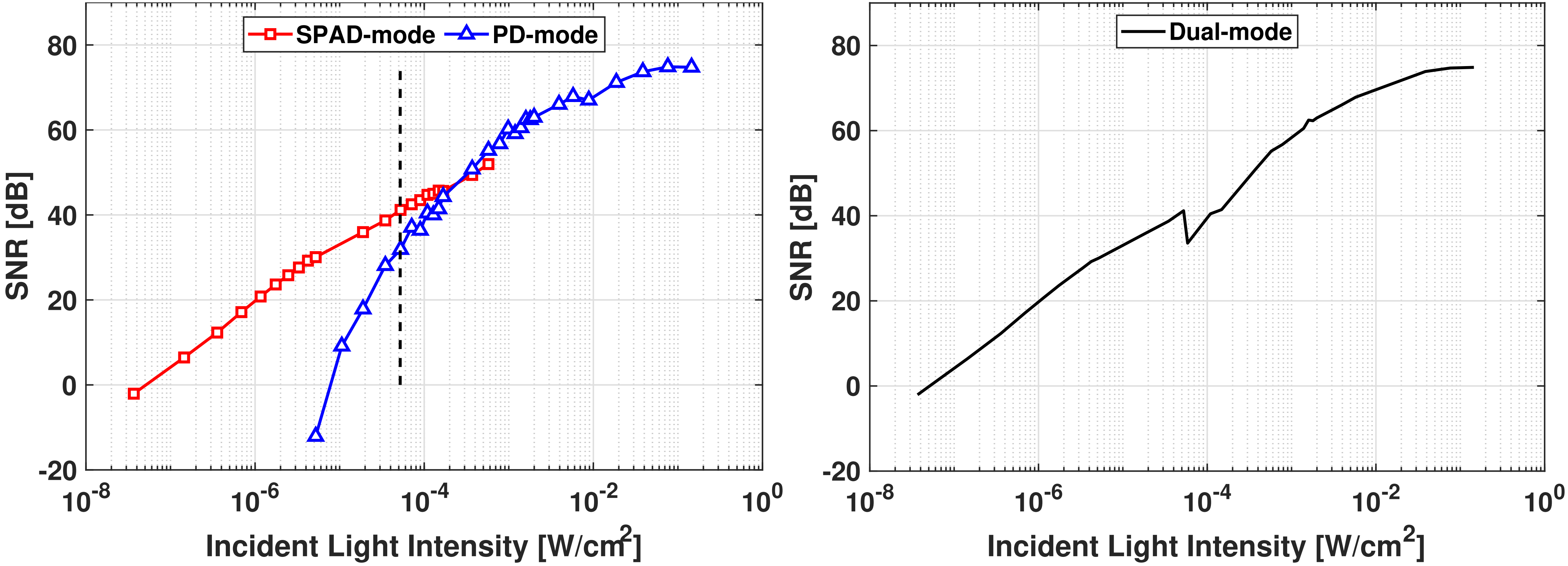






$$DR = 20\,log\frac{Max.Signal}{Min.Signal\ @dark}$$

Dual-Mode Signal-to-Noise Ratio



Performance Comparison

Reference	Wang et al., *TED*, 2006	Manickam et al., *JSSC* 2017	Dutton et al., *Sensors* 2018	Mori et al., *ISSCC* 2016	**This Work**
Process	180 nm CMOS	130 nm	40 nm FSI	110 m BSI	**180 nm CMOS**
Array Size	28 x 28	32 x 32	96 x 40	1280 x 720	**8 x 8**
Pixel Size	23 μm	100 μm	8.25 μm^a	3.8 μm	**80 μm**
Fill-factor	25 %	25 %	66 % / 26 %[a]	-	**0.8 %**
Diode Operation	PD	PD	SPAD	APD/PD	**SPAD/PD**
Readout Architecture	In-pixel	In-pixel	In-pixel	APS column readout	**In-pixel**
Frame Rate (FPS)	30	1	240[b]	30 (APD) 30 (PD)	**100 (SPAD) 30 (PD)**
Optical Dynamic Range (dB)	110	116	99.6[b] @OSR=256	1 photon (APD) 60 (PD)	**129**
Photons Detection Range (photons/cm^2·s)[c]	10^{13}-10^{17}	10^{10}-10^{15}	-	10^{8}-10^{13}	**10^{11}-10^{18}**
Dark Signal	-	20 fA	150 cps	0.1 cps	**135 kcps**
Max. SNR (dB)	<60[d]	<80[e]	52	-	**75**
Power Consumption per pixel [f]	0.25 μW	115 μW	-	-	**36 μW (SPAD) 40 μW (PD)**
Interface Data Rate per pixel	-	100 kbps	46 kbps	-	**5.6 kbps (SPAD) 560 bps (PD)**
Integrated HV-LV Bias	-	-	N	N	**Y**

[a] Readout circuits are separate, and the fill-factor was calculated as the ratio of imaging array area to whole chip area.
[b] Estimated from summary table for a 1M-pixel HDR QIS reported in the reference.
[c] Converted from reported lux or intensity (W/cm^2·s) to photon flux, or estimated from values in the reference if optical sensing range is not explicitly provided.
[d] Estimated from ADC resolution; [e] estimated from a measured SNR plot; [f] total power including core and I/O power normalized to number of channels.

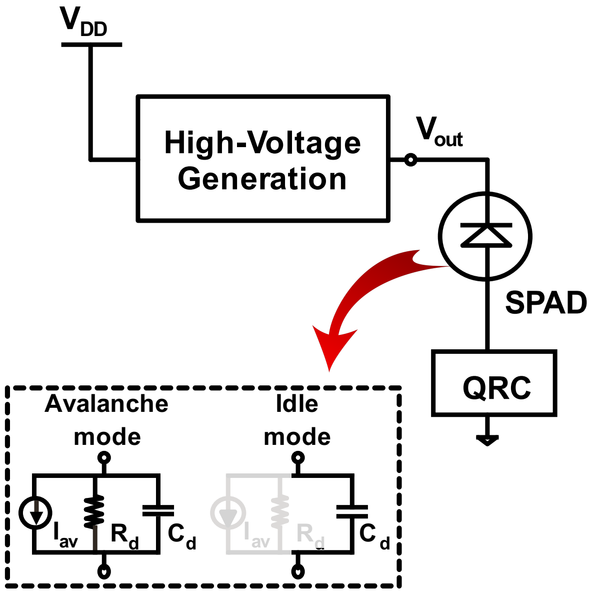
H. Ouh, B. Shen, and M.L. Johnston, "Combined in-pixel linear and single-photon avalanche diode operation with integrated biasing for wide-dynamic-range optical sensing," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 392-403, 2020.

Outline

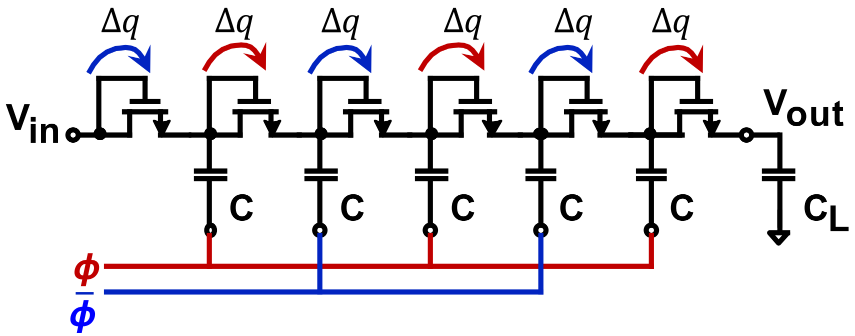
Boyu Shen
Ph.D. Candidate

- ❑ Motivation & Background
- ❑ In-Pixel Wide Dynamic Range Optical Sensor Array
- ❑ **On-Chip High-Voltage and Low-Voltage Bias Generation**

HV Biasing Considerations for SPAD Arrays



Electrical equivalent model of SPAD

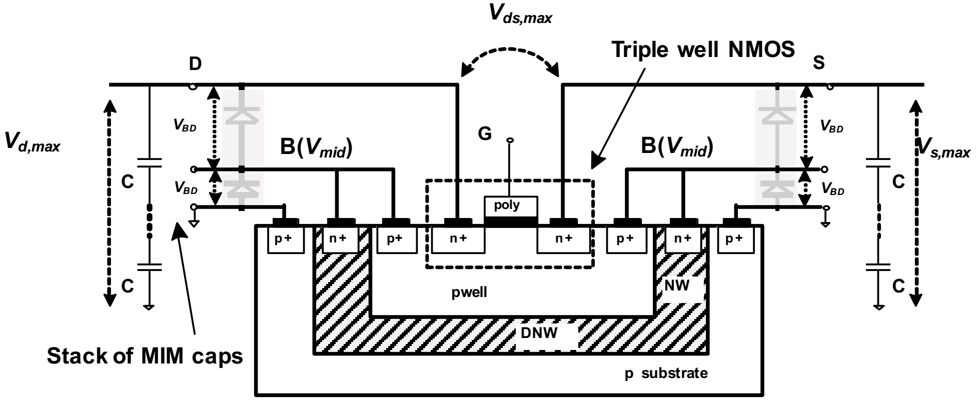


Challenges

- Low breakdown voltage of MOS (<5V)
- Large area due to low density MIM caps
- Closed-loop regulation with high output voltage

Addressing low breakdown voltage of MOS

- Triple well NMOS switches
- Increasing V_{BODY} in later charge pump stages
- Thick oxide NMOS for higher V_{DS} across switches



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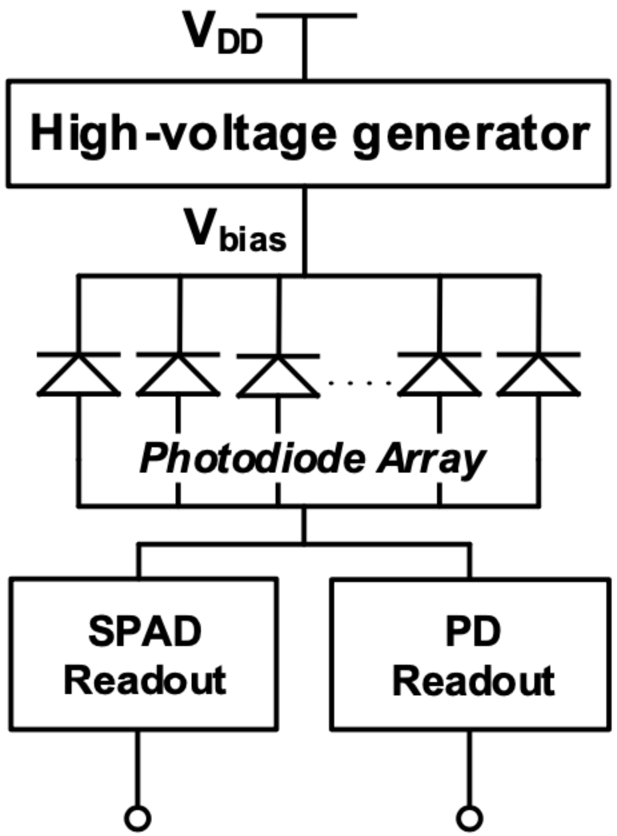

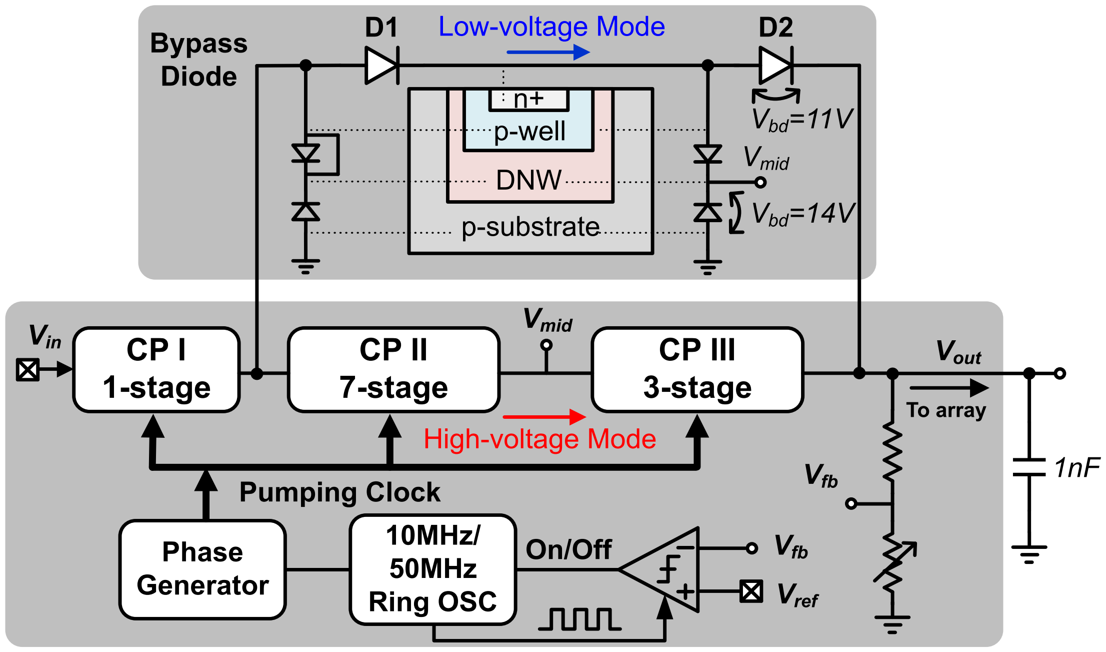

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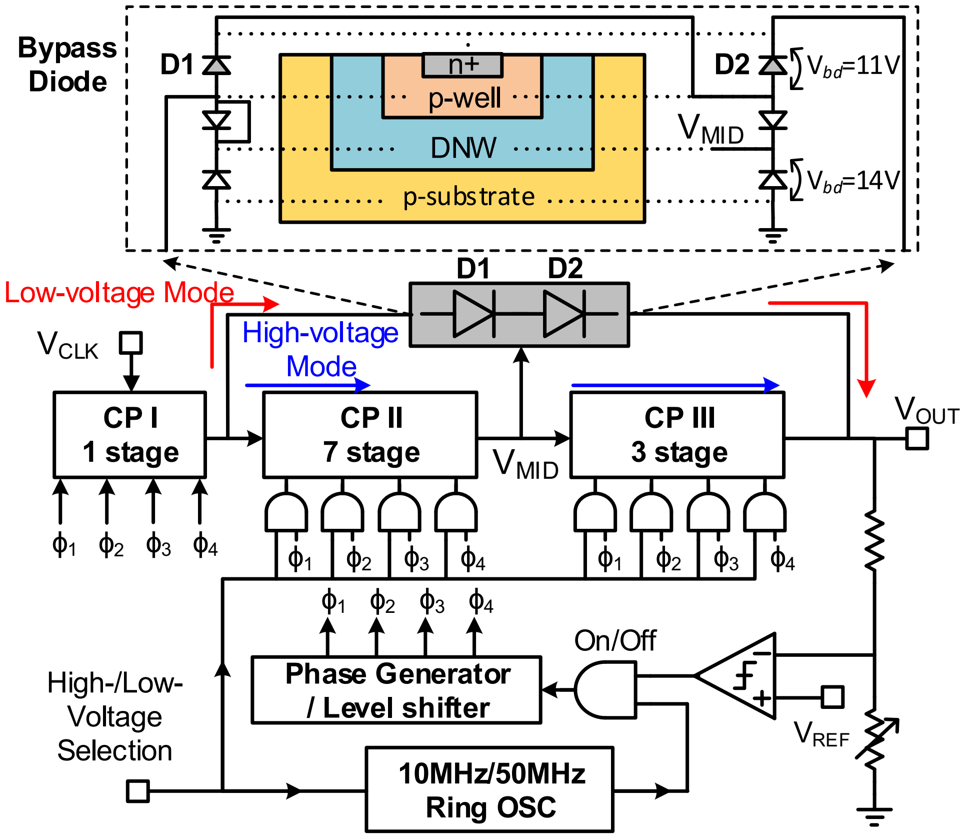
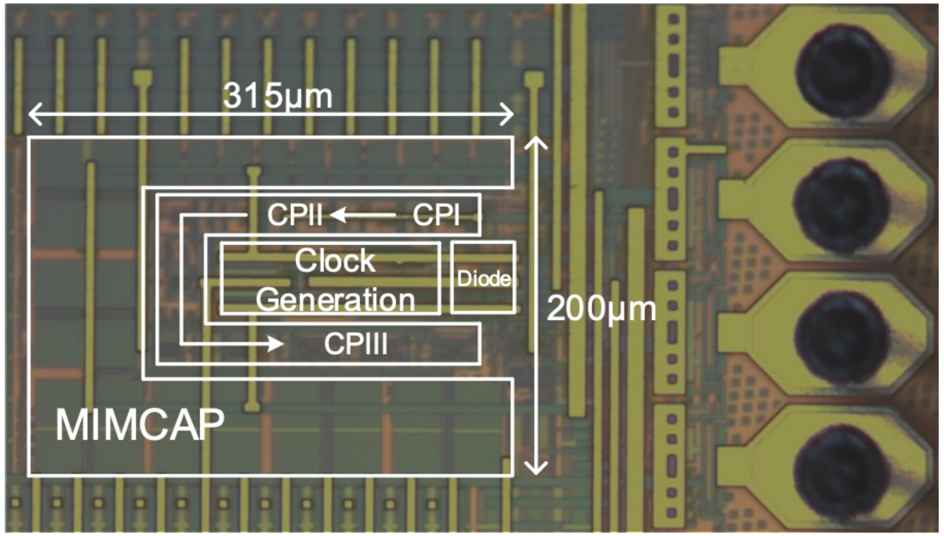
Dual-mode HV-LV Charge Pump

Dual-mode HV generation system architecture



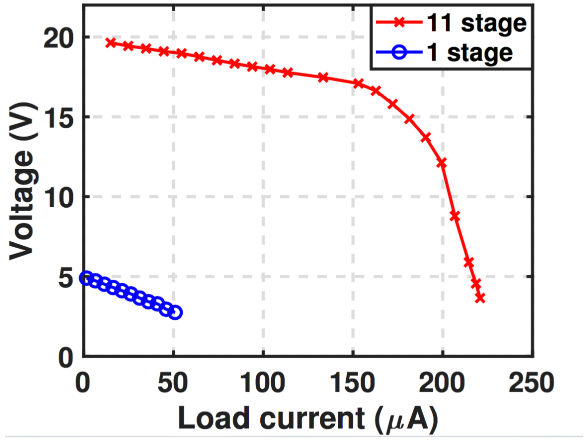


- Single voltage source for efficient, dual-mode high (>10V) and low(<5V) voltage generation.
- A high voltage triple-well diode structure is proposed to reconfigure the high voltage and low voltage output.
- Frequency and feedback ratio tuning to improve efficient operation in both HV and LV modes.

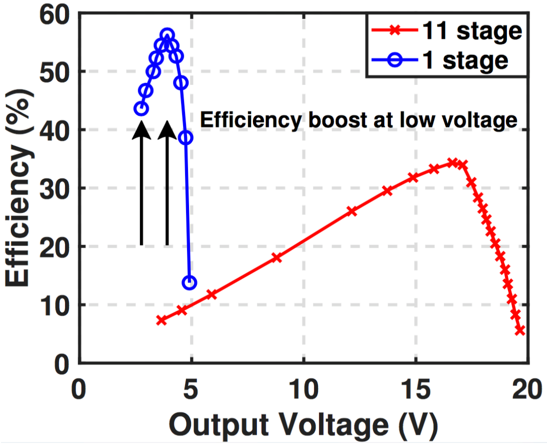
B. Shen, S. Bose, and M.L. Johnston, "A 1.2V-20V closed-loop charge pump for high dynamic range photodetector array biasing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2018, vol. 66, no. 3, pp. 327-331, 2019.

Dual-mode HV-LV Charge Pump

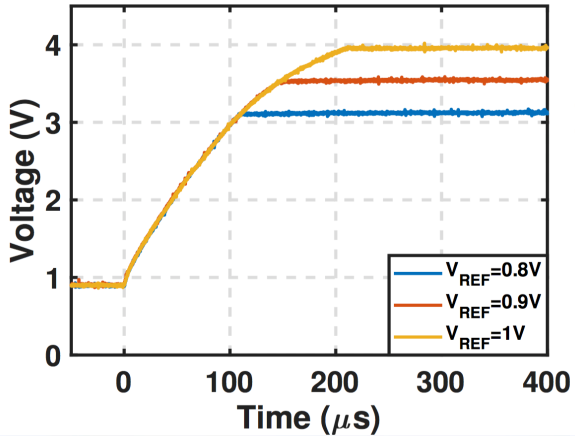
I-V characteristic



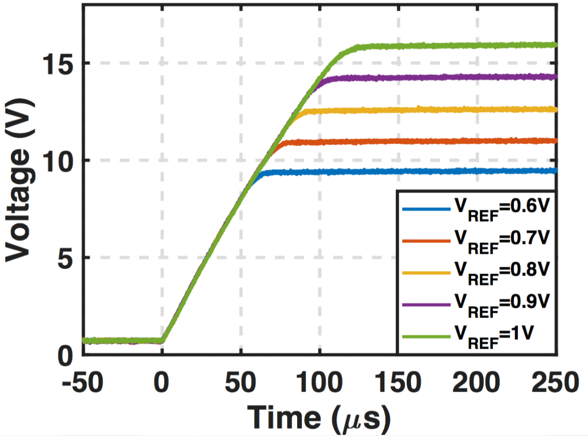
Efficiency versus Output voltage

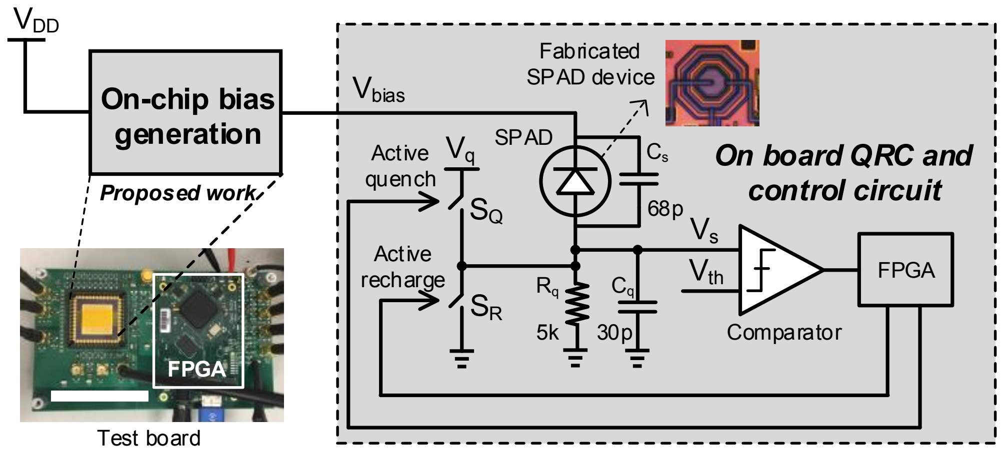


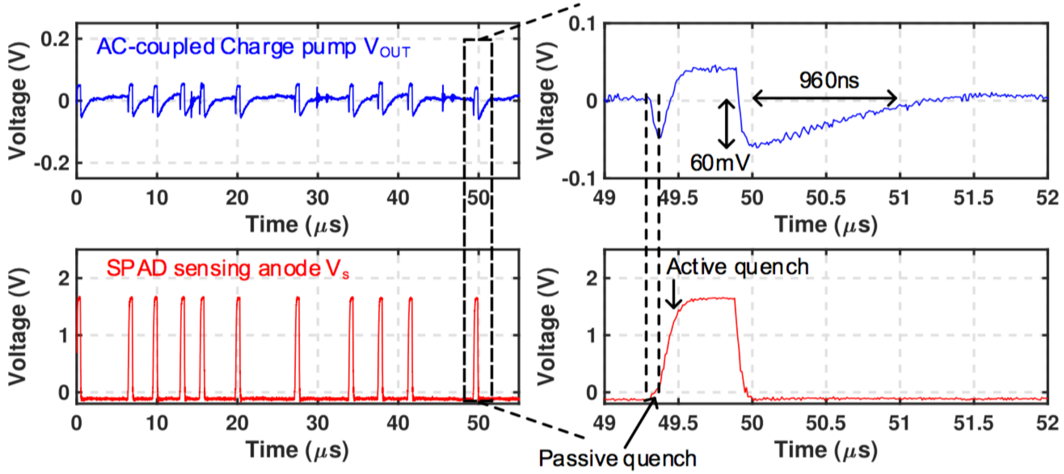
Low-voltage start-up



High-voltage start-up







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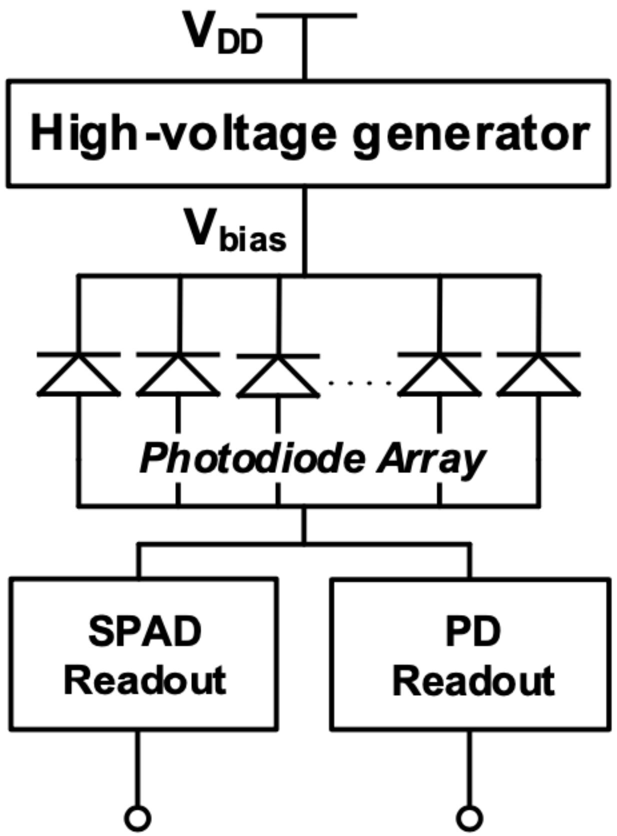
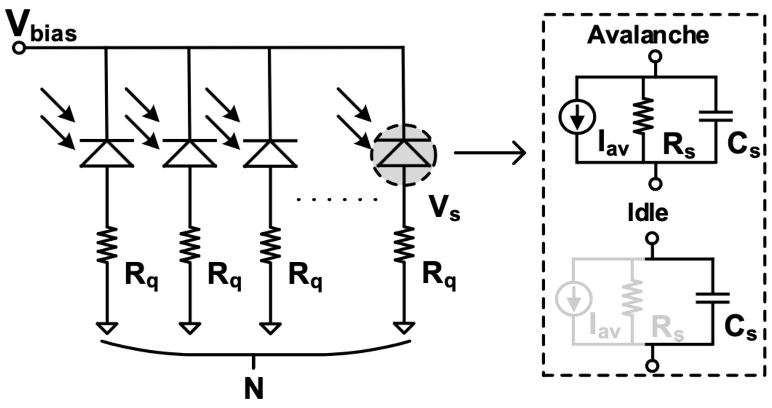
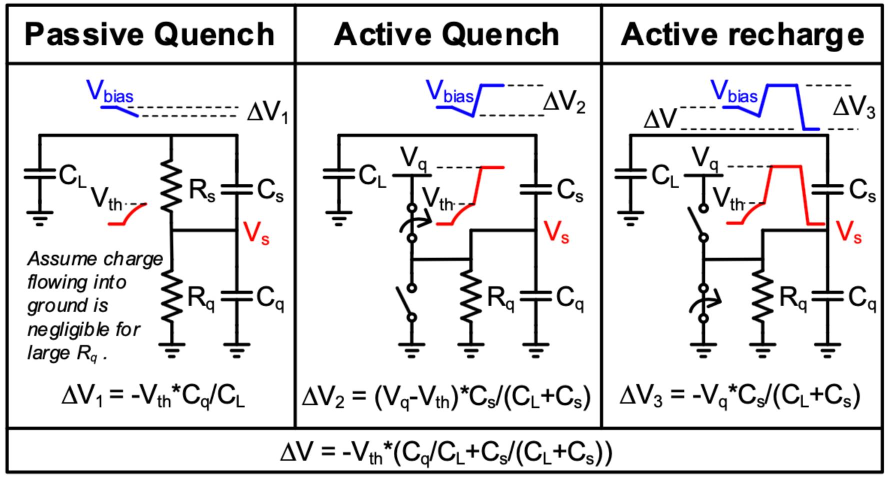
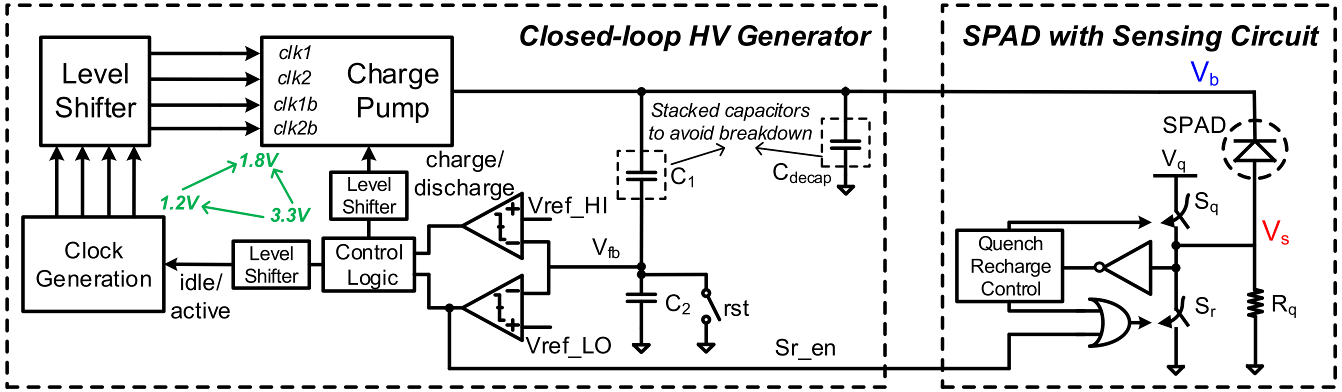
HV Biasing Considerations for SPAD Arrays

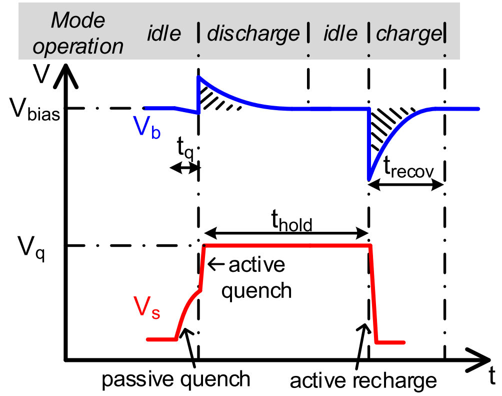


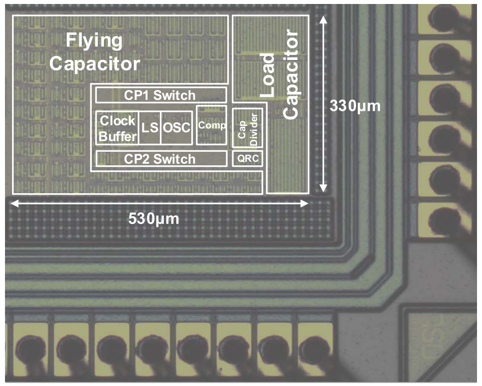


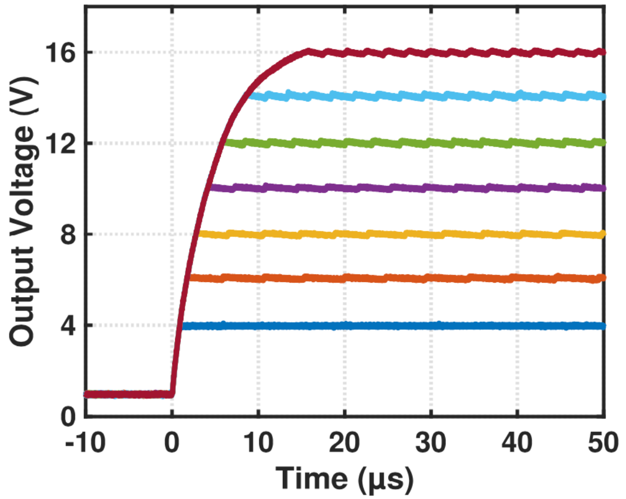


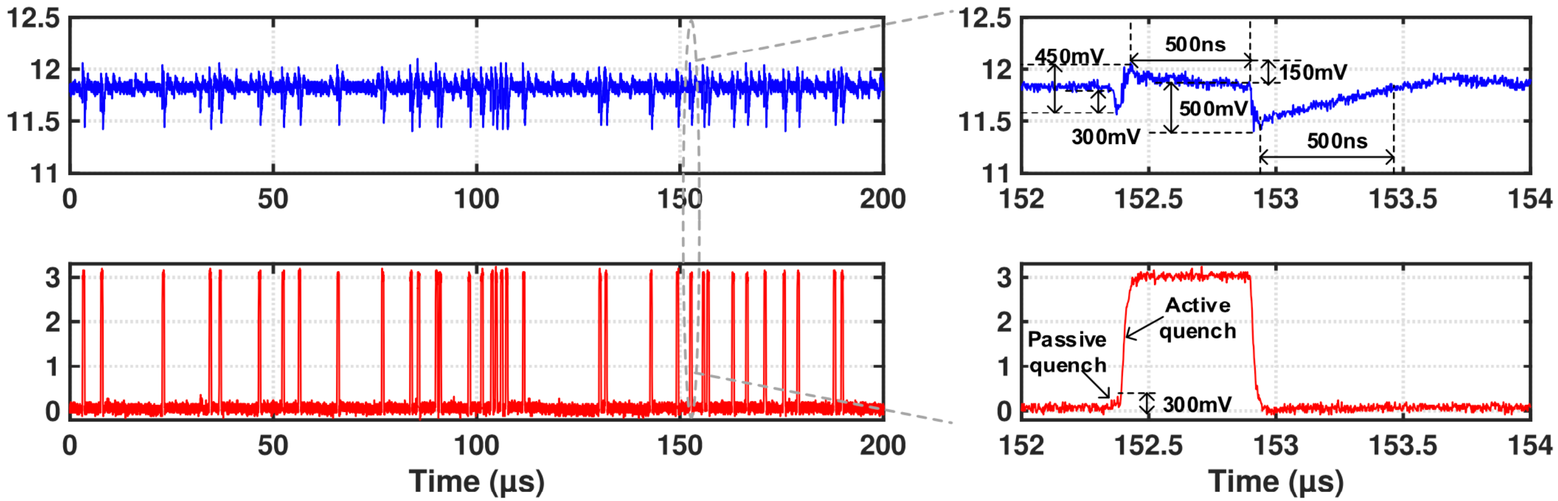
HV Charge Pump with Active Charge/Discharge











B. Shen, S. Bose, and M.L. Johnston, "Fully-integrated charge pump design optimization for above-breakdown biasing of single-photon avalanche diodes in 0.13 μm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 1258-1269, 2019.

Summary & Future Work

- Geiger-mode and linear-mode photodiode operation combined in-pixel for >129dB optical dynamic range
- On-chip high-voltage and low-voltage biasing in low-voltage CMOS
- Fully standalone pixel architecture with small-area integrated biasing promising for optical detection in bio/chemical applications

Related Publications

1. H. Ouh, B. Shen, and M.L. Johnston, "Combined in-pixel linear and single-photon avalanche diode operation with integrated biasing for wide-dynamic-range optical sensing," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 392-403, 2020.
2. B. Shen, S. Bose, and M.L. Johnston, "A 1.2V-20V closed-loop charge pump for high dynamic range photodetector array biasing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2018, vol. 66, no. 3, pp. 327-331, 2019.
3. B. Shen, S. Bose, and M.L. Johnston, "Fully-integrated charge pump design optimization for above-breakdown biasing of single-photon avalanche diodes in 0.13 μm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 3, pp. 1258-1269, 2019.
4. S. Bose, H. Ouh, S. Sengupta, and M.L. Johnston, "Parametric study of p-n junctions and structures for CMOS-integrated single-photon avalanche diodes," *IEEE Sensors Journal*, vol. 18, no. 13, pp. 5291-5299, 2018.
5. H. Ouh and M.L. Johnston, "Dual-mode, in-pixel linear and single-photon avalanche diode readout for low-light dynamic range extension in photodetector arrays," *IEEE Custom Integrated Circuits Conference (CICC),* San Diego, CA, pp. 1-4, Apr. 2018.
6. H. Ouh, S. Sengupta, S. Bose, and M.L. Johnston, "Dual-mode, enhanced dynamic range CMOS optical sensor for biomedical applications," *IEEE Biomedical Circuits and Systems Conference (BioCAS),* Turin, Italy, pp. 1-4, Oct. 2017.
7. B. Shen, S. Bose, and M.L. Johnston, "On-chip high-voltage SPAD bias generation using a dual-mode, closed-loop charge pump," *IEEE International Symposium on Circuits and Systems (ISCAS),* Baltimore, MD, pp. 1-4, May 2017.

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Combining linear and SPAD-mode diode operation in-pixel for wide dynamic range CMOS optical sensing

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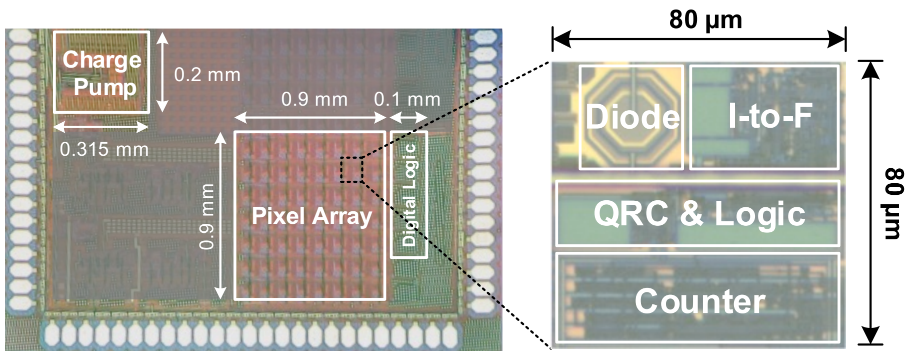

Thanks!

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