3D Integrated Front Side Illuminated **Photon-to-Digital Converters:** Status and Applications

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GRAMS

What is a Photon-to-Digital Converter - PDC

A Photon-to-Digital Converter (PDC) is a SPAD array read out by a CMOS pixelated circuit with embedded digital signal processing.

- The name “PDC” is inspired from “Analog-to-Digital Converter”.
- Digital signal processing can be simple or advanced:
  - Photon/Triggered SPAD counts,
  - Time stamping,
  - Timing skew correction, sorting, dark count filter,
  - Advanced algorithms embedded in CMOS for online processing (e.g.: Gauss-Markov estimator).

-Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs, Lemaire, Nolet, Dubois, C. Therrien, Pratte, Fontaine, NIM:A, Vol. 959, 2020, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2020.163538
-A 256 Pixelated SPAD readout ASIC with in-Pixel TDC and embedded digital signal processing for uniformity and skew correction, Nolet, Lemaire, Dubois, Roy, Carrier, Samson, Charlebois, Fontaine, Pratte, NIM:A, Vol. 949, 2020, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2019.162891

Photon-to-Digital Converter Implementation Schemes

Back side illumination

Front side illumination

Why is front side illuminated PDC relevant?

For optimal Single Photon Timing Resolution (SPTR)

Ultimate target: sub 10-ps SPTR (SPAD + CMOS readout)

SPAD designed for:

- Minimum drift between photoelectron interaction and the high E field avalanche region
- Minimum drift time variation (= jitter)
- Uniformed E field
- Spectral sensitivity < 650 nm; UV and VUV also of interest (more later in this talk)

Why Targeting 10 ps Single Photon Timing Resolution?

For Medical Imaging

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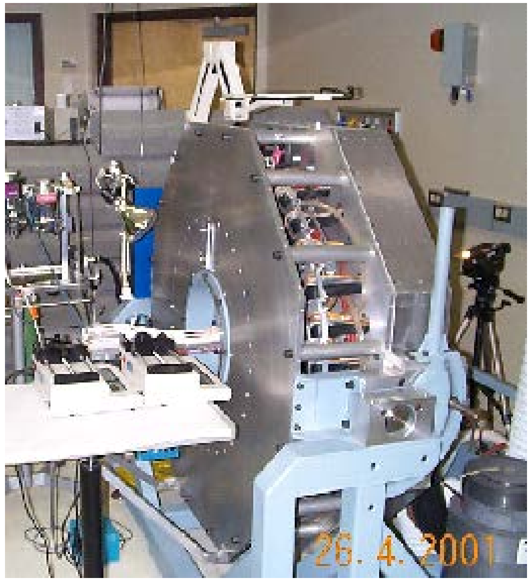
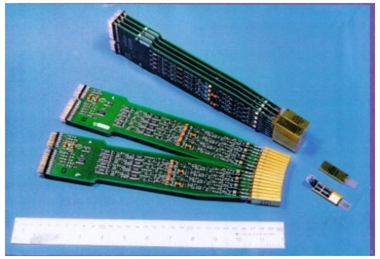
Medical Imaging @ Sherbrooke: Positron Emission Tomography

BGO Scanner (1995-2009) ✓ 1st APD-based PET scanner in the world




8-channels front-end board

2.1 mm
~14 µl

LabPET™(2005) ✓ 1st APD-based commercial PET scanner

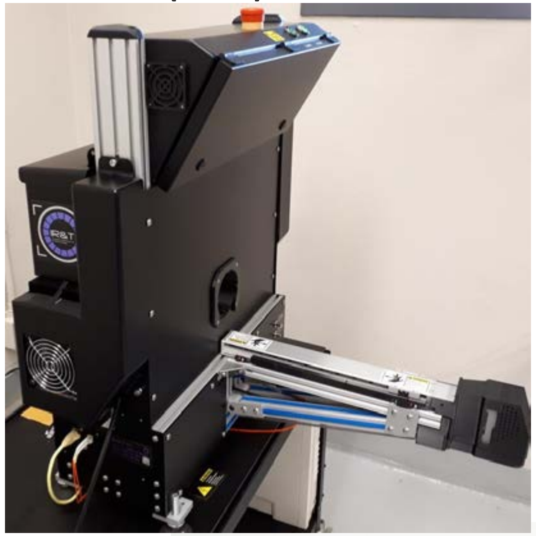

64-channels front-end board and digitizer

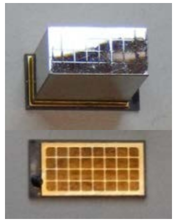
1.35 mm
~2.4 µl

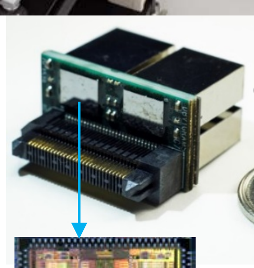
IR&T

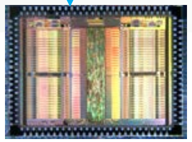
https://imagingrt.com/

LabPET II™(2015) ✓ 1st Commercial scanner with sub-mm resolution



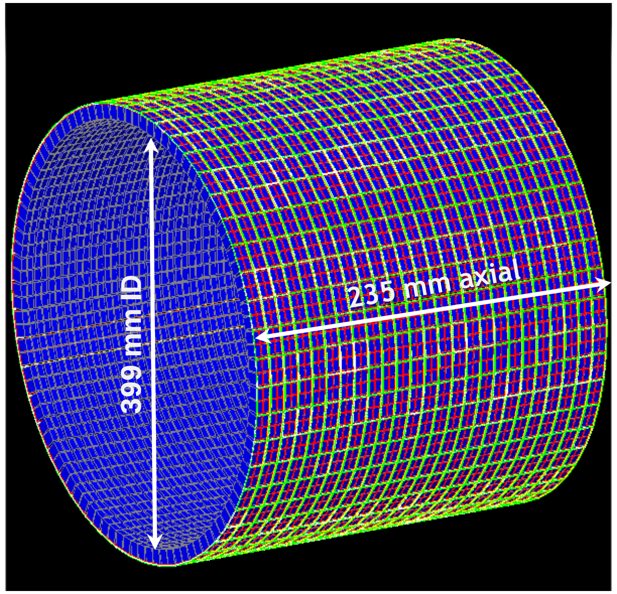

32 pixels APD


128-channels detector module


64-channels ASIC

0.73 mm
~0.4 µl

UHR™(2020) ✓ Brain scanner



1,008 modules
129,024 channels

1.3 mm
~2.1 µl

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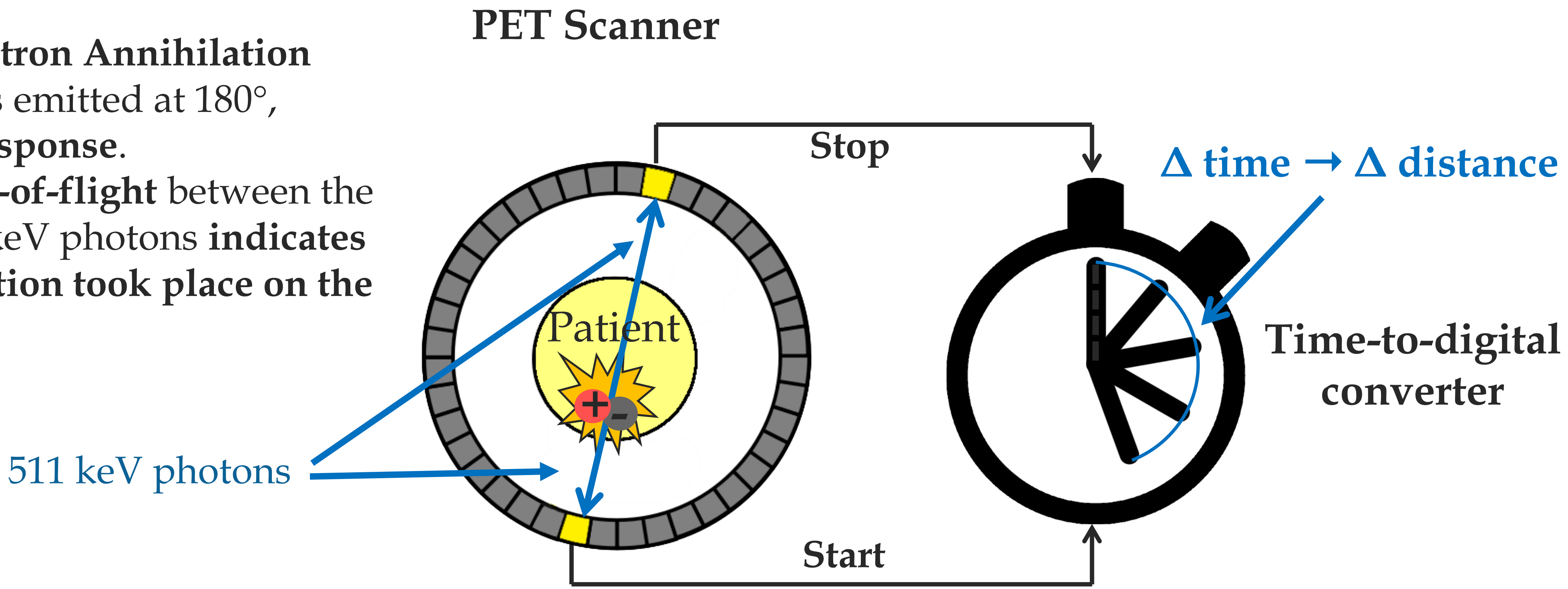
Time-of-Flight in Positron Emission Tomography Medical Imaging

How does PET works?

Positron-Electron Annihilation

→ 2 x 511 keV photons emitted at 180°, creating a **line of response**.

→ Measuring the **time-of-flight** between the arrival of both 511 keV photons **indicates where the annihilation took place on the line of response**



10 ps FWHM coincidence timing precision => 1.5 mm spatial precision

PDC Single Photon Timing Resolution required: < 10 ps FWHM

Advantages of Time-of-Flight Positron Emission Tomography

Time-of-Flight:

- improve image's contrast,
- lower radiotracer dose,
- real-time imaging (reconstruction-less),
- **pediatric care**,
- …

- Roadmap toward the 10 ps time-of-flight PET challenge, Physics in Medicine & Biology, 2020, http://iopscience.iop.org/10.1088/1361-6560/ab9500
- https://the10ps-challenge.org/

Photon-to-Digital Converters for Particle Physics

…to Answer Fundamental Questions about Matter and our Universe.

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PDC to Enable Neutrino Physics and Dark Matter Discovery

- Liquid argon (87 K) and liquid xenon (165 K)
- Cryogenic operation - PDC operated in noble liquid
  - Low power
- Large area (5 to 200 m^2)
- VUV sensitivity required
  - Liquid argon: 125 nm (without wavelength shifter)
  - Liquid xenon: 178 nm

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Is the Neutrino its own Antiparticle (Majorana Particle) ?
Revolutionizing the Standard Model of Particle Physics

Following Art McDonald' 2015 Nobel prize, we know that **neutrino** has **mass**,
but the actual mass is **unknown**…

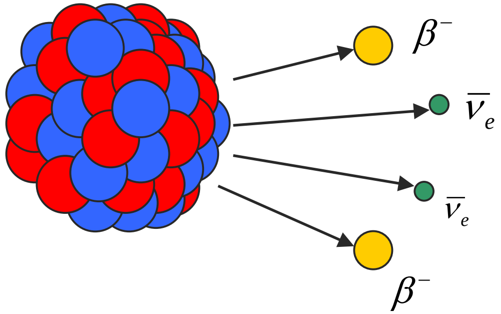
A **measurement** that would shed light both on the **actual mass** of a neutrino and the **origin** of this mass is the detection of a theoretical and extremely rare process known as
neutrino-less double beta decay (0νββ).

Additionally, observation of this process could shed light on another fundamental mystery: why in a **Big Bang** that started with **pure energy** we ended up with a **universe** composed almost entirely of **matter** but no **anti-matter**?

Standard model

2ν double β - decay

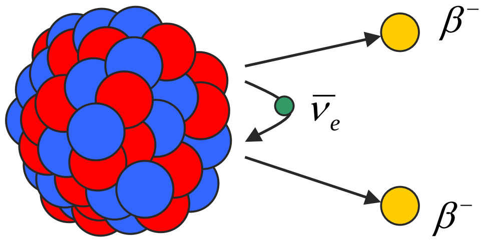
$$2\,n \rightarrow 2\,p + 2\,\beta^- + 2\,\bar{\nu}_e$$



New physics

0ν double β - decay

$$2\,n \rightarrow 2\,p + 2\,\beta^- + 0\,\bar{\nu}_e$$



Lepton number conservation violated

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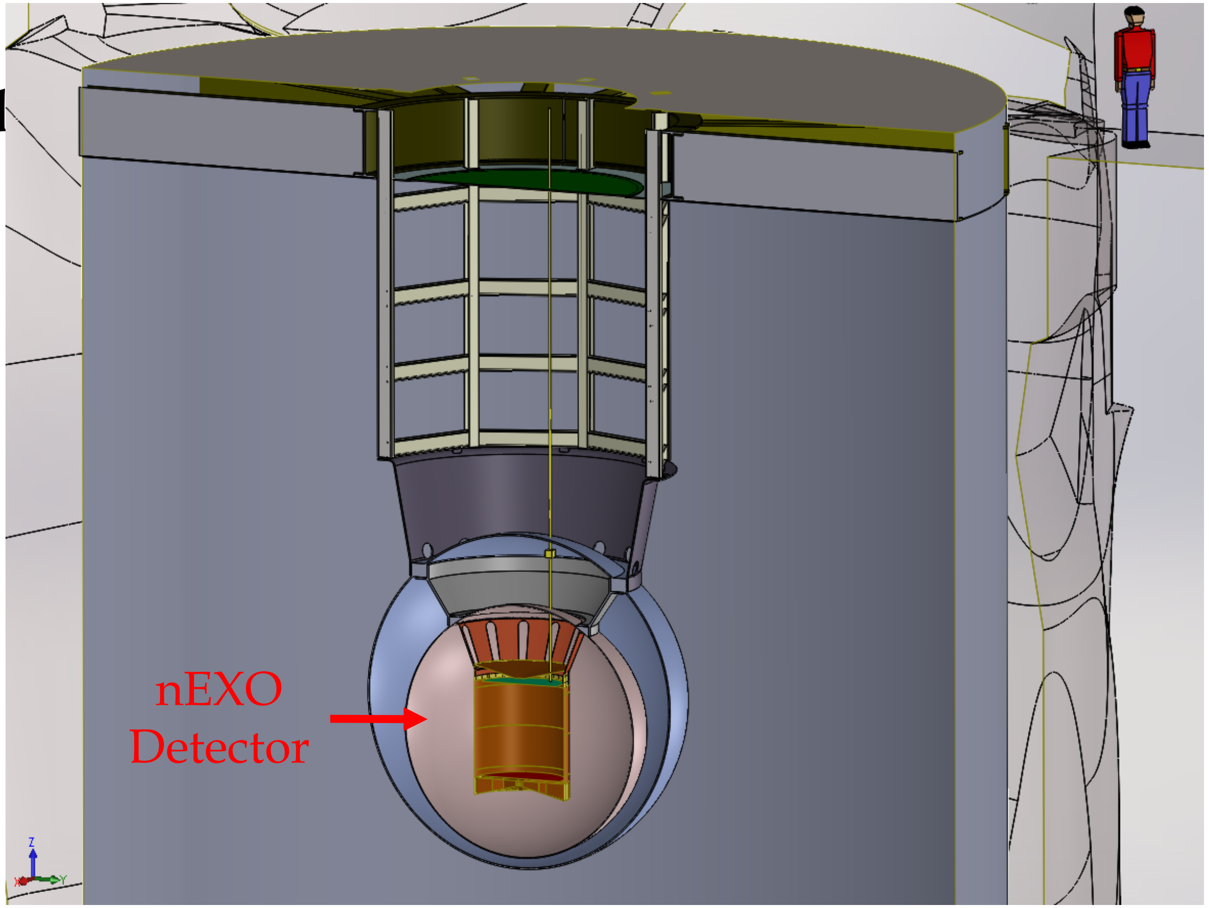
nEXO

nEXO – the next Enriched Xenon Observatory

- 2 km underground (SNOLAB, Sudbury, Canada, is considered)
  - Earth crust shields for cosmic background
- Measures
  - secondary electrons
  - LXe scintillation light (178 nm)
- Detector volume
  - 1.3 m Ø × 1.3 m
  - 5 t of enriched liquid Xenon-136
    - 165 K
  - **4.5 m² of photodetectors**
    - **100 W** power budget



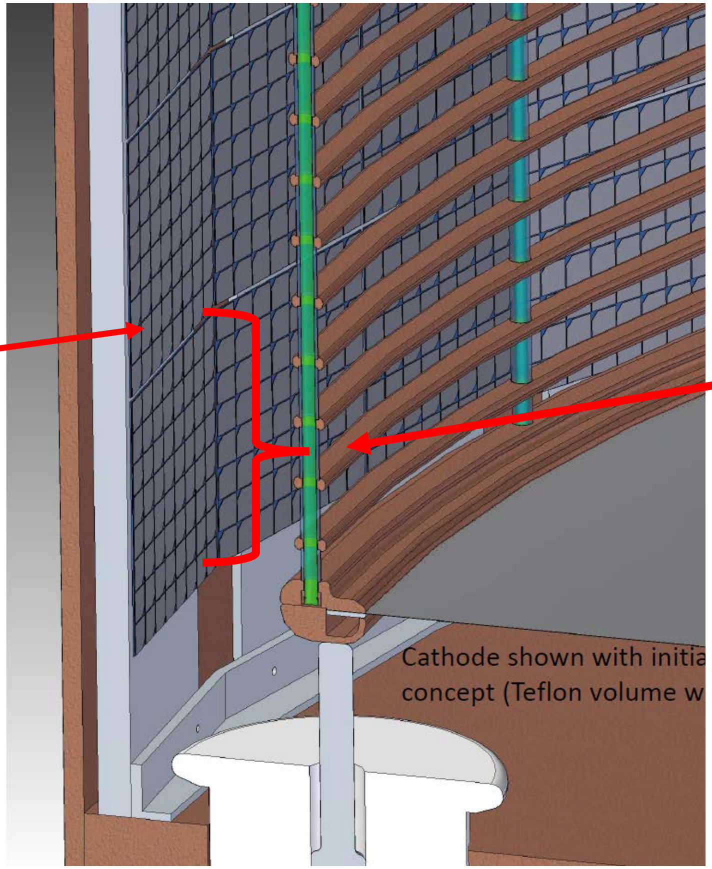
2016/06/27 nEXO Collaboration Meeting document - Allen House - Vessels/Mechanics summary

nEXO – Sherbrooke's Goal : PDC Photodetector Tiles

Photodetector barrel

<u>Baseline design:</u>
Analog SiPM (FBK or Hamamatsu)

<u>Sherbrooke's proposal:</u>
VUV-PDC on Silicon Interposer



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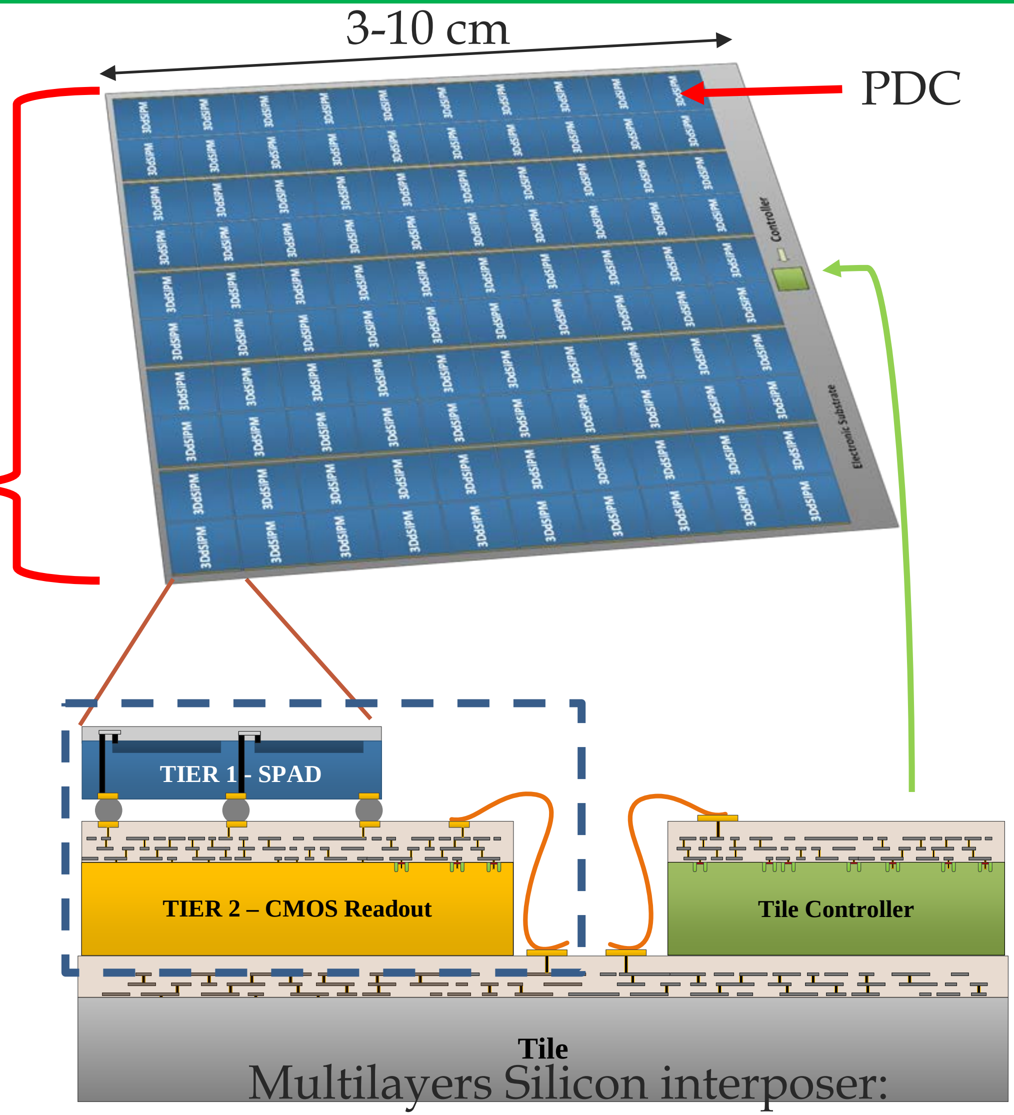


Multilayers Silicon interposer:
Matching the CTE of the tile

Development of the PDC Technology:

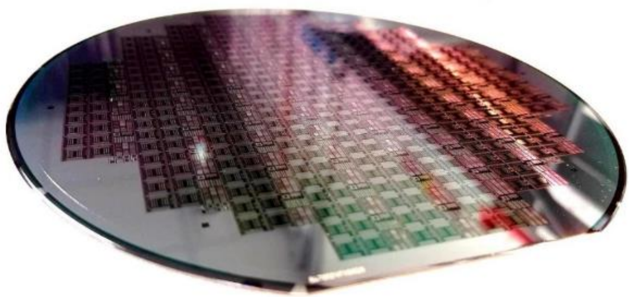
Parallel R&D on SPAD, 3D Vertical Integration and CMOS readout circuits

Development of the PDC Technology:

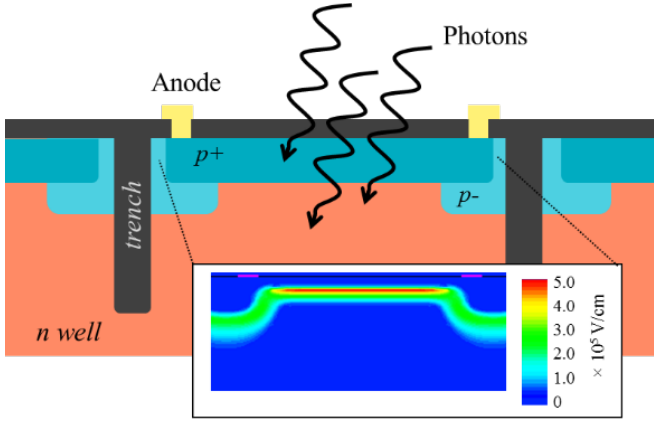
The SPAD Array

SPAD R&D and Characterization

- 150 mm wafer (custom process using Teledyne-DALSA CCD production line)
- 1x1 to 5x5 mm^2 SPAD array
- 50-100 um diameter **front-side illuminated** shallow P+N type SPAD (~0.4 um depth)
- 4 um width / 22 um depth optical/electrical isolation trench (highly doped polysilicon filling)
- 2D process for parallel SPAD development
- New SPAD received March 2020: Covid-19 is delaying testing



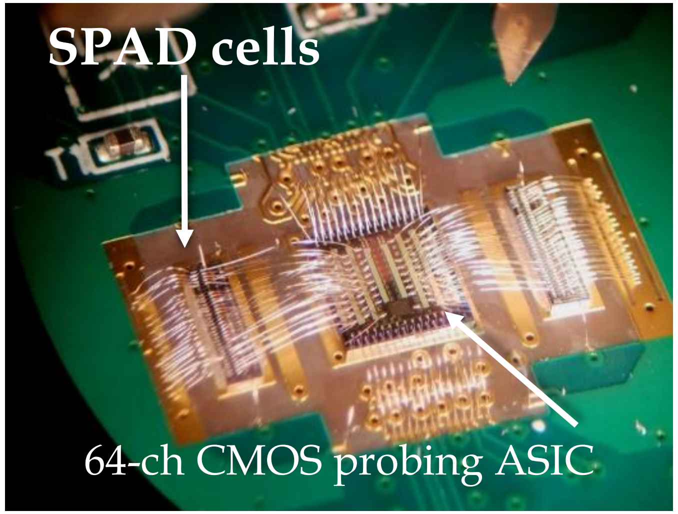
TELEDYNE DALSA
Everywhereyoulook™



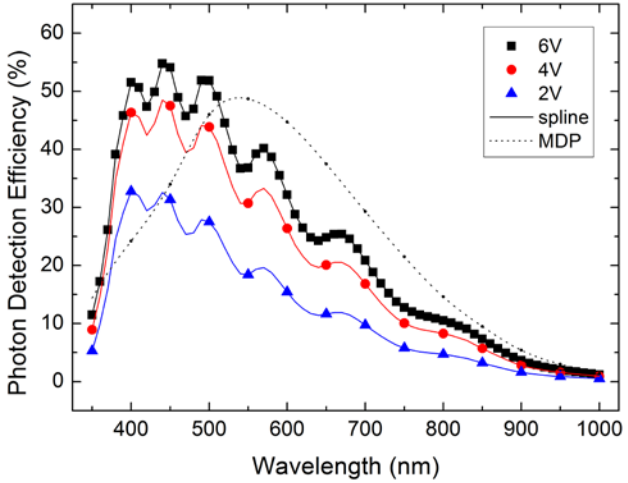
Front-side illuminated shallow $p^{+}n$ type SPAD

SPAD R&D and Characterization

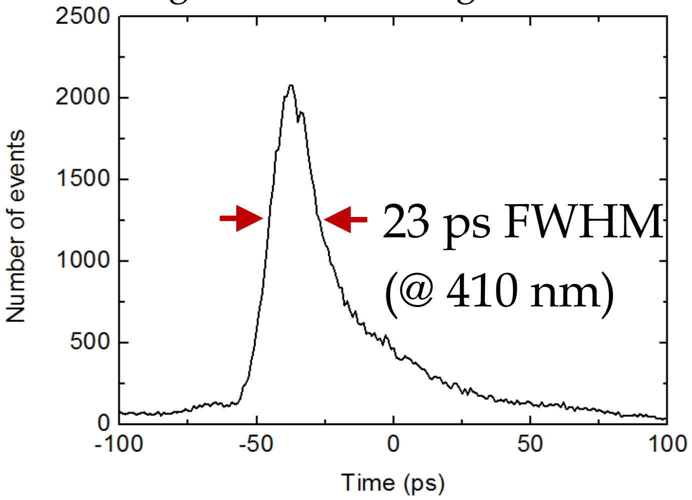
2D SPAD development platform



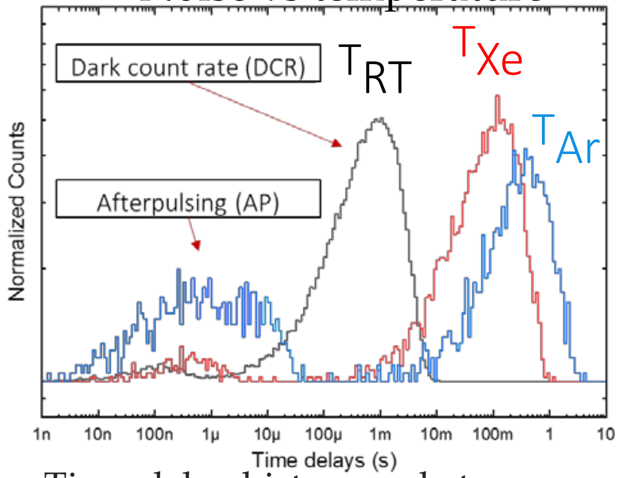
Photon Detection Efficiency



Single Photon Timing Resolution



Noise vs temperature



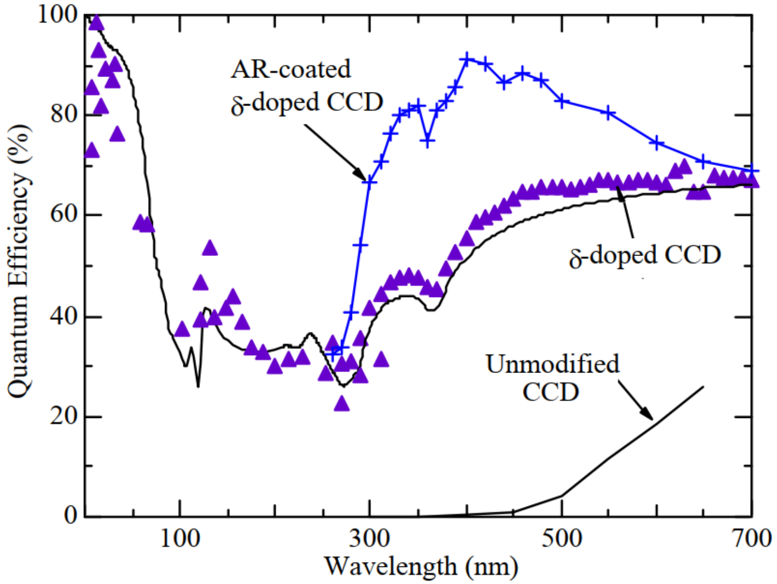
Time-delay histogram between two consecutive counts

SPAD array DCR:
~1000 Hz/mm²
(assuming 38 μm SPAD with 60% FF)

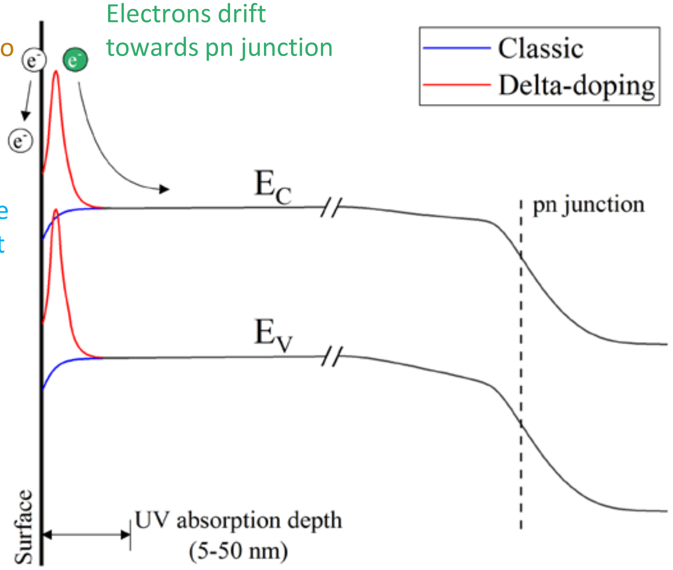
VUV Sensitivity Enhancement for Liquid Argon and Liquid Xenon

- Penetration depth @ 175 nm = 5.8 nm
- Delta-doping: surface energy band engineering to cause electron drift toward the high field avalanche region
- Delta doping: increase internal quantum efficiency (~100% IQE in CCDs ▲)
- Delta doping + anti-reflective coating (+) : major PDE improvement
- UdeS-TRIUMF-Lawrence Berkeley Lab collaboration « Towards high efficiency single VUV photon

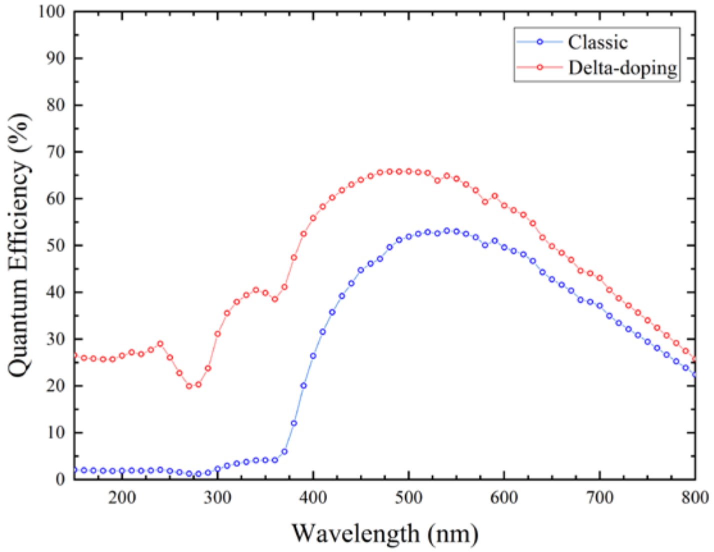
Arthur B. McDonald
Canadian Astroparticle Physics Research Institute



Delta-doped back-illuminated CMOS imaging arrays: progress and prospects.
M.E. Hoenk (In Infrared Systems and Photoelectronic Technology IV 2009)



Simulation of energy bands with delta-doping



Simulation of SPAD internal efficiency with delta-doping

Development of the PDC Technology:

The 3D Vertical Integration Process

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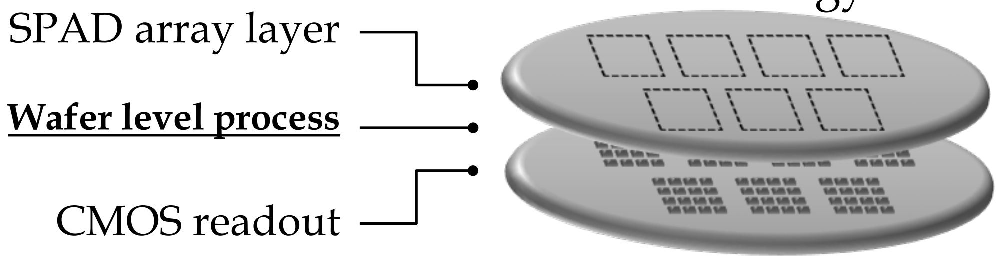
Photon-to-Digital Converter : Al-Ge 3D Integration Process and Resistivity Measurement

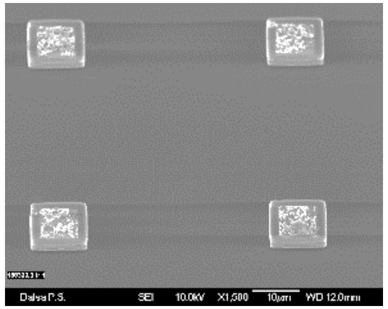
3D Process overview :

- ✓ SPAD array and trenches
  (skipped for 3D 1st run)
- ✓ Direct bonding on handle wafer
- ✓ Back side thinning + Back side Ge interconnect
- ✓ AlGe wafer-to-wafer bonding with fake CMOS
- ➢ Front side relief (handle removing)
- ➢ CMOS pads opening, dicing

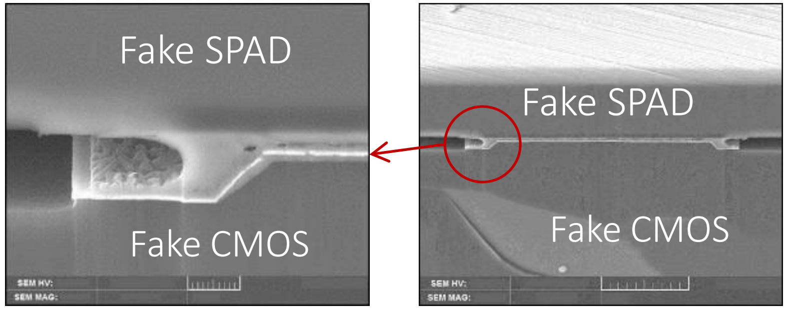
- Measurement of AlGe interconnect <1 Ω
- Towards completion of 3D validation samples

Wafer scale PDC technology

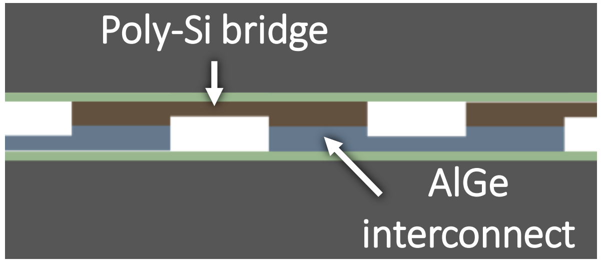


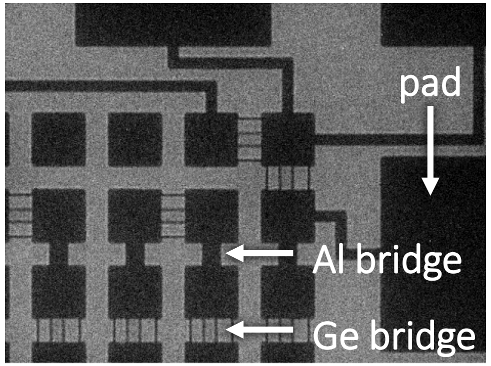


Ge interconnects :
10x10 um size
50 um pitch



AlGe "solder" (eutectic alloy) :
CMOS --> Al ; SPAD --> Ge
Established technology in MEMS foundry





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Development of the PDC Technology:

Microelectronic Readout Integrated Circuit for Precise Single Photon Timing Resolution (Goal: sub 10 ps)

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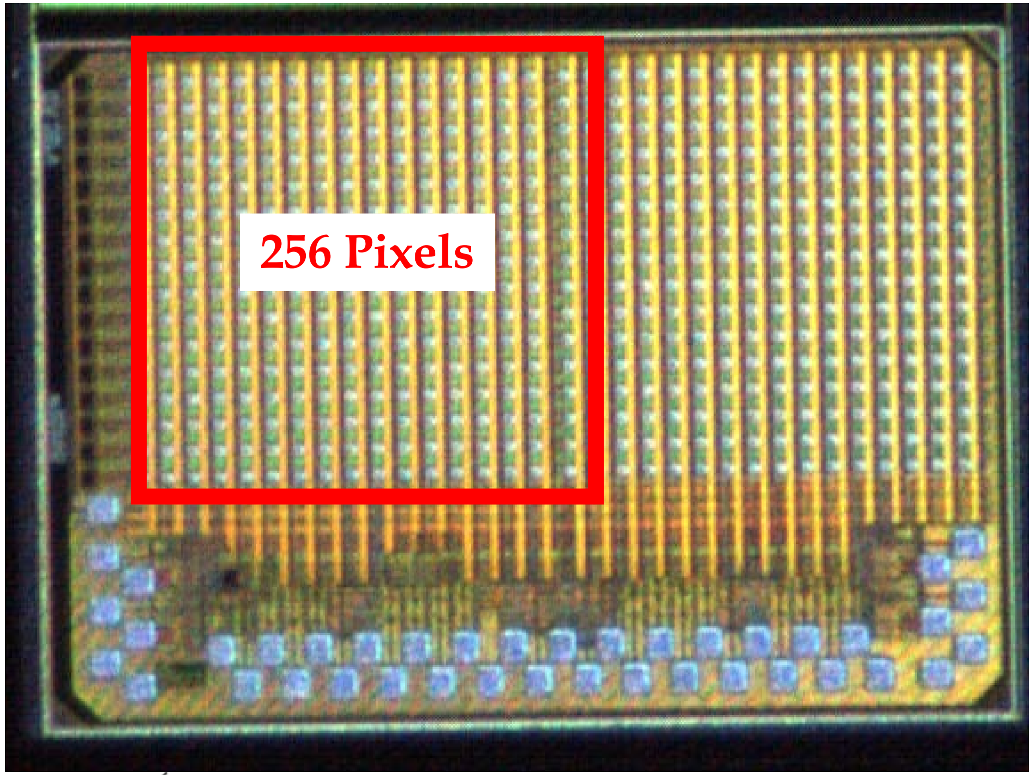
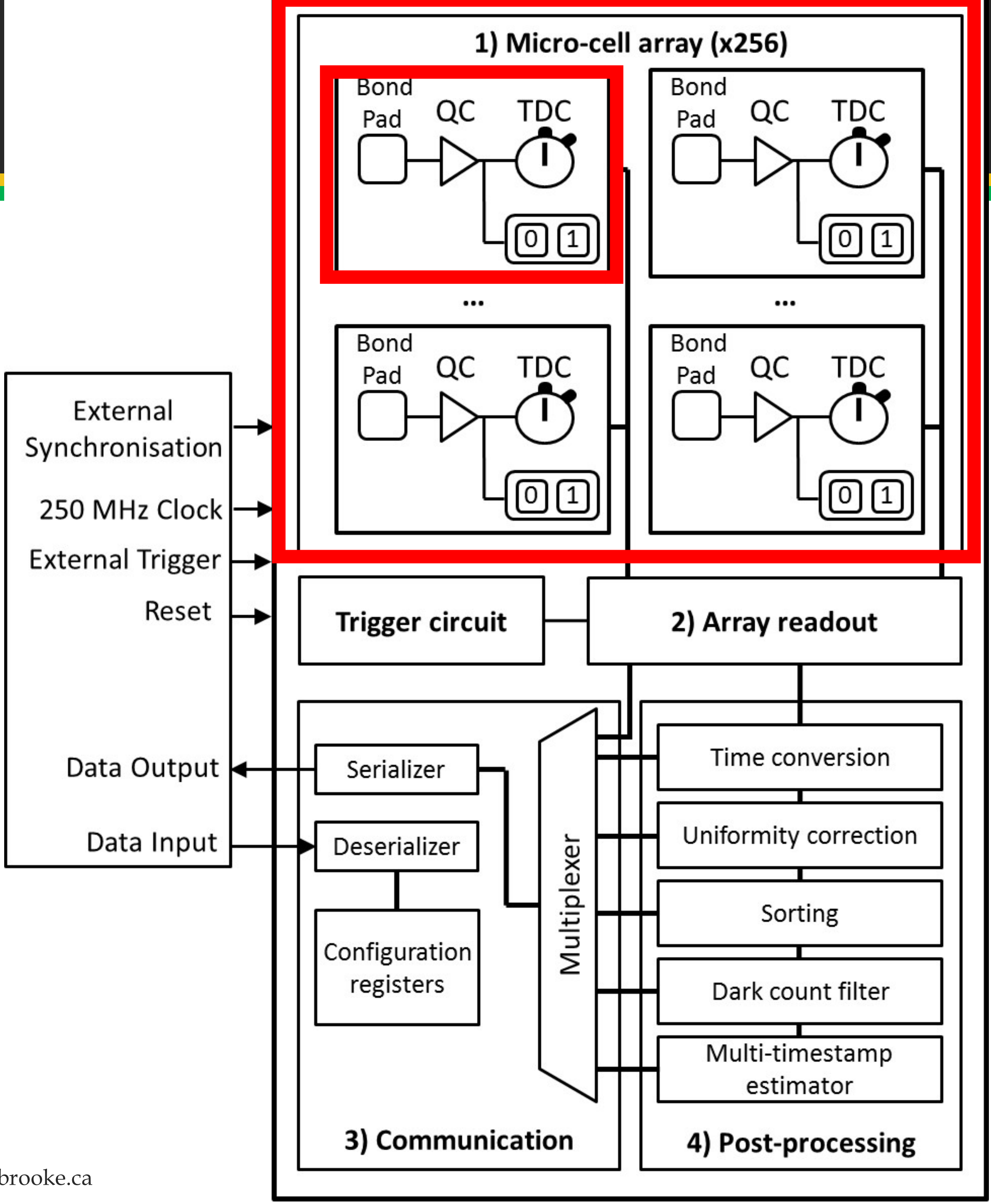
ASIC Overview (originally for PET)

- TSMC 65 nm CMOS (GP)
- 16 × 16 pixels in 1.1 × 1.1 mm² (red box)
- New revision May 2020 in fab
  - 1 TDC shared with 4 SPAD
  - LP instead of GP process flavor





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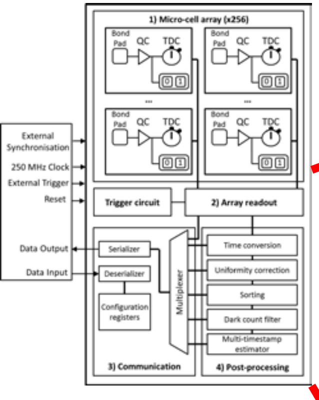
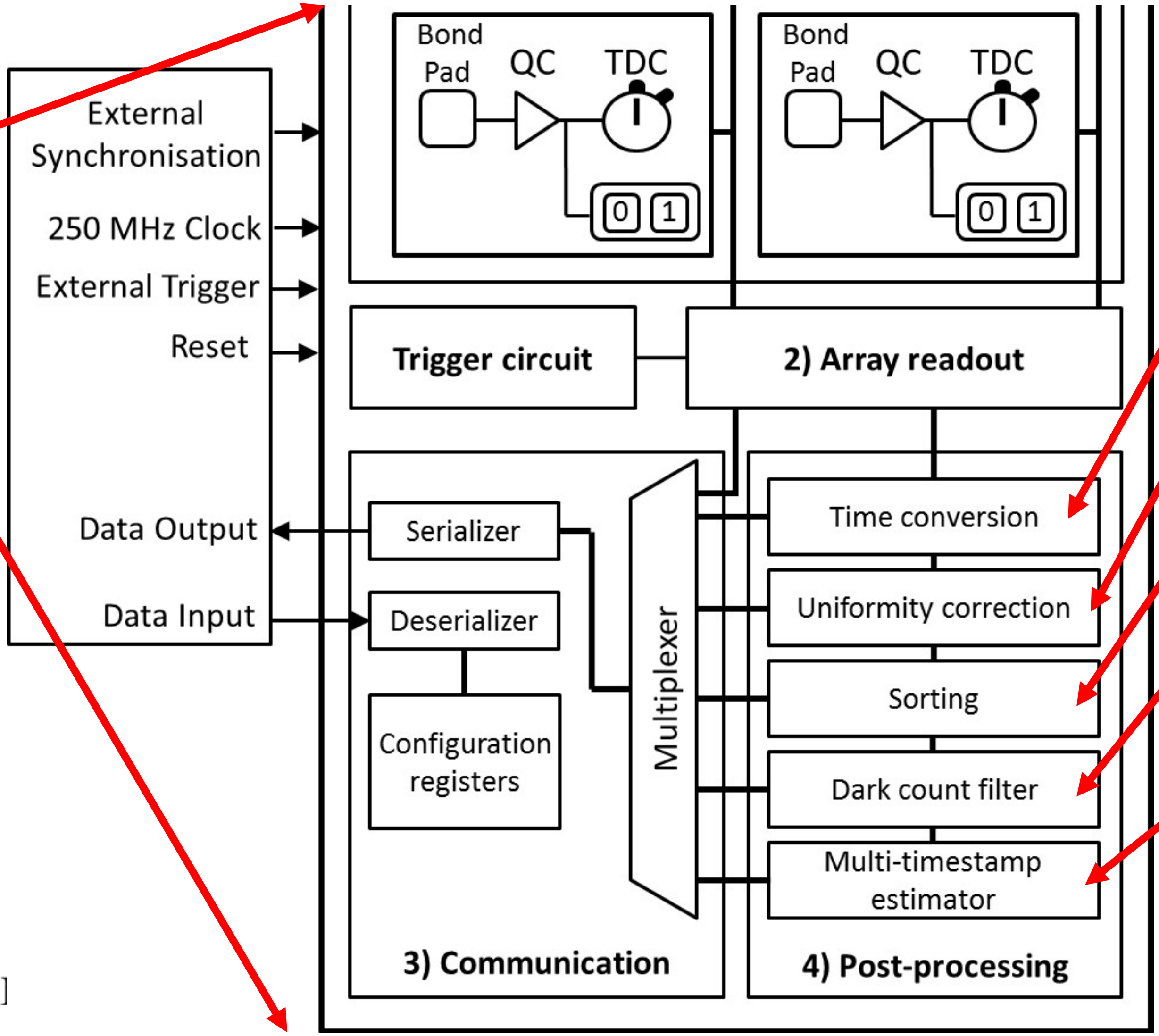
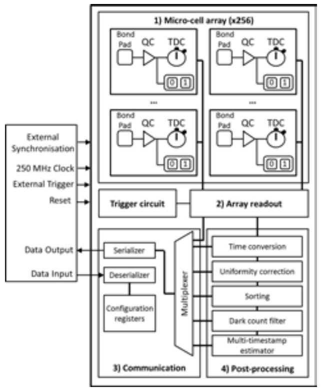
Embedded Digital Signal Processing: Improved Coincidence Timing Resolution and Lower Output Data Bandwidth

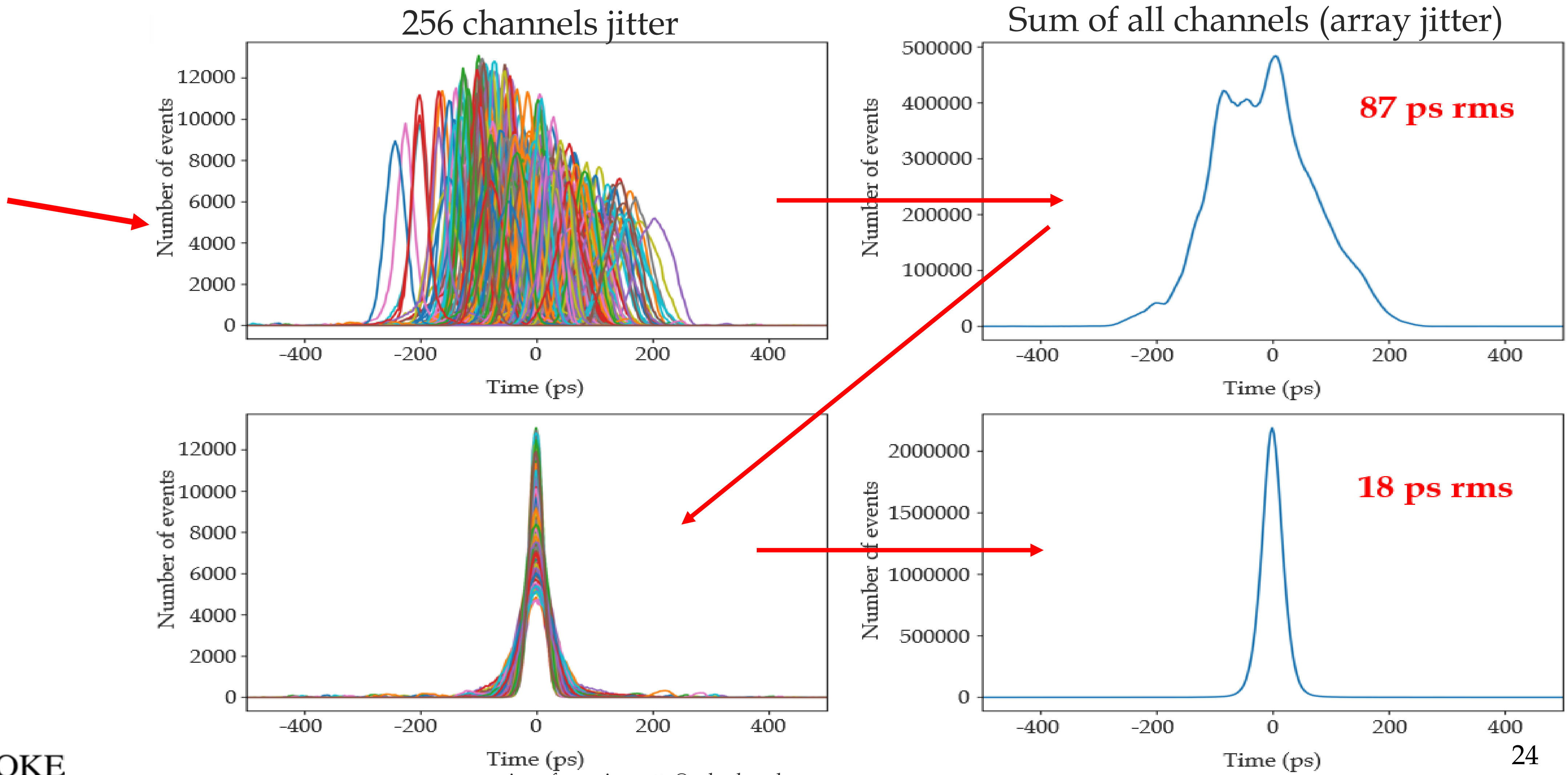




- Time conversion
- Uniformity correction
- Sorting – first 32 photons
- Dark Count Filter
- Multi-timestamp estimator (BLUE)

Integrated Circuit Embedded Digital Signal Processing Example: Uniformity Correction





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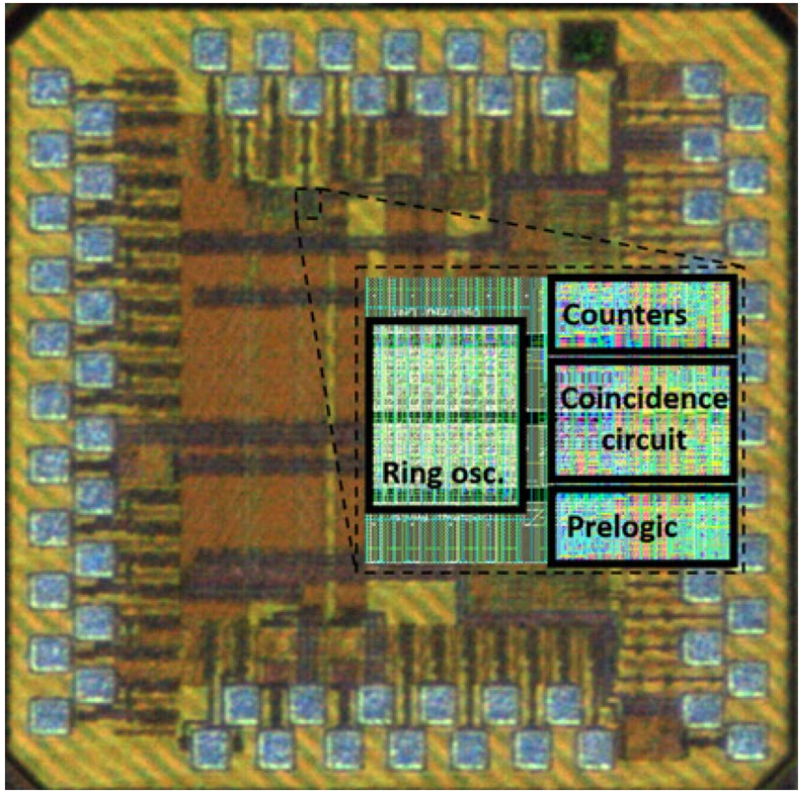
Ring Oscillator based Vernier Time-to-Digital Converter

22 µW, 5.1 ps LSB, 5.5 ps RMS jitter Vernier time-to-digital converter in CMOS 65 nm for single photon avalanche diode array, Electronics Letters, April 2020, Vol. 56 No. 9 pp. 424–426,
F. Nolet, N. Roy, S. Carrier, J. Bouchard, R. Fontaine, S.A. Charlebois and J.-F. Pratte



Parameter	This work	Ref. [3]	Ref. [7]	Ref. [5]
technology, nm	65	65	65	350
area, mm^2	0.00151	0.0013	0.068	0.3
LSB, ps	5.1	15	2.2	10
jitter, ps RMS	5.5	6.9	0.6	17.2
event rate, ME/s	1–8	3	2.2	0.3
power, µW	22–41	160	2 300	15,000
pJ/event	22–5.1	32	46	5000
FoM	0.17–0.04	0.29	1.9	25,800
FoM = [Power (µW) × Jitter (ps RMS) × Area (mm^2)] / [Event Rate (Mevents/s)]				

$$\text{FOM} = \frac{\text{Power }(\mu\text{W}) \times \sigma_{\text{global}}\ (\text{ps}) \times \text{Area }(\text{mm}^2)}{\text{Events Rate (Mevents/s)}} \left[\text{pJ/event} \cdot \text{ps}_{\text{rms}} \cdot \text{mm}^2\right]. \quad (21)$$

Time-to-Digital Converters R&D

- New TDC architecture/concept developed
- Patent written. Final proof read. Should be submitted for evaluation before end of June 2020.

Development of the PDC Technology:

Microelectronic Readout Integrated Circuit for Low Power PDC and Large Area Detectors

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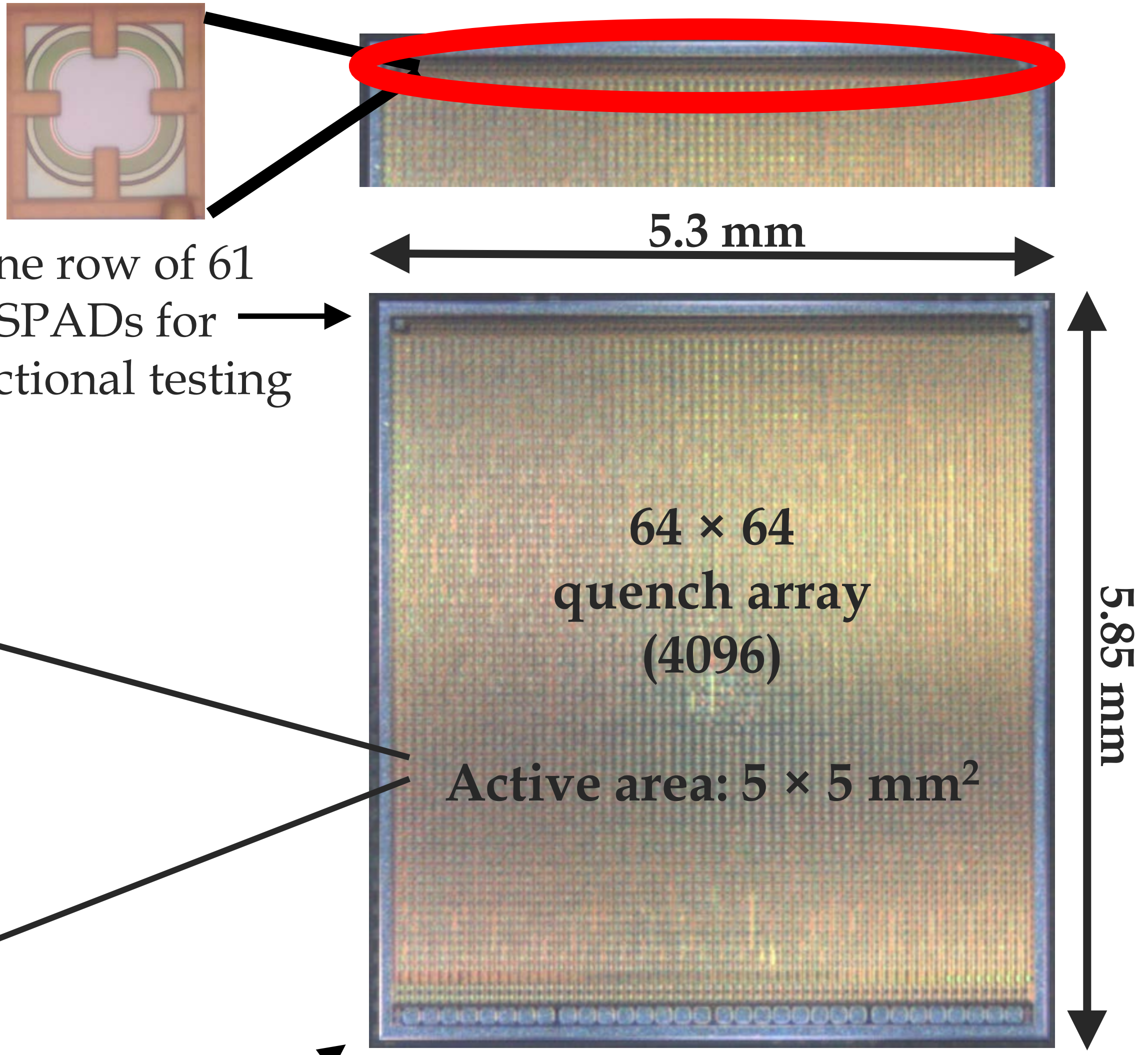
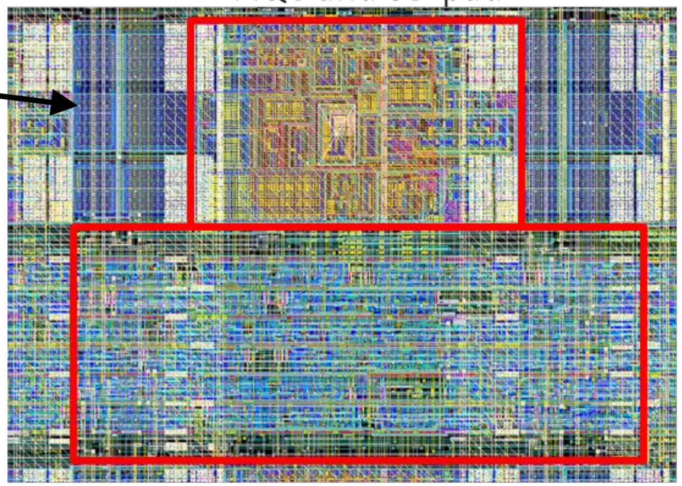
CMOS Readout for PDC – Overview

- TSMC 180 nm BCD process
- 5 x 5 mm^2 active area
- 64 x 64 pixels (4096)
- 78 µm pixel pitch
- 3-side buttable (for tiles)
- Digital-on-Top design flow





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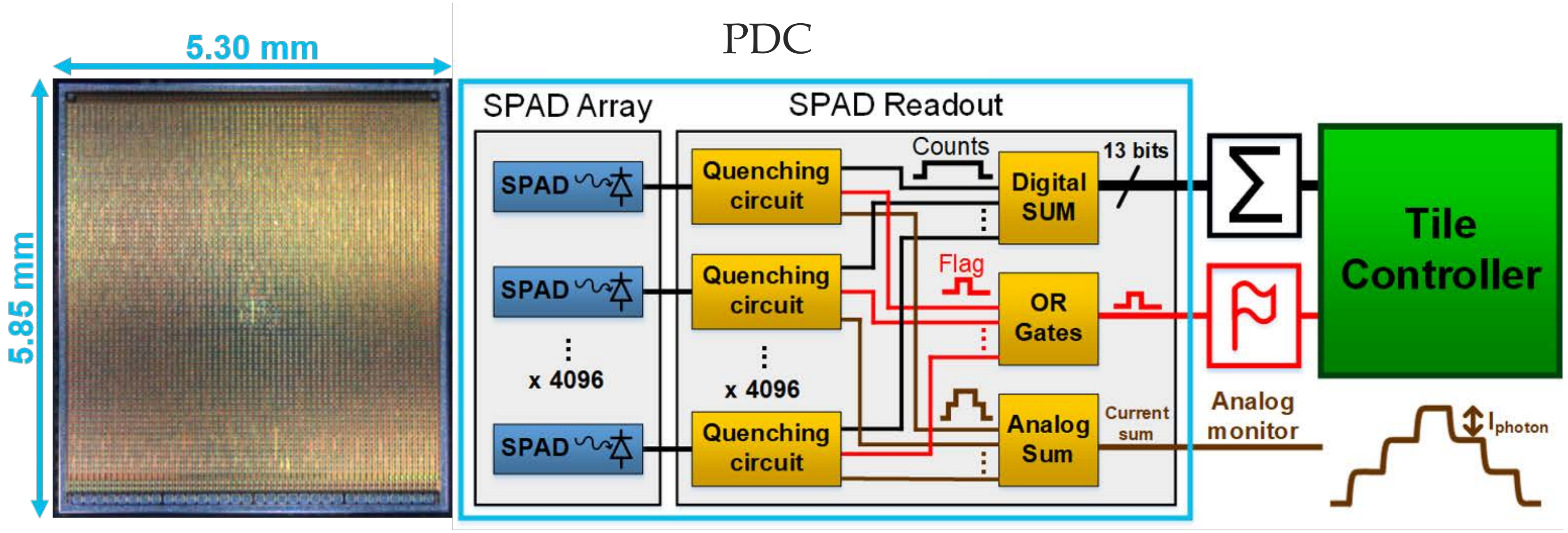
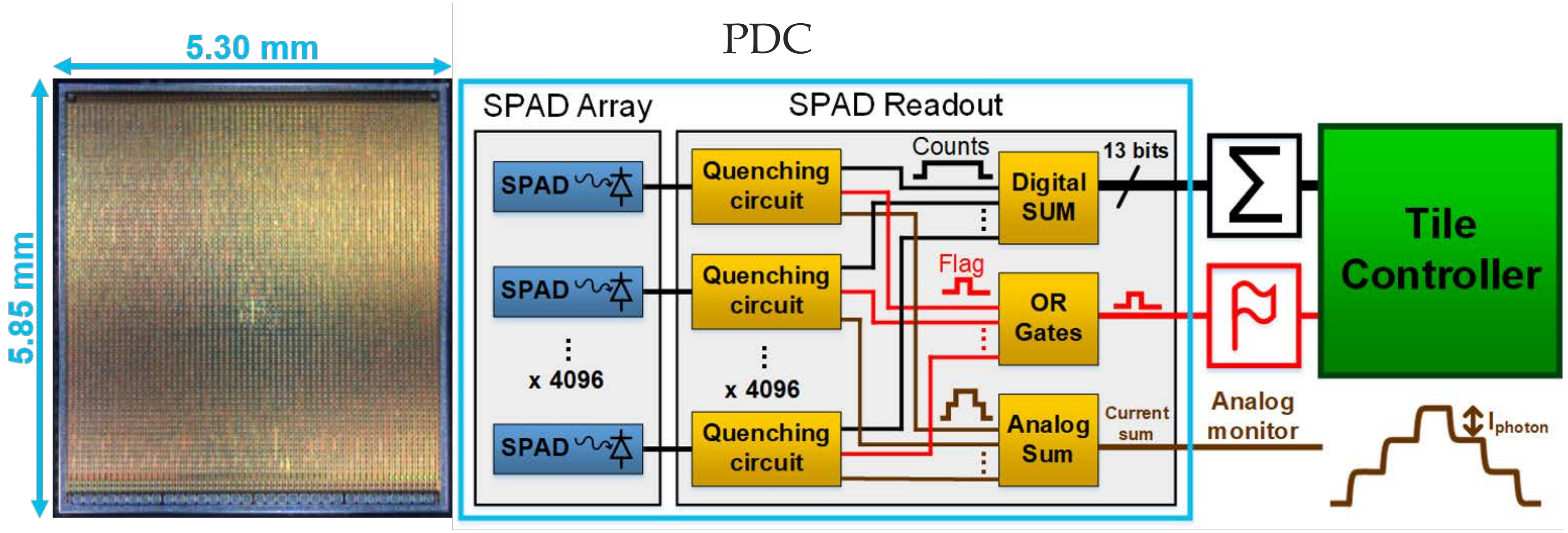
CMOS Readout for PDC – Low Power Architecture



CMOS Readout for PDC – Low Power Architecture

- nEXO operation mode: **INTEGRATION**
  - Event driven: each PDC signals the tile controller when a SPAD triggers
  - **Asynchronous (no event no clock – low power)**
  - Integration time from 10 ns to 10 µs
  - Transmission of total counts (over integration time) when requested by the tile controller
  - Analog monitor for demonstration



CMOS Readout for PDC – Low Power Architecture

- nEXO operation mode: **INTEGRATION**
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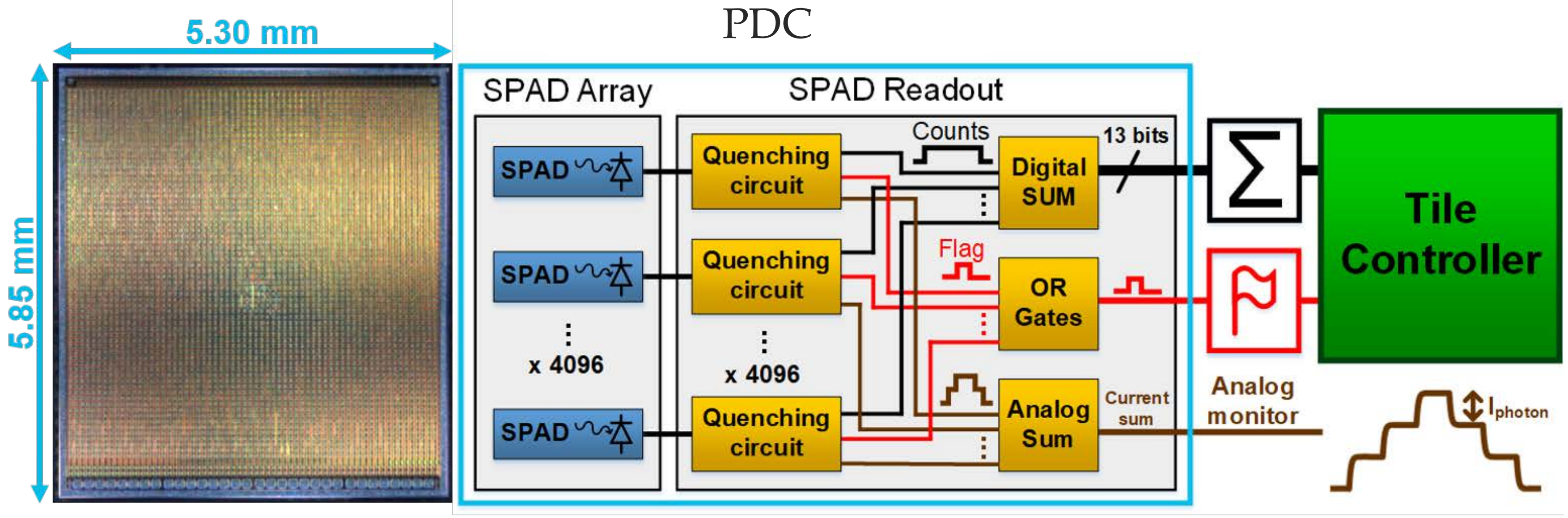
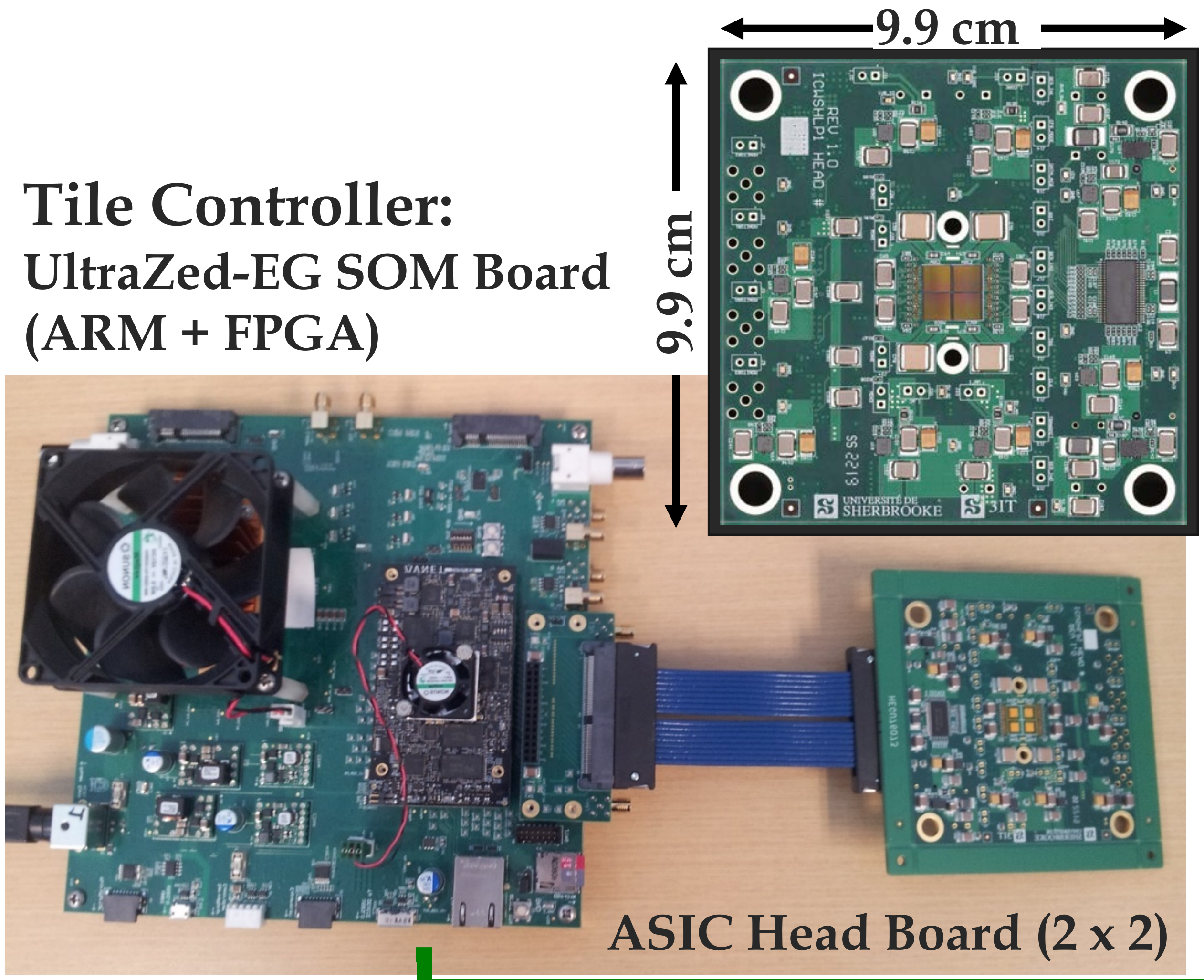
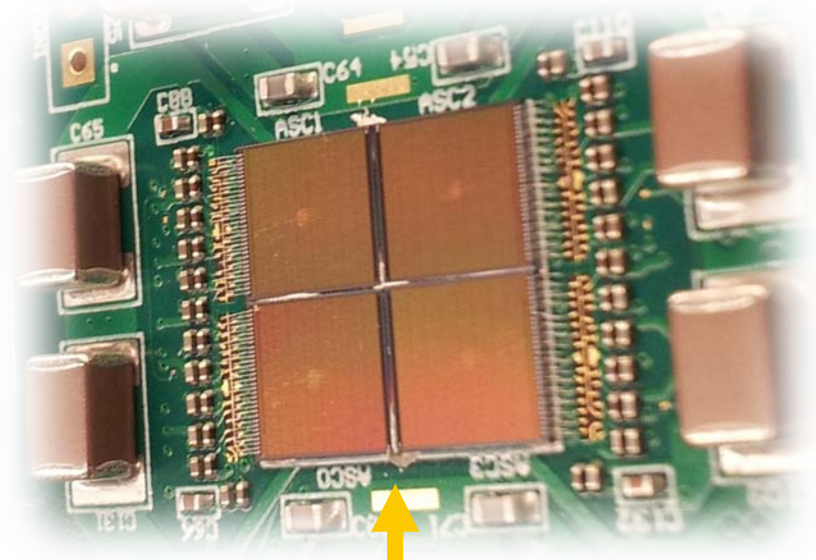
  - **Asynchronous (no event no clock – low power)**
  - Integration time from 10 ns to 10 µs
  - Transmission of total counts (over integration time) when requested by the tile controller
  - Analog monitor for demonstration
- LAr operation mode: **CONTINUOUS SAMPLING**
  - Synchronous operation by a clock
  - Flags the controller to signal counts
  - Low flag jitter (<250 ps) to allow time-of-flight
  - 128 FIFO depth for transmission on request
  - FIFO sampling bins: short (10 ns) and long frames (1 µs) to allow PSD (Pulse Shape Discrimination)

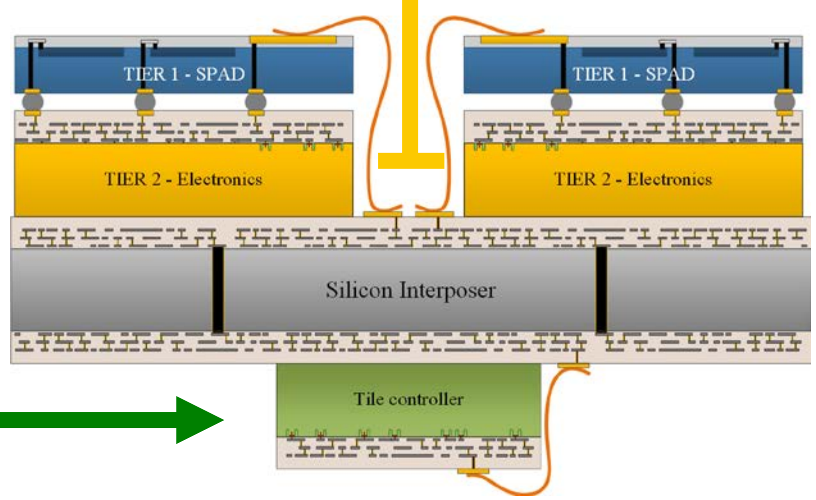


Measurement Testbench – Toward Tile Integration

Tile Controller:
UltraZed-EG SOM Board (ARM + FPGA)

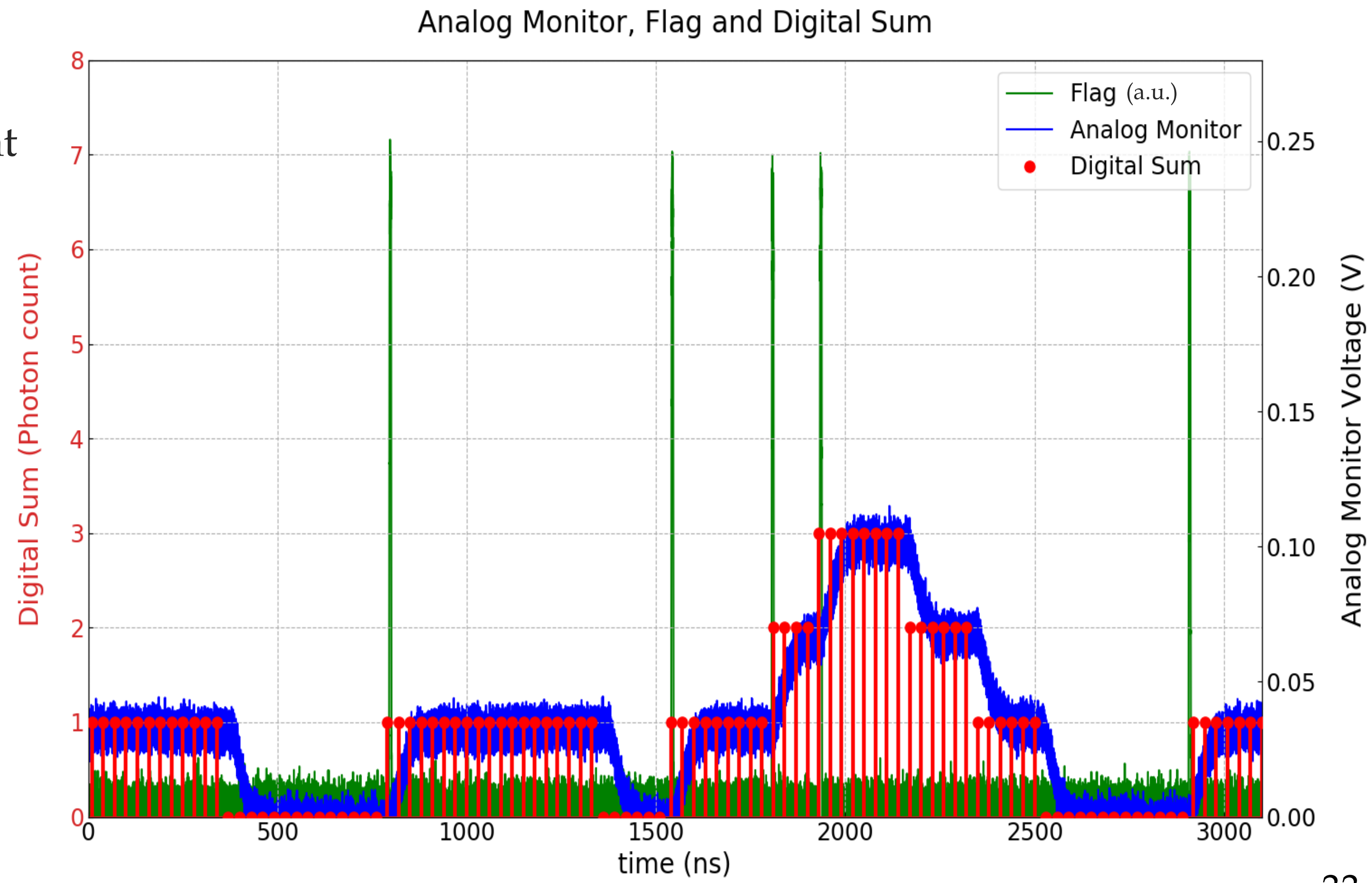






Photon-to-Digital Converter Measurements: Flag, Digital Sum and Analog Monitor Corroborated

- ADC like **measurement**
  - Number of pixels triggered at the moment of the acquisition
- Flag signals every detected event
- Analog monitor confirms the digital output
- 25.2 W / 4.5 m^2 for nEXO operation mode



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Conclusion

- No fundamental limitation to build Front side illumination Photon-to-Digital Converter, but it is a great engineering challenge.
- First PDC expected in 2021.
- SPAD array, 3D integration and readout electronics developed and optimized in parallel.
  - Microelectronics readout for particle physics: wafer level production winter 2021.
  - SPAD R&D within Teledyne-DALSA.
    - New masks set in fabrication (optimized SPAD).
    - New SPAD arrays last March 2020: Covid-19 delay.
- PDC architecture flexible and versatile: they can be used/tailored for your application.
- (We are recruiting! Ph.D. and Postdoc.)
- Back side illumination SPAD array under design for VUV to NIR.

Selected Publications from our Team

- **Roadmap toward 10 ps time-of-flight PET challenge.** (2020). Lecoq, P.; Morel, C.; Pratte, J-F. et al. *Physics in Medicine and Biology*. Institute of Physics and engineering in Medicine.
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- **Embedded time of arrival estimation for digital photomultipliers with in-pixel TDCs.** (2020). Lemaire, W.; Nolet, F.; Dubois, F.; Corbeil Therrien, A.; Pratte, J-F.; Fontaine, R. *Nuclear Inst. And Methods in Physics Research, A*. 163538
- **Dark Count Resilient Time Estimators for Time-of-Flight PET.** (2020). Lemaire, W.; Corbeil Therrien, A.; Pratte, J-F.; Fontaine, R. *IEEE Transactions on Radiation and Plasma Medical Sciences*. 4(1): 24-29
- **A 256 Pixelated SPAD Readout ASIC with in-Pixel TDC and Embedded Digital Signal Processing for Uniformity and Skew Correction.** (2019). Nolet, F.; Lemaire, W.; Dubois, F.; Carrier, S. G.; Samson, A.; Charlebois, S. A.; Fontaine, R.; Pratte, J-F. *Nuclear Inst. And Methods in Physics Research, A*. 162891
- **Record breaking timing resolution with a room temperature single photon detector - Two photons timing resolution of record-breaking low jitter SPADs measured by Time Tagger Ultra HiRes.** (2019), Application Note Si-0004. M. Kolarczik, H. Fedder, M. Wick, F. Nolet, S. Parent, N. Roy, and J.-F. Pratte
- **Single Photon Avalanche Diodes and Vertical Integration Process for a 3D Digital SiPM using Industrial Semiconductor Technologies.** (2^{nd} position NSS student competition – oral prensentation). (2018). Parent, S.; Côté, M.; Vachon, F.; Groulx, R.; Martel, S.; Dautet, H.; Charlebois, S. A.; Pratte, J-F. *2018 IEEE NSS-MIC Conference Record*. 2018 IEEE NSS-MIC, Sydney, Australia.
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- **Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution**. (2018). Nolet, F.; Parent, S.; Roy, N.; Mercier, M.-O.; Charlebois, S. A.; Fontaine, R. ; Pratte, J-F. *MDPI - Instrument - Special Issue Advances in Particle Detectors and Electronics for Fast Timing*. 2(4)

Selected Publications from our Team

- **Digital SiPM channel integrated in CMOS 65 nm with 17.5 ps FWHM single photon timing resolution**. (2017). Nolet, F. and Dubois, F. and Roy, N. and Parent, S. and Lemaire, W. and Massie-Godon, A. and Charlebois, S. A and Fontaine, R. and Pratte, J.-F. *Nuclear Instruments and Methods in Physics Research Section A*, 912: 29-32.
- **TDC Array Trade-Offs in Current and Upcoming Digital SiPM Detectors for Time-of-Flight PET**. (2017). Tetrault, M.-A.; Lemaire, W.; Corbeil-Therrien, A.; Fontaine, R.; Pratte, J.-F. *IEEE Transactions on Nuclear Science*. 64(3): 925-932.
- **Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3D Digital SiPM**. (2017). Roy, N. and Nolet, F. and Dubois, F. and Mercier, M-O. and Fontaine, R. and Pratte, J.-F. *IEEE Transactions on Radiation and Plasma Medical Sciences*. 10(6): 486-494.
- **A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS with Low Output Capacitance**. (2016). Nolet F, Rhéaume V-P, Parent S, Charlebois SA, Fontaine R, Pratte J-F. *IEEE Transactions on Nuclear Science*. 63(4): 2293-2299.
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- **Dark Count Impact for First Photon Discriminators for SPAD Digital Arrays in PET**. (2014). Tétrault M.-A., C. Therrien A., Desaulniers Lamy A., Boisvert A., Fontaine R., Pratte J.-F. *IEEE Transactions on Nuclear Science*. 62(3): 719-726.
- **Real-Time Discreet SPAD Array Readout Architecture for Time of Flight PET**. (2014). Tétrault M.-A., Desaulniers Lamy É., Boisvert A., Thibaudeau C., Dubois F., Fontaine R., Pratte J.-F. *IEEE Transactions Nuclear Science.* 62(3): 1077-1082.

A Team's Work

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CMC MICROSYSTEMS

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The End