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3D-Stacked SPAD in 40/45nm BSI Technology

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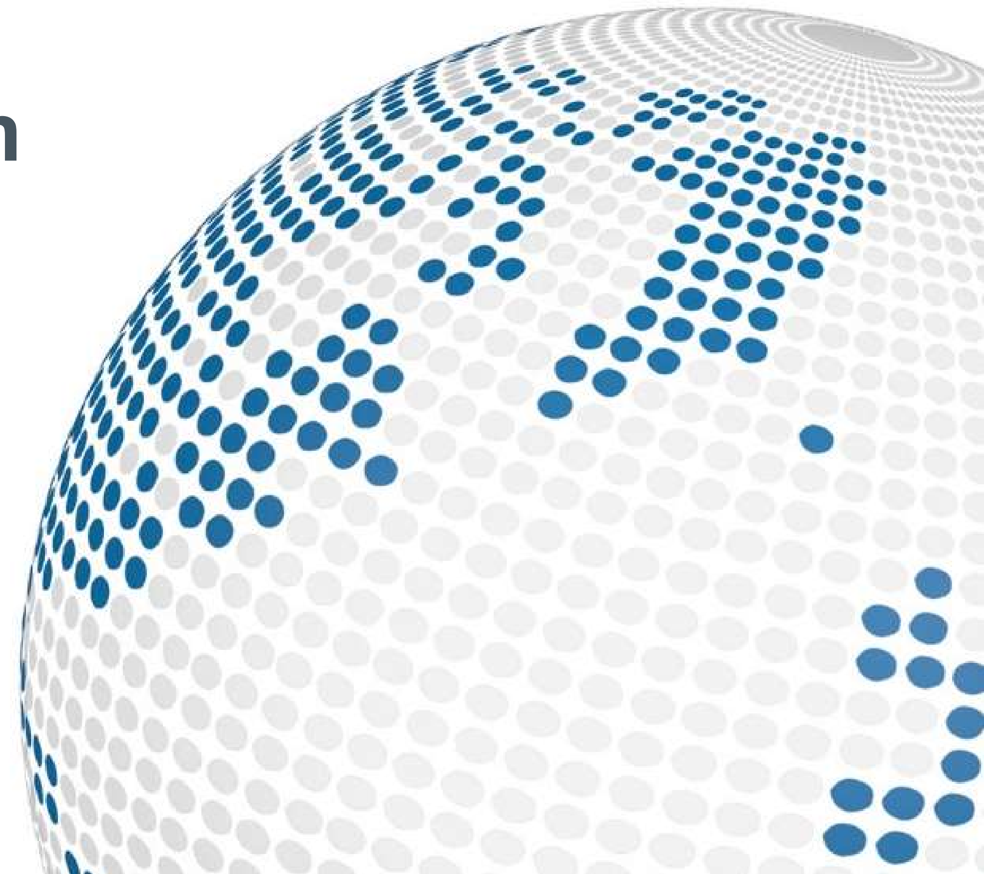

Georg Röhrer
June 8, 2020

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Outline of Presentation

Motivation for 3D-Stacking

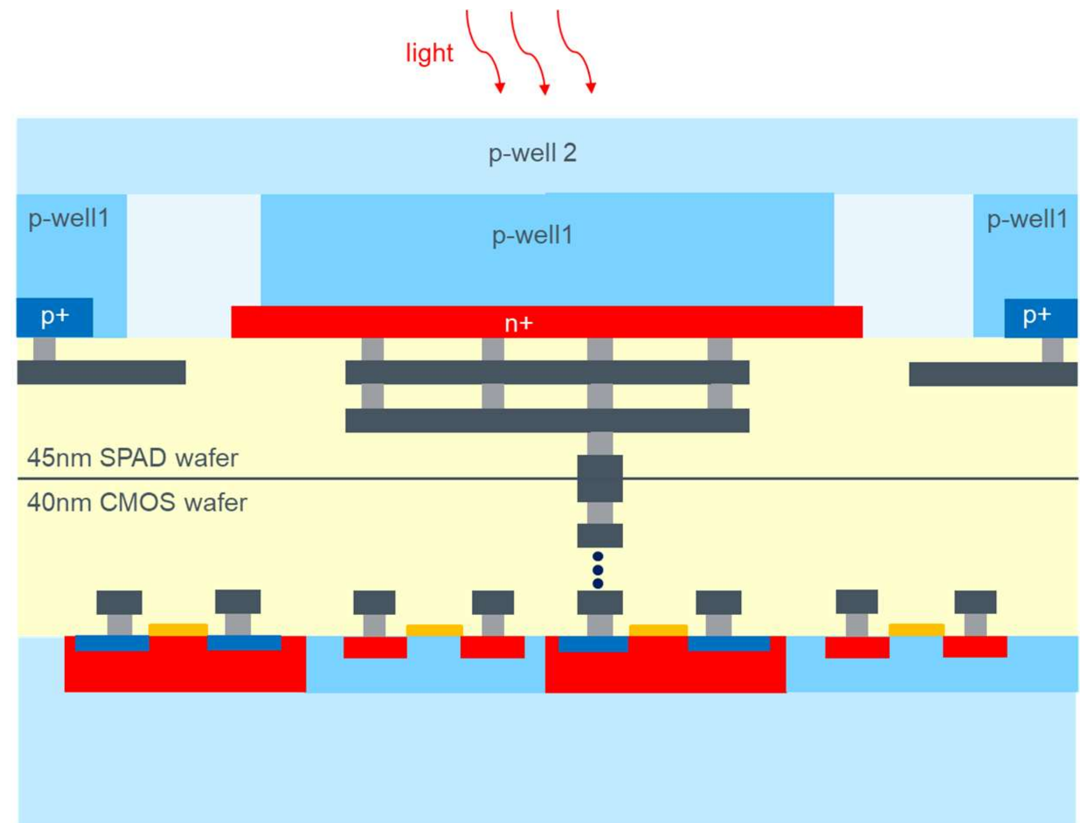
Test structure and SPAD description

Characterization Results

Benchmark

Motivation for 3D Stacking

- Back side illuminated (BSI)
- Fill factor limited by SPAD only.
- Process for SPAD wafer can be optimized for SPAD performance (e.g. depletion layer width).
- SPAD process can be re-used for different CMOS nodes – enabling optimized products in terms of performance and cost.



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Test Structure and SPAD Schematic

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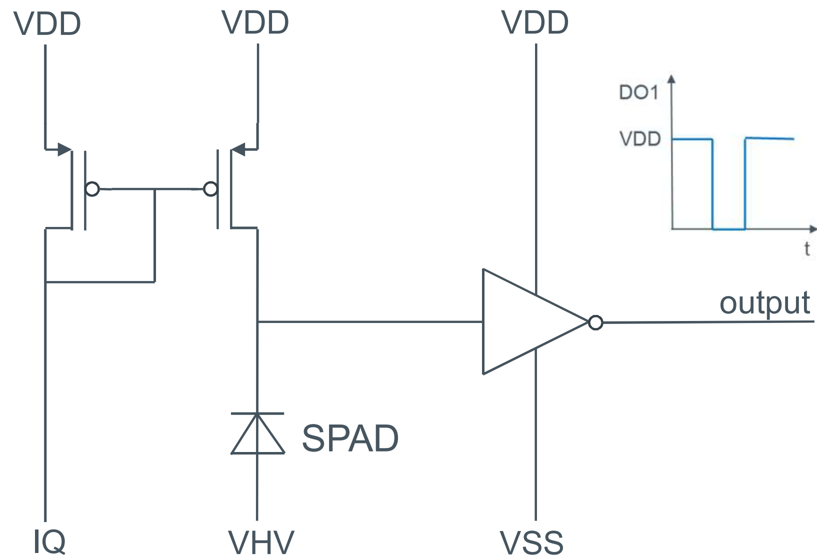
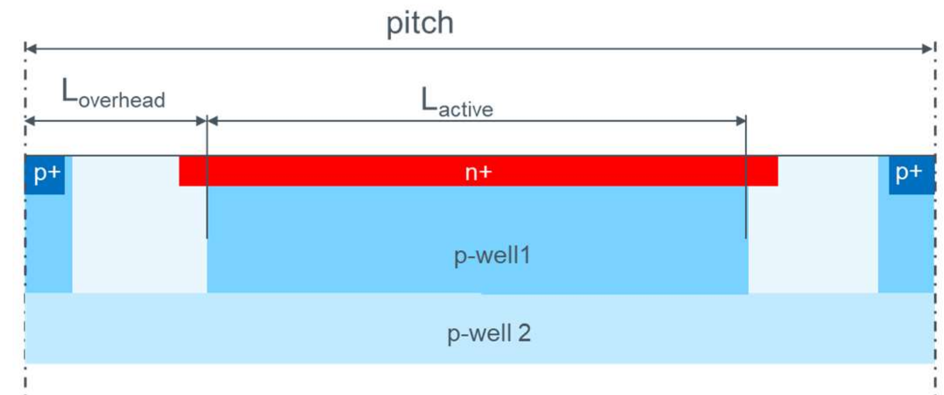


- SPAD is biased between VDD and VHV (negative).
- Passive quenching used.
- Current IQ used to set the dead time over a wide range (~10ns….~10µs).
- For crosstalk characterization, outputs for two neighboring SPADs are available.



Device	Fill Factor[%]	$L_{overhead}$ [um]
1	25	3.15
2	32	2.75
3	36	2.55
4	40	2.35
5	44	2.15
6	48	1.95
7	52	1.75

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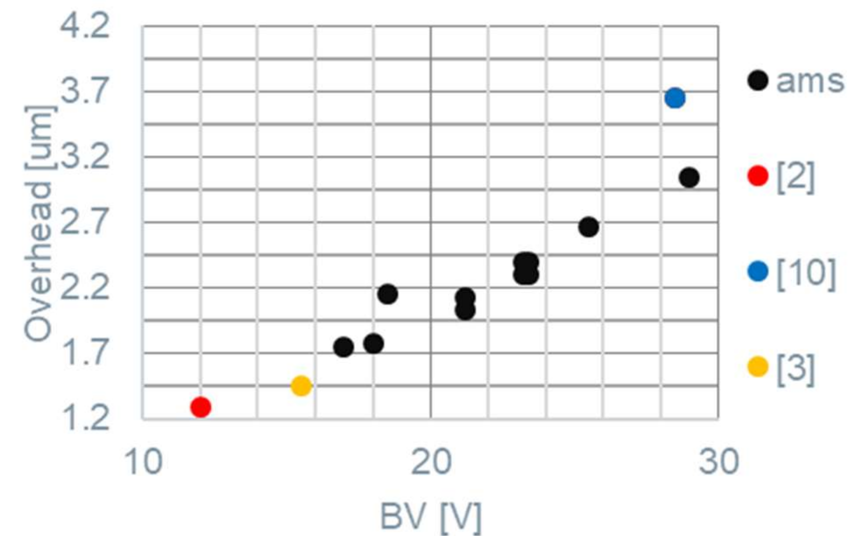
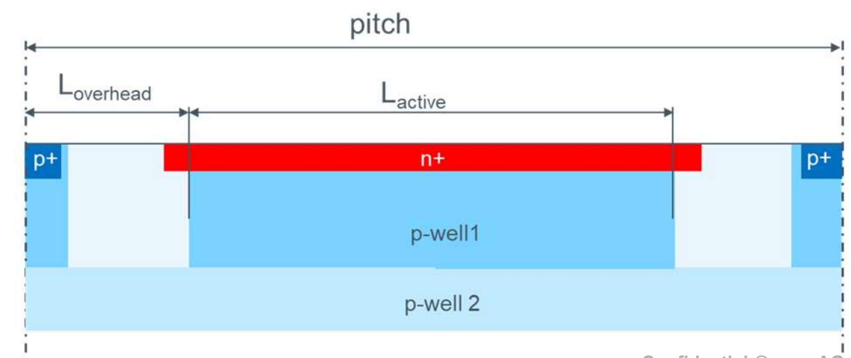
Breakdown Voltage

Main impact factors of breakdown voltage:

- Achievable fill factor limited by break down voltage. Required minimum “overhead” region scales approximately linearly with breakdown voltage.
- Depletion layer width (impact on PDE, junction capacitance)
- DCR (for low BV, tunneling dominates DCR).
- Energy per SPAD event scales with breakdown voltage.





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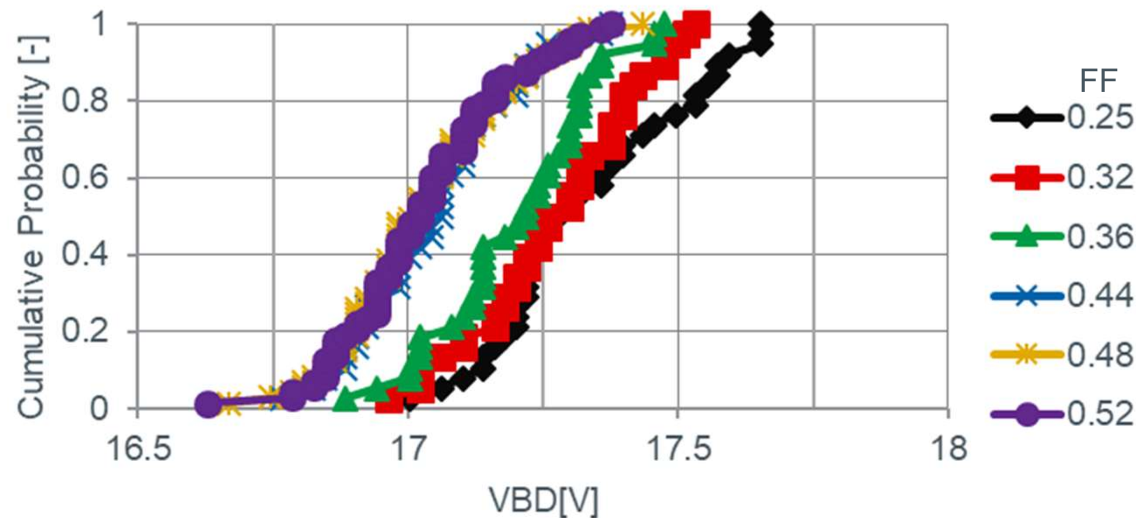
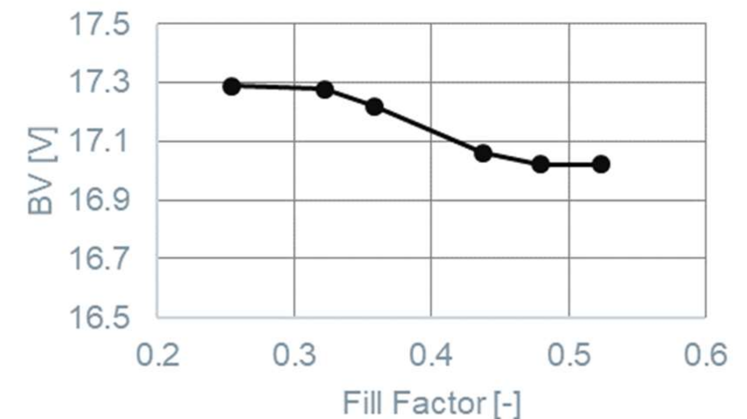
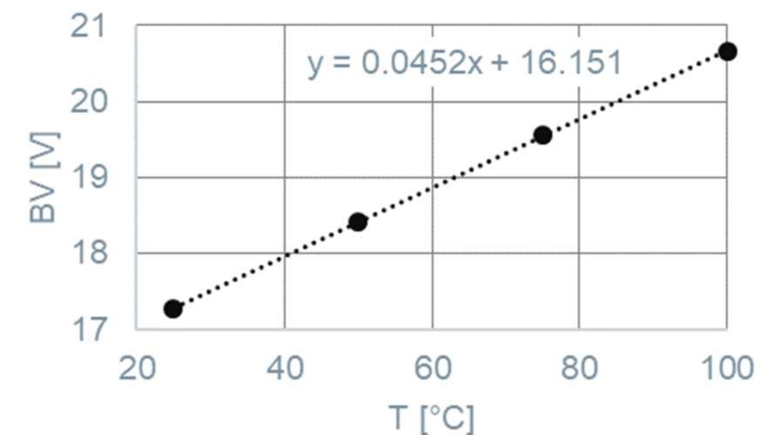
Breakdown Voltage (VBD)

Results for different fill factors







- VBD slightly decreases with fill factor (250mV).
- Standard deviation of within wafer distribution is ~150mV.
- VBD temperature coefficient is 45mV/°C, no impact of the fill factor.

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Dark Count Rate

25°C, Vexc=2.0V

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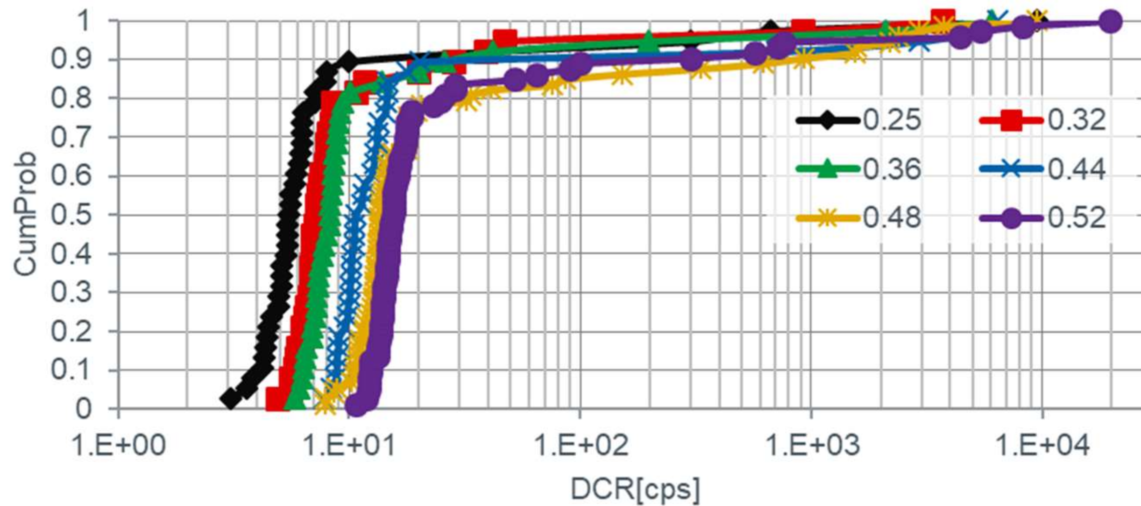
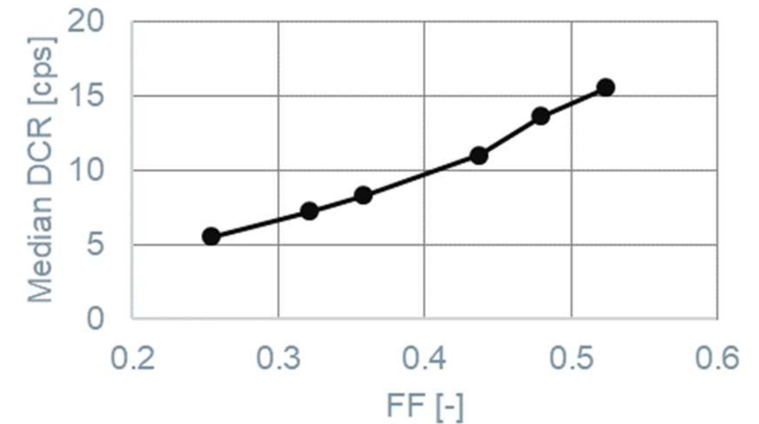
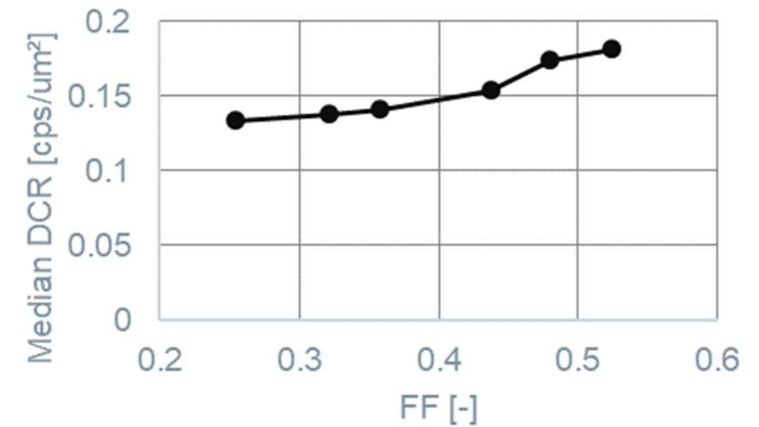


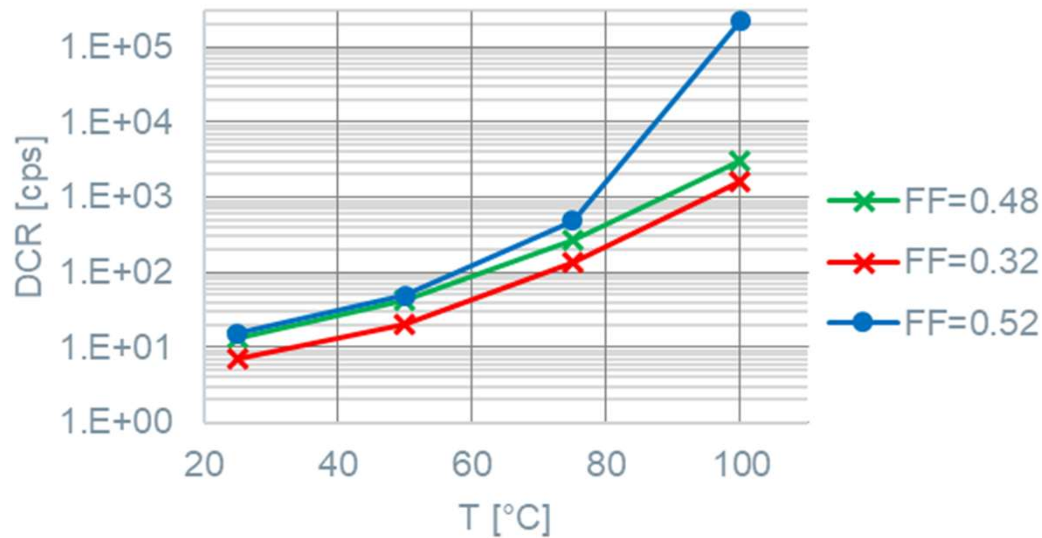


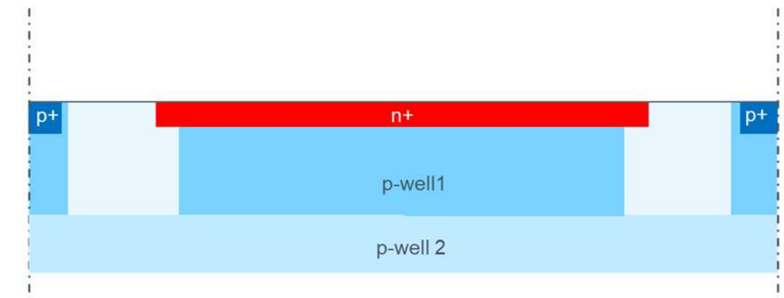
- DCR (median) is 6cps for a fill factor of 25% and 16cps for a drawn fill factor of 52%.
- Around 80% of SPADs show a DCR close to median value.
- When DCR is normalized to drawn active area, DCR (in cps/um²) still increases with fill factor. Indication that drawn active area ≠ real active area.

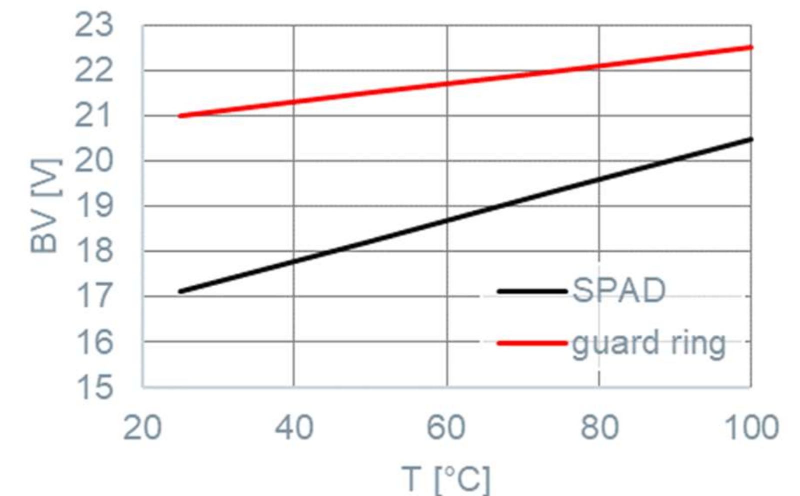


Dark Count Rate: Temperature Impact

Vexc=2.0V







- Activation energy (extracted from 75°C and 100°C measurements) is 1.08eV.
- For the device with the fill factor of 52%, the DCR becomes very high at 100°C, caused by the different temperature coefficient of the guard ring versus the avalanche junction.

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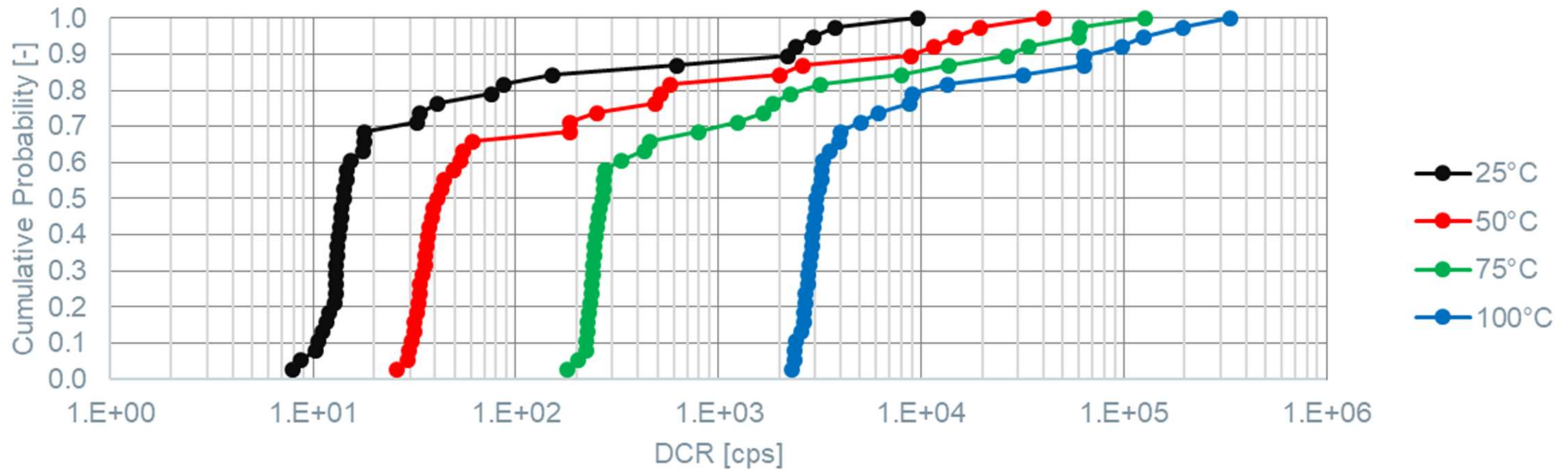
DCR Distribution for 25/50/75/100°C

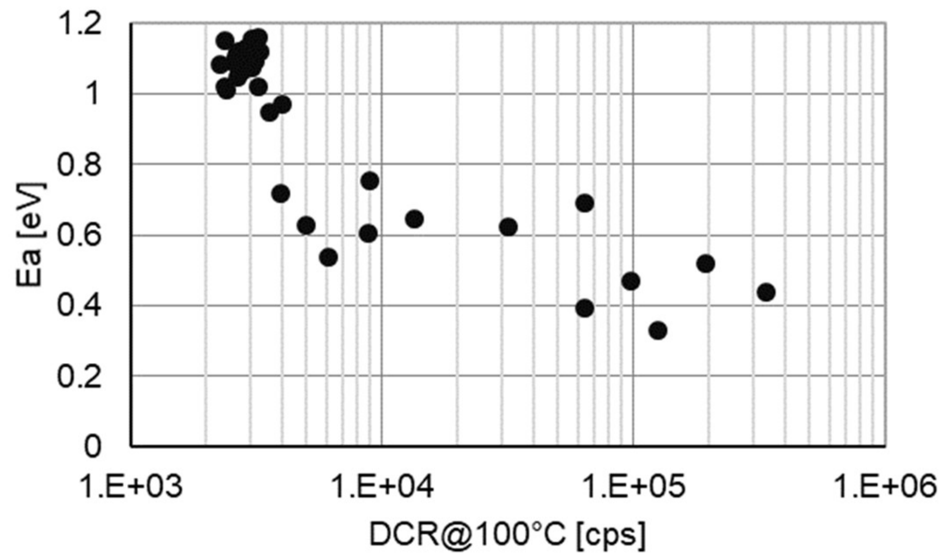
FF=0.48, Vexc=2.0V

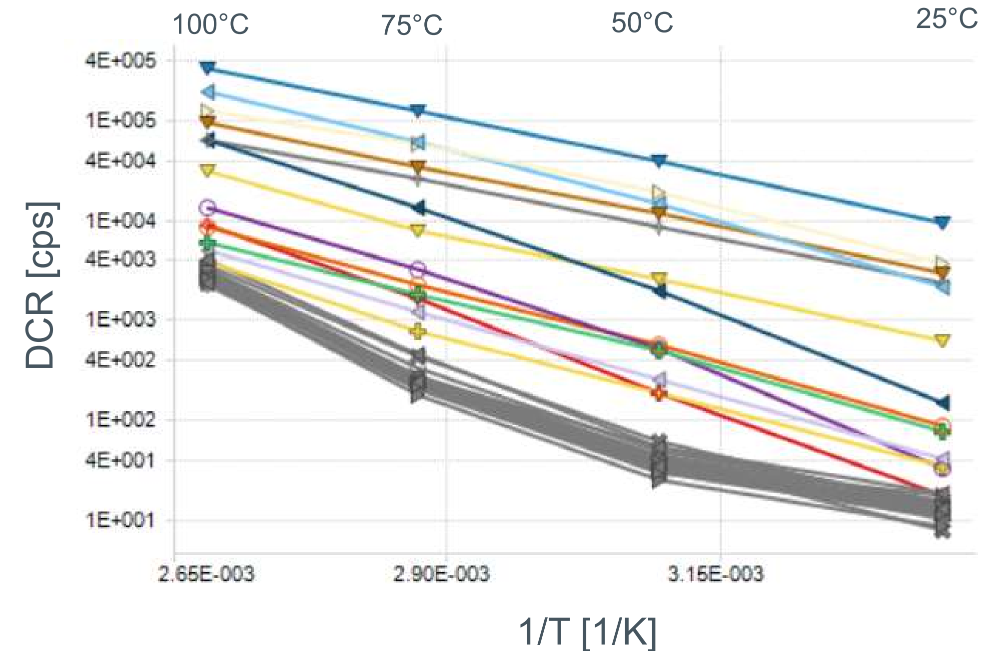


- At 75°C, median DCR is 270cps and the most noisy SPAD has a DCR of 130kcps. This is still a reasonable DCR at 75°C!

Activation Energy for Hot Pixels

FF=0.48





- DCR for 25°C, 50°C dominated by tunneling, for 75°C and 100°C by thermal diffusion.
- Noisy SPADs dominated by diffusion for all temperatures (25°C-100°C).
- Some SPADs are in the main population at 25°C, but end up as hot pixel at 100°C and vice versa.
- Activation energy tends to be lower for SPADs with larger DCR.

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Impact of Fill Factor on PDE and PDP

940nm

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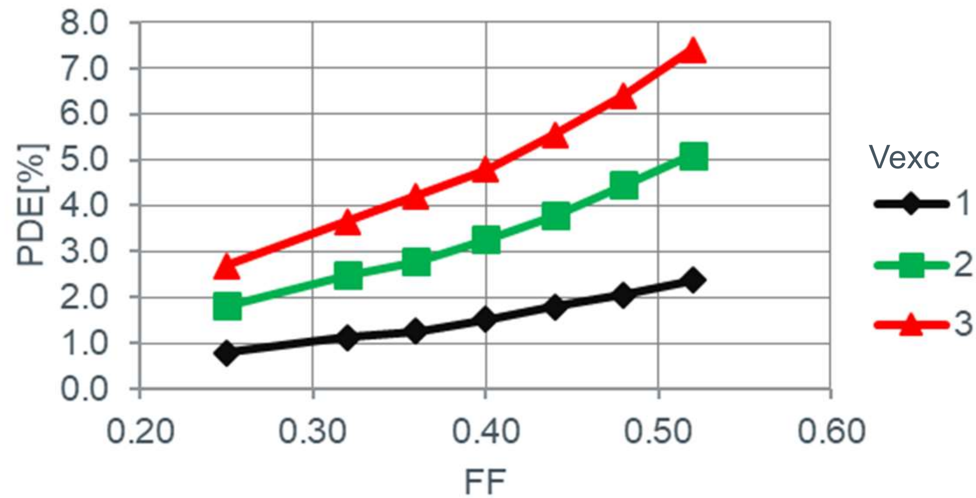

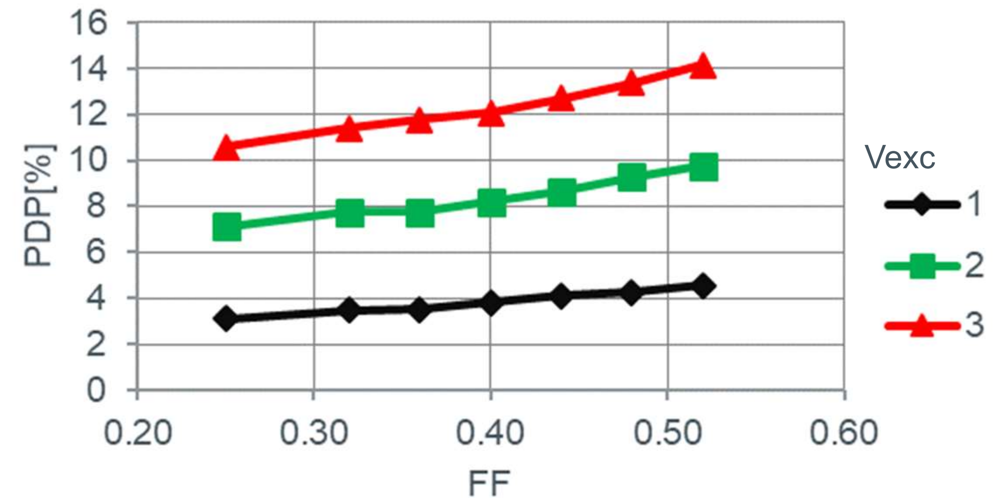

- PDE = PDP * FF
- PDE increases non-linearly with fill factor.
- Hence PDP is not constant over fill factor.

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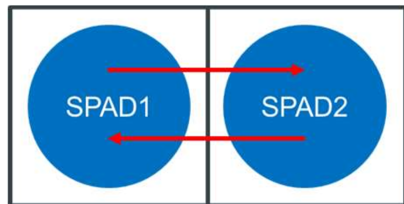
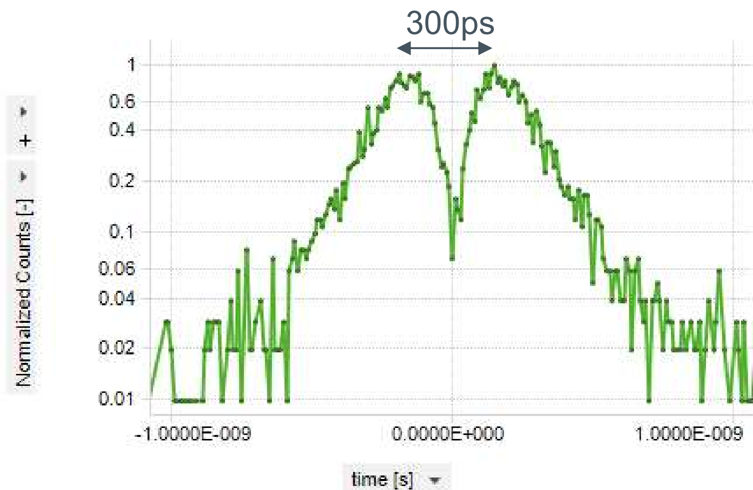
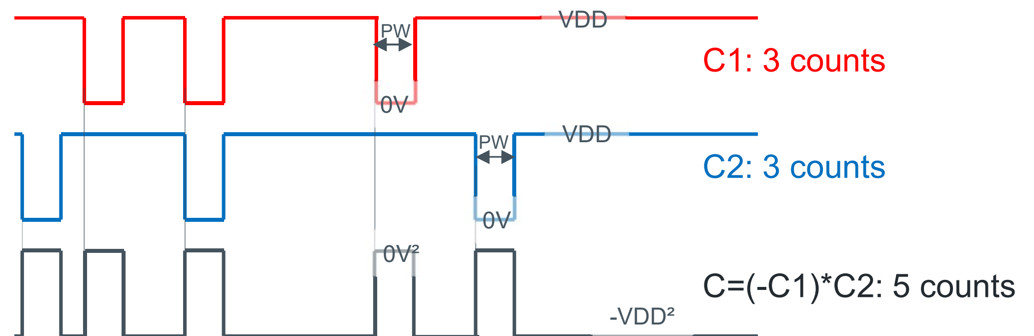
Crosstalk

Measurement Method



Light emission of SPAD1 (when triggered by DCR or light) can trigger the neighboring SPAD2 (or vice versa) → optical orthogonal cross-talk.





The cross talk between SPAD1 and SPAD2 is measured by counting the events for SPAD1, SPAD2 and both SPADs combined.

Cross talk is calculated as: (C1+C2-C)/C

Impact of Fill Factor and Vexc on Crosstalk (1)

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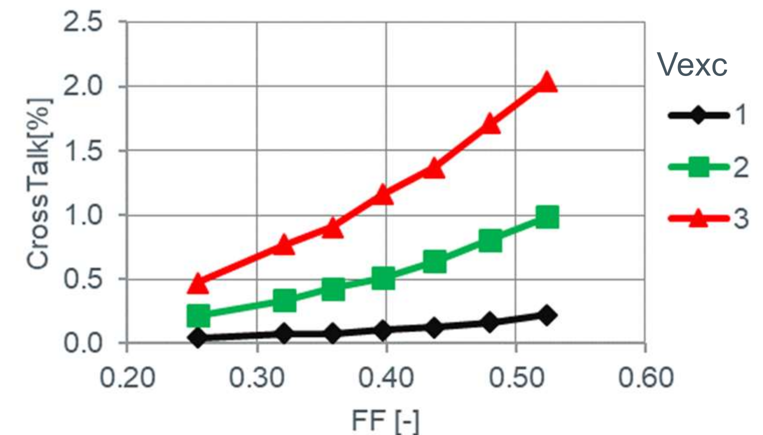
Cross talk increases with fill factor and excess bias voltage.

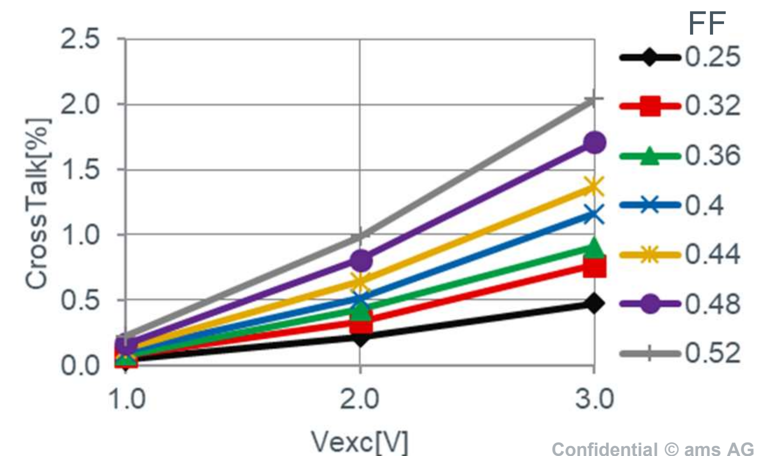
Fill factor:

- Distance between SPAD active area becomes smaller for larger fill factors.
- Capacitance increases with fill factor, thus the charge per SPAD trigger event is increased (more light emission).
- PDE increases with fill factor.

Excess bias voltage:

- PDE increases ~linearly with excess bias voltage. Thus probability of SPAD triggering is increased.
- The charge per SPAD trigger event increases with excess bias voltage (more light emission).





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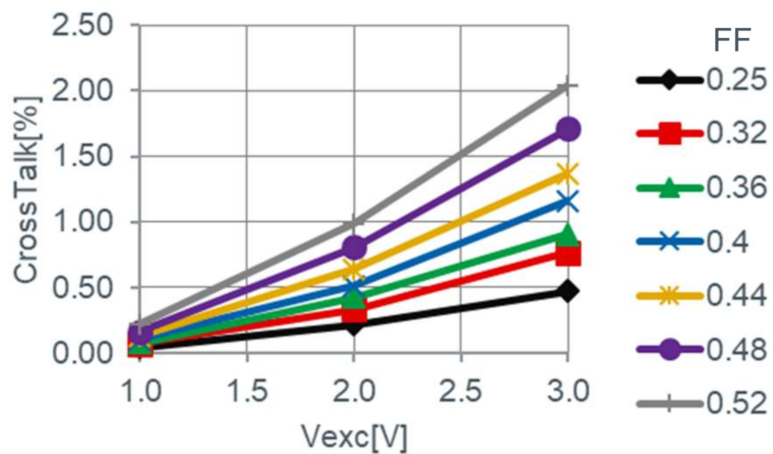
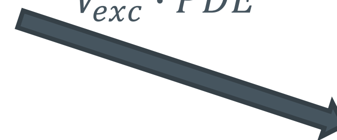
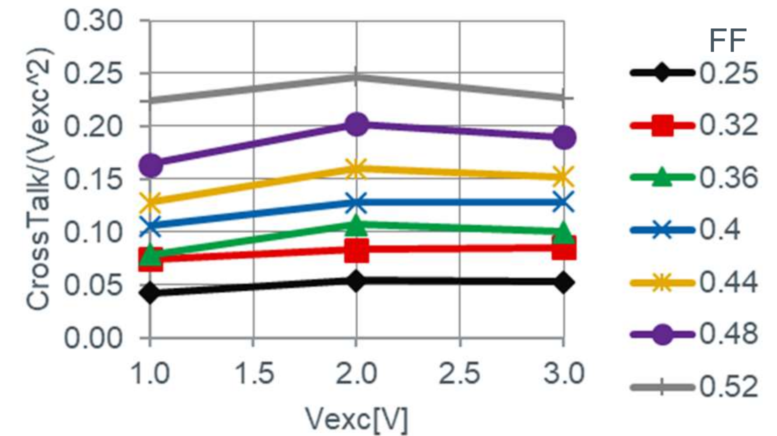
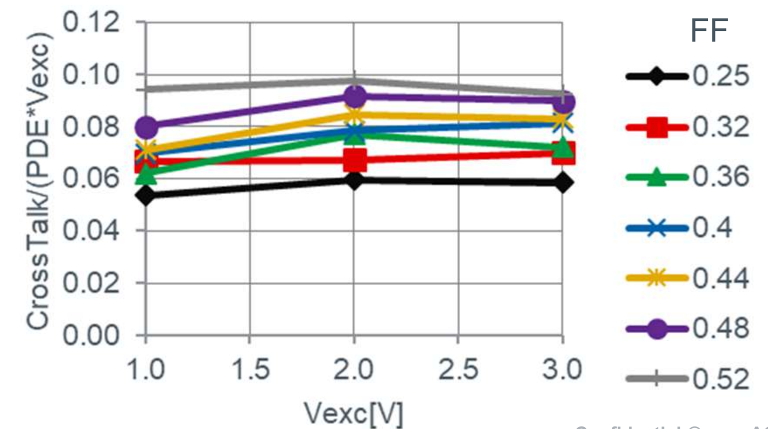
Impact of Fill Factor and Vexc on Crosstalk (2)









Results:

- Excess bias voltage impact nearly eliminated (less then 10% variation over Vexc remains).
- Normalization with V_{exc}^2: Remaining impact of the fill factor is much stronger, since increase of PDE with fill factor is not taken into account.
- Normalization with $V_{exc} \cdot PDE$: Remaining impact of fill factor due to reduced spacing with fill factor and increased capacitance.

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Crosstalk – PDE Trade-Off

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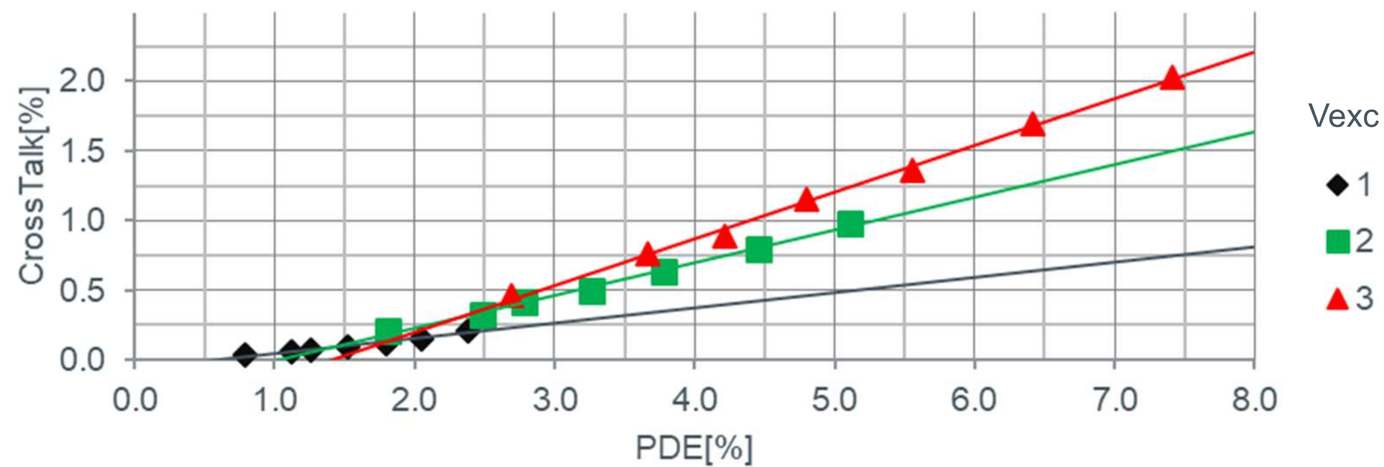

- Trade-off between PDE (@940nm) and cross-talk.
- Slightly worse trade off for larger excess bias voltage.

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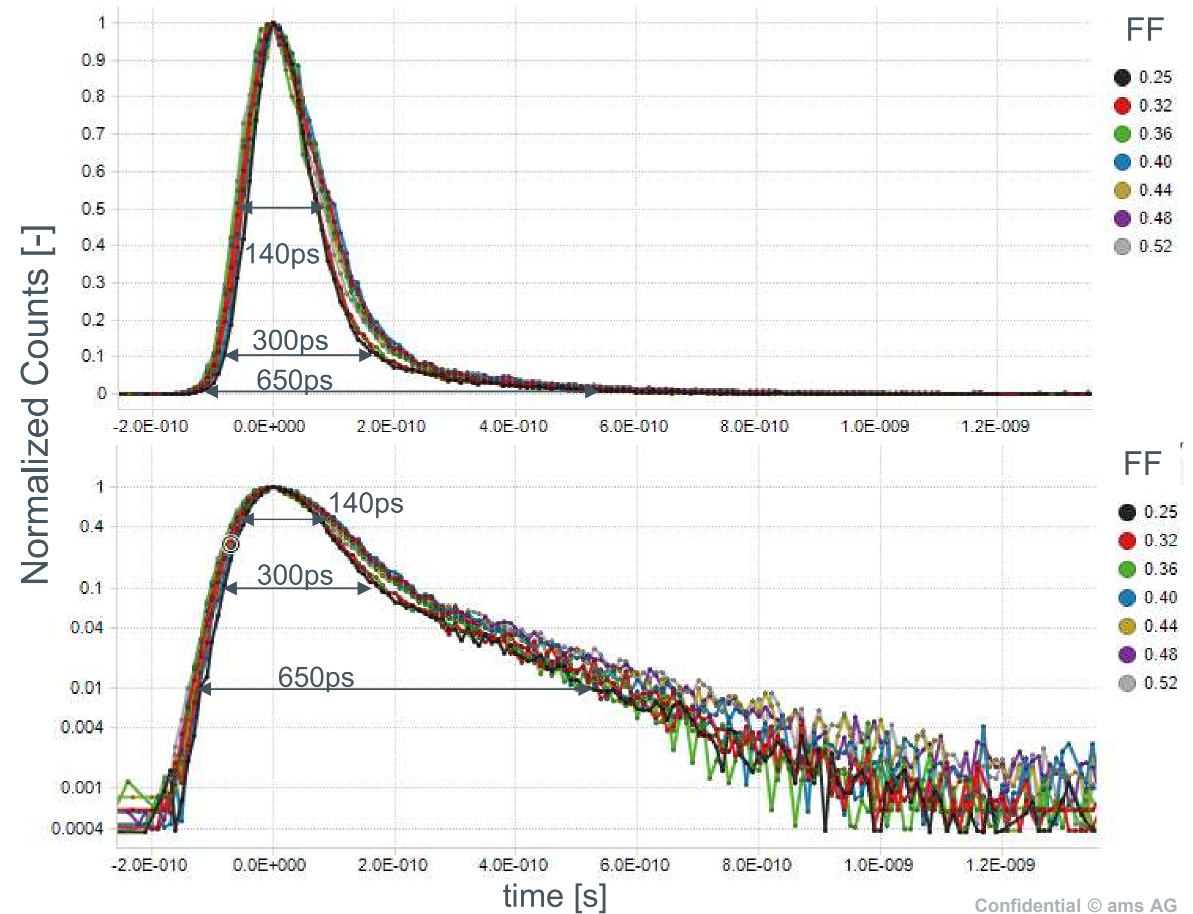
Timing Jitter @940nm

25°C, Vexc=2.0V, 940nm

FF	FWHM	FW@10%	FW@1%
0.25	120	260	630
0.32	130	270	650
0.36	140	290	640
0.40	150	320	680
0.44	140	310	660
0.48	145	310	790
0.52	140	300	830

- Good jitter characteristics at 940nm!



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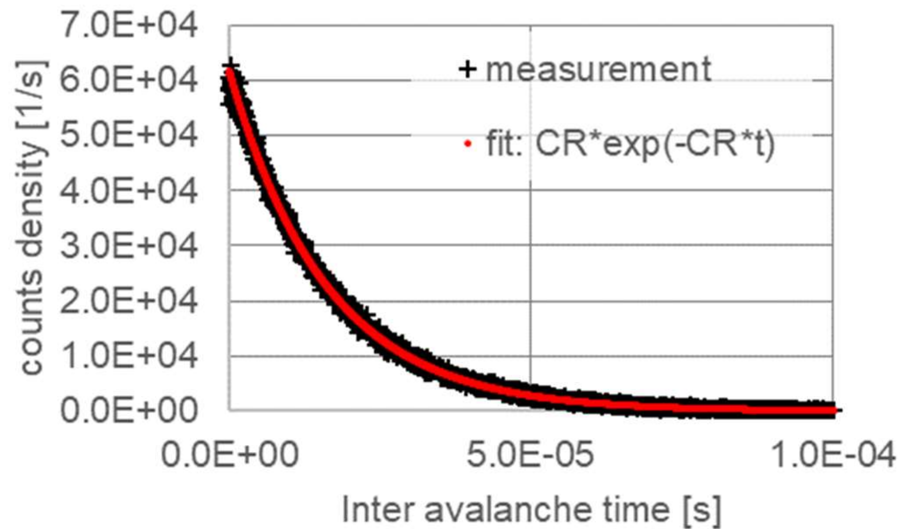
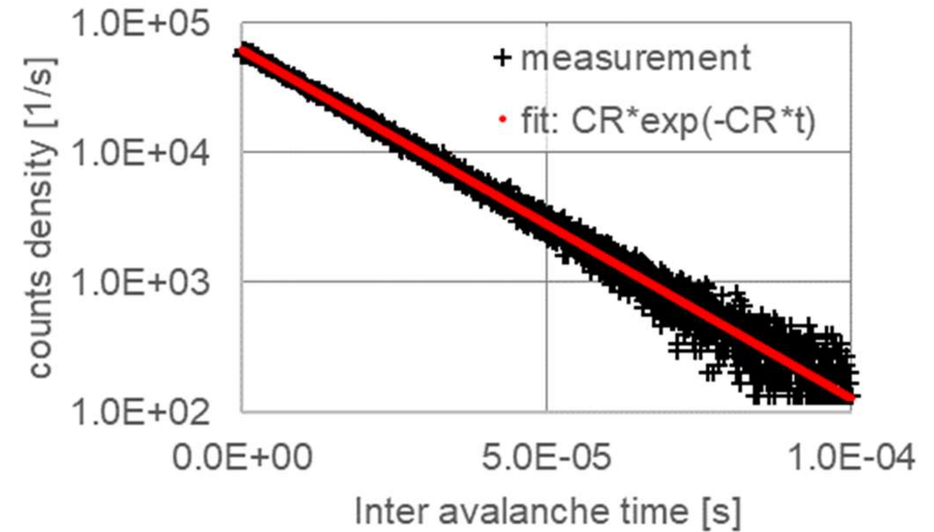
After Pulsing Probability

25°C, Vexc=3.0V





- After pulsing probability is measured by the inter-avalanche time method.
- Measurement taken with 7ns dead time and low light condition.
- After pulsing probability < 0.5%

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Performance Table

Typical parameters at 2V excess bias voltage, FF=0.48

Key Performance Indicator	Unit	Stacked BSI 45/40nm
Pixel pitch	um	~12.5
Breakdown voltage	V	17.0
DCR (25°C)	cps	14
DCR (75°C)	cps	270
PDE at 940nm	%	4.5
Timing jitter FWHM at 940nm	ps	145
Timing jitter (FW10%M) at 940nm	ps	310
Timing jitter (FW1%M) at 940nm	ps	790
After pulsing probability at 7ns dead time	%	<0.5
Cross talk probability	%	0.8

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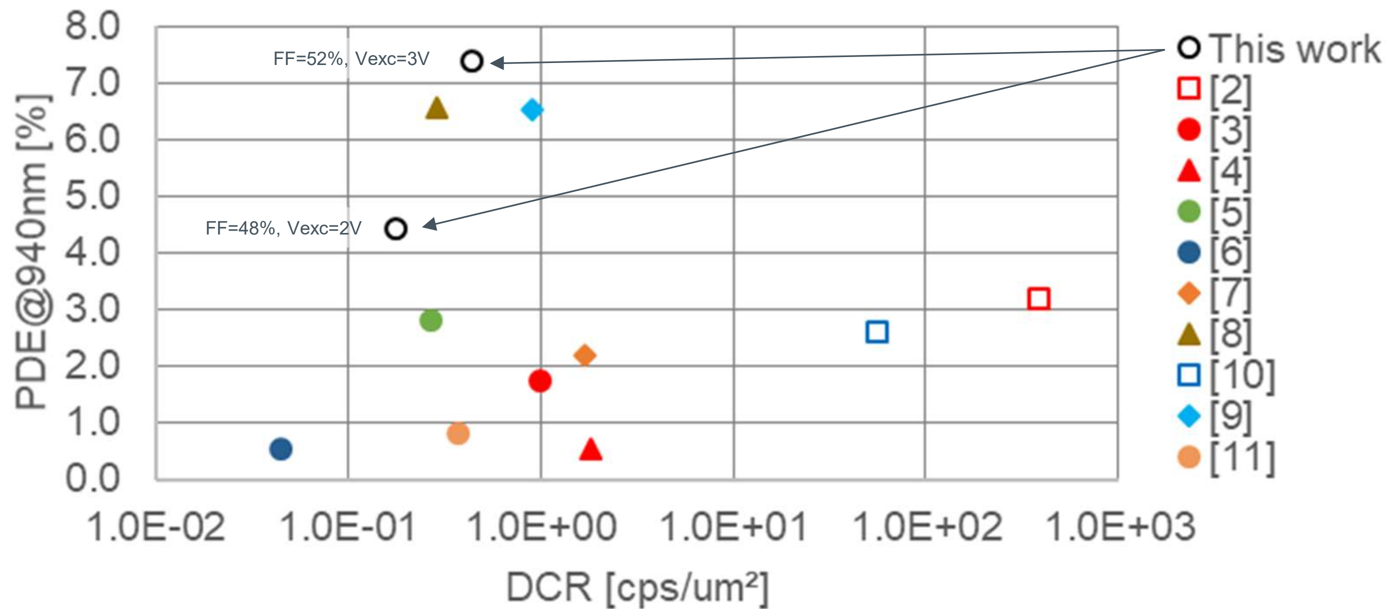
Benchmark



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