Small and Smart SPAD Pixels

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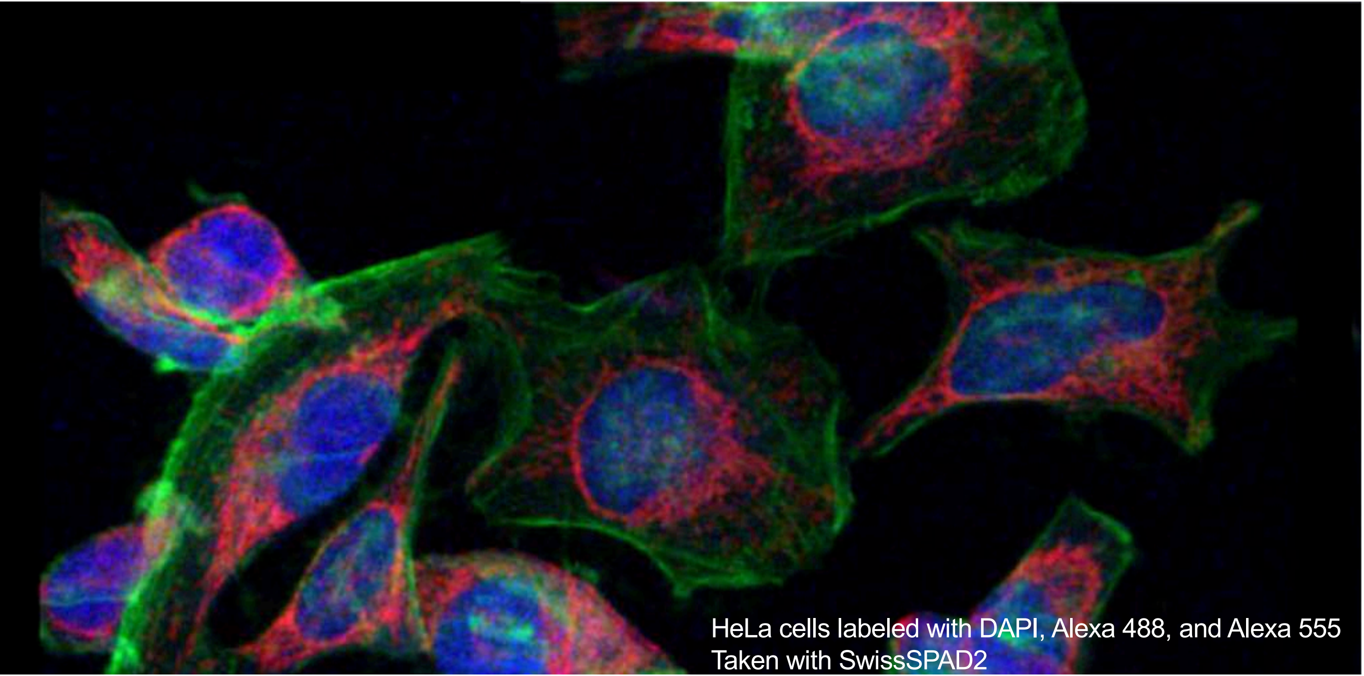
ISSW 2020

Large-Format SPAD Cameras – Why?

- SPADs are fast and have high timing resolution – ideal for 3D/LiDAR
- SPADs are natively digital – inherently simpler processing
- Emerging applications requiring both – larger formats are needed

Example: Fluorescence Image Taken in Milliseconds



HeLa cells labeled with DAPI, Alexa 488, and Alexa 555
Taken with SwissSPAD2

This has been made possible by large-format cameras!

3 Key Challenges of a Large-format SPAD Camera

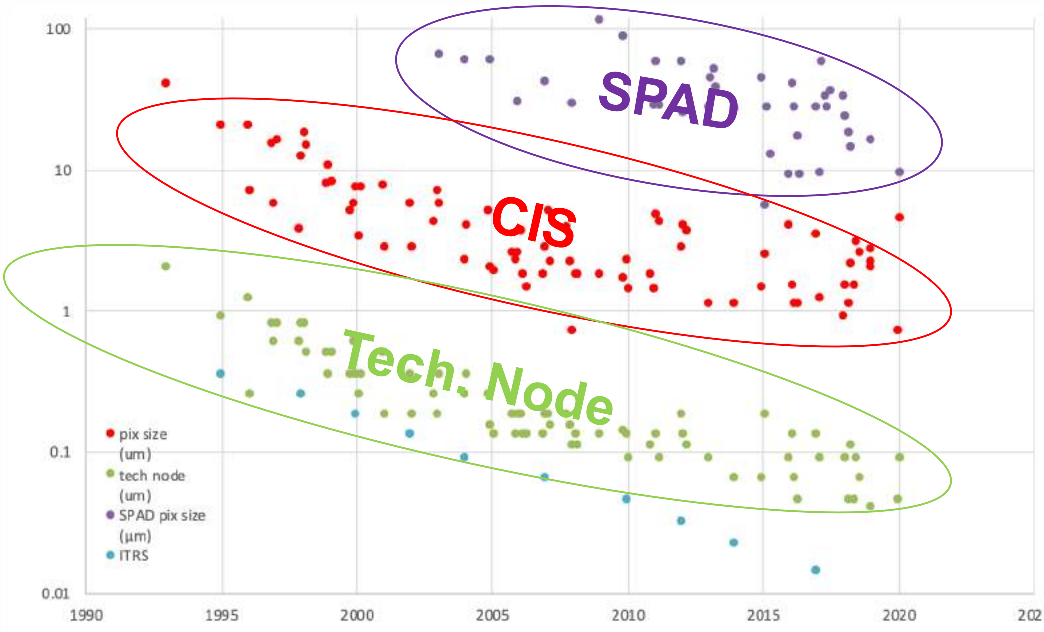
1. Pixel pitch

2. Power

3. *Data*

Challenge 1: Pixel pitch

Why is SPAD Pixel Pitch so Far Behind?

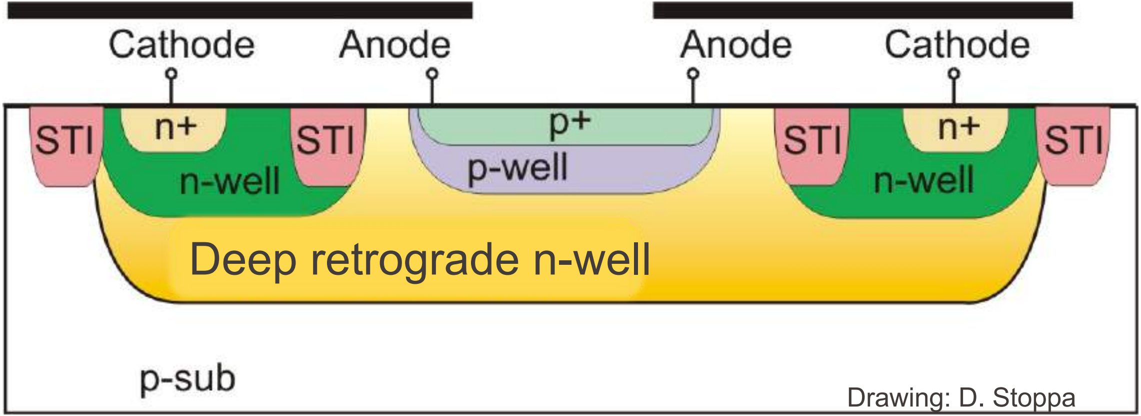


Source: Albert Theuwissen, Harald Homulle, and Edoardo Charbon

Reasons for Delayed SPAD Miniaturization

- High voltage requirements – only older nodes support them
- Guard rings
- Backside illumination and 3D-stacking came later to SPADs
- For many years, SPADs were considered of no economic interest!

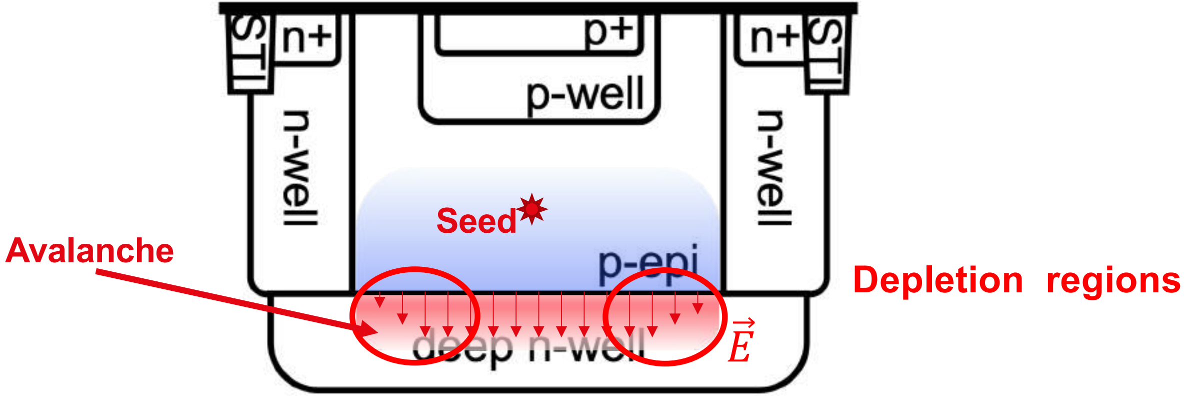
Mostly Guard Rings



Henderson *et al.*, 2009

- The guard ring is implicitly obtained from lightly-doped deep n-well (on the surface)
- Suitable for deep-submicron processes (in this case 130nm)
- Compatible with triple-well process
- Good DCR performance

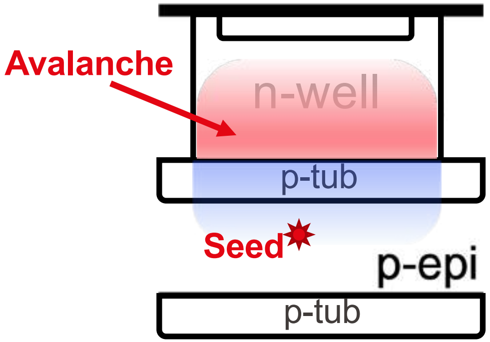
Compact Alternative: the p-i-n SPAD Structure



C. Veerappan and E. Charbon, 2015

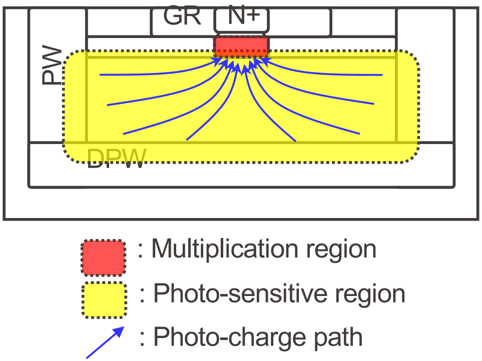
Guard rings reduce E-field at the edges to suppress premature edge breakdown

Vertical Flow APDs (VAPD)



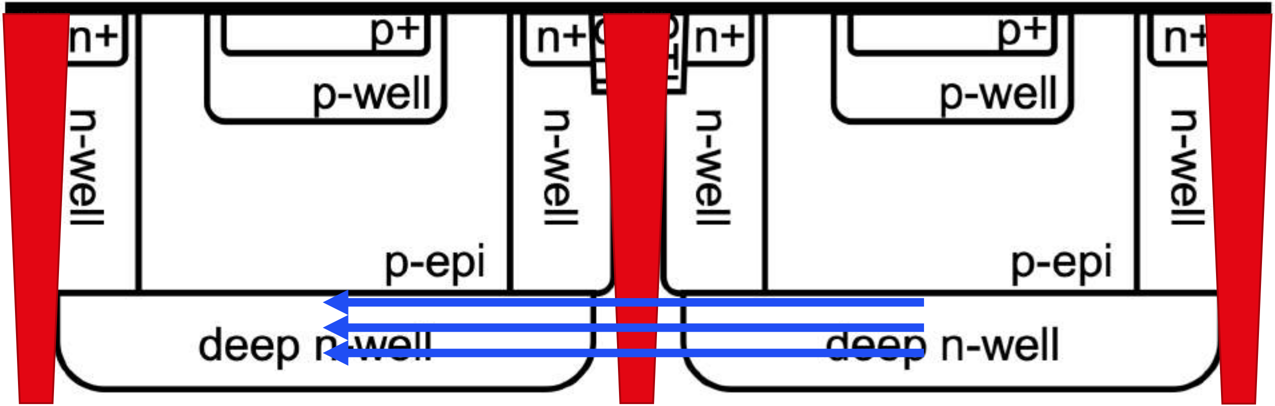
Y. Hirose *et al.*, ISSCC 2019

Charge-focusing SPAD



K. Morimoto, ISSW 2020

Densifying Pixels: Deep Trench Isolation



Photons produced by impact ionization may trigger an avalanche in a neighbor pixel (cross-talk)

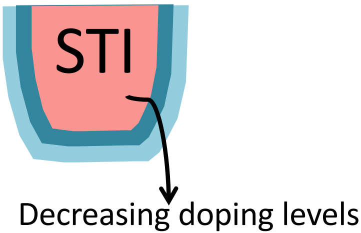
DTIs reduce optical cross-talk between SPADs

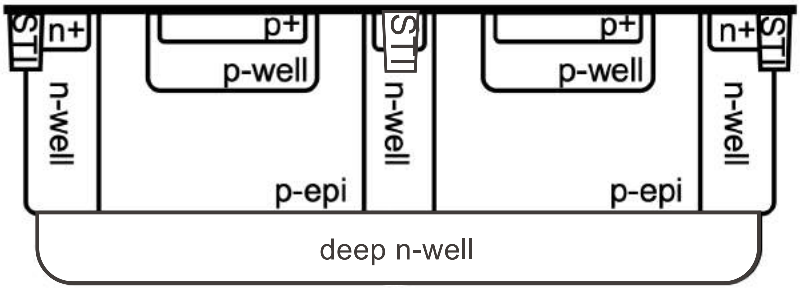
Achieving Very Low Pitch

- Share n-wells and deep n-wells
- Share guard rings
- Share electronics
- 3D-stacking
- Microlenses

Achieving Very Low Pitch (1)

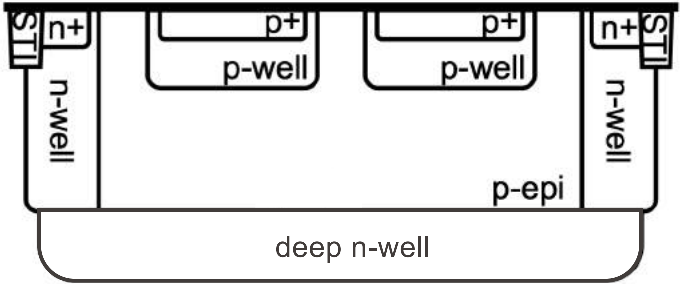
- <u>Share n-wells and deep n-wells</u>
- Share guard rings
- Share electronics
- 3D-stacking
- Microlenses





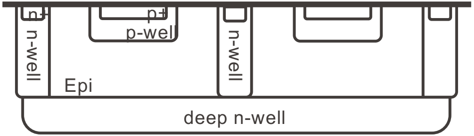
Achieving Very Low Pitch (2)

- Share n-wells and deep n-wells
- Share guard rings
- Share electronics
- 3D-stacking
- Microlenses

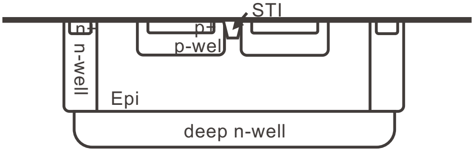


Achieving Very Low Pitch (1-2)

Well sharing

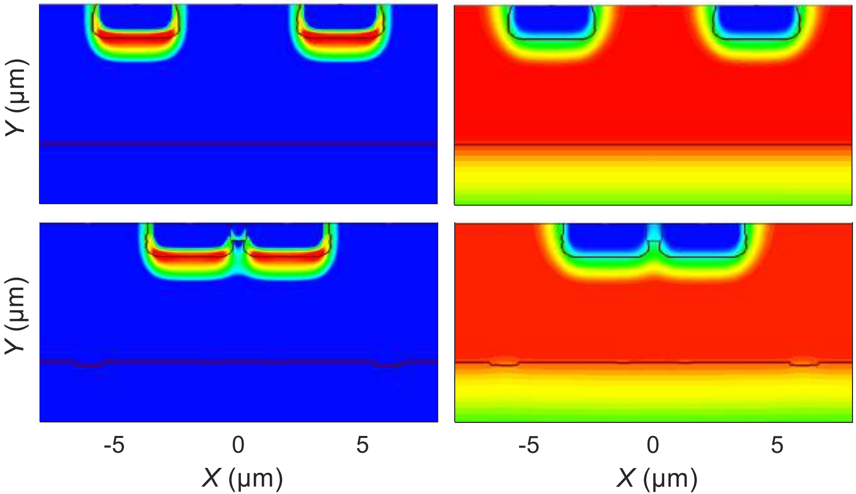


Guard-ring sharing



Electric field

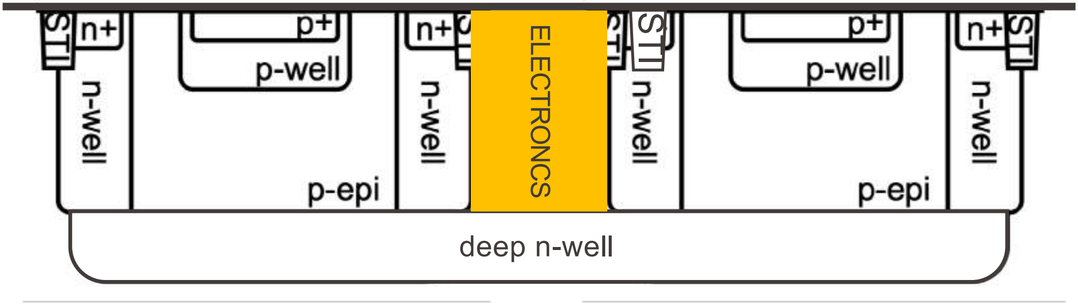
Electrostatic potential



K. Morimoto and E. Charbon
Optics Express, 2020

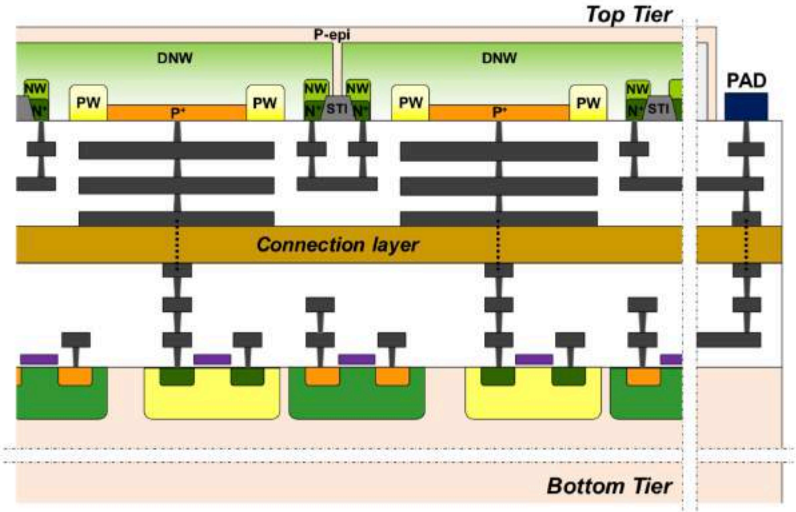
Achieving Very Low Pitch (3)

- Share n-wells and deep n-wells
- Share guard rings
- Share electronics
- 3-Stacking
- Microlenses



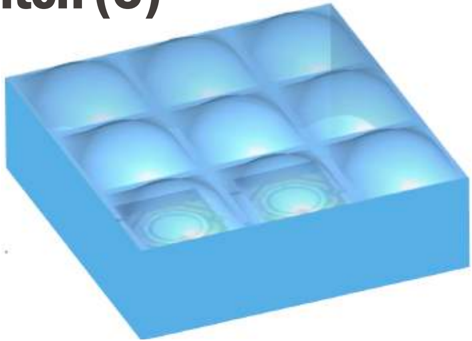
Achieving Very Low Pitch (4)

- Share n-wells and deep n-wells
- Share guard rings
- Share electronics
- 3D-Stacking
- Microlenses



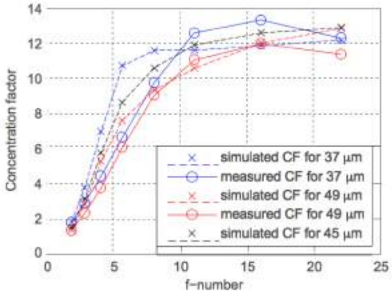
M.J. Lee et al., *JSTQE* 2018

Achieving Very Low Pitch (5)



- Share n-wells and deep n-wells
- Share guard rings
- Share electronics
- 3D-stacking
- Microlenses
  - Electrical μlens. e.g. C. Veerappan, IISW'13
  - Optical μlens

Smaller pixels with lower fill factor become attractive because of low DCR



I.M. Antolovic, *et al.*, Trans. Electron Dev. 2015

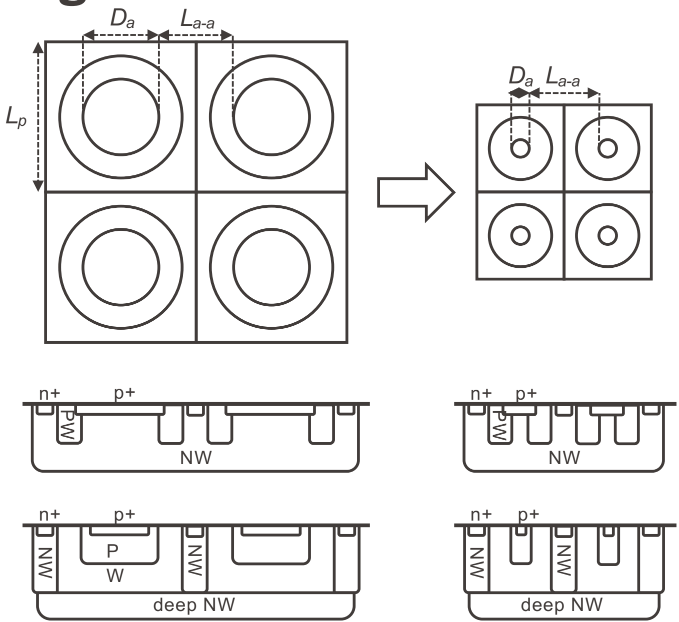
Scaling Law

Pixel pitch: $L_p = D_a + L_{a\text{-}a}$

Assumptions:

- Uniform square grid
- Circular active area & GR
- Pixel circuit not included
- Scaling parameter: L_p
- $L_{a\text{-}a}$ not scaled with L_p

Kazuhiro Morimoto, *PhD Thesis*
Lausanne, June 2020



Scaling Law

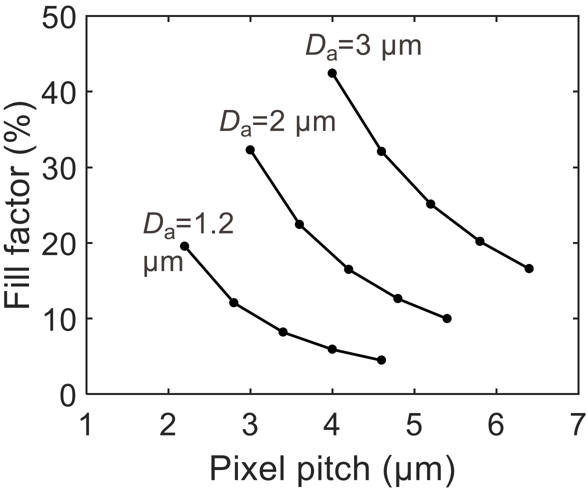
Characteristics	Equation
Fill factor (%)	$\frac{(L_p - L_{a-a})^2}{L_p^2}$
PDP (%)	$(\frac{L_p - L_{a-a} - 2r_{in}}{L_p - L_{a-a}})^2$
PDE (%)	$\frac{(L_p - L_{a-a} - 2r_{in})^2}{L_p^2}$
DCR (cps)	$(L_p - L_{a-a} - 2r_{in})^2$
DCR density (cps/μm^2)	$\frac{(L_p - L_{a-a} - 2r_{in})^2}{(L_p - L_{a-a})^2}$
Afterpulsing probability (%)	$\left[\frac{\pi\epsilon(L_p - L_{a-a})^2}{4W_{eff}} + C_0\right]$,
Crosstalk probability (%)	$\left[\frac{\pi\epsilon(L_p - L_{a-a})^2}{4W_{eff}} + C_0\right] \times \frac{e^{-\alpha L_p}}{L_p^2} \times \frac{(L_p - L_{a-a} - 2r_{in})^2}{L_p^2}$
Power consumption (pJ)	$\left[\frac{\pi\epsilon(L_p - L_{a-a})^2}{4W_{eff}} + C_0\right]$

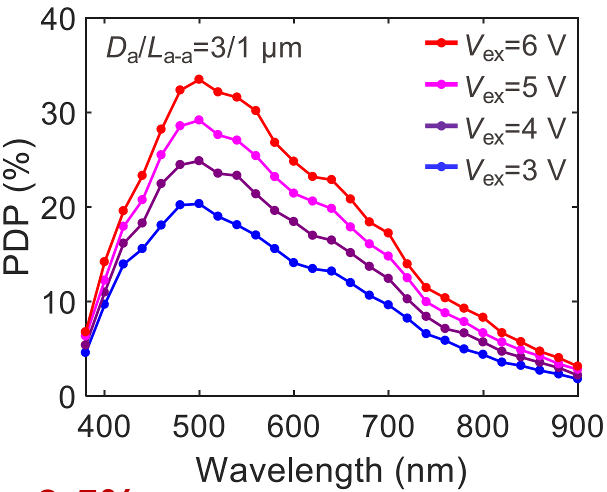
Pixel pitch:
$L_p = D_a + L_{a\text{-}a}$

Kazuhiro Morimoto, *PhD Thesis*
Lausanne, June 2020

Pixel Scaling

Pixel pitch:
$L_p = D_a + L_{a\text{-}a}$



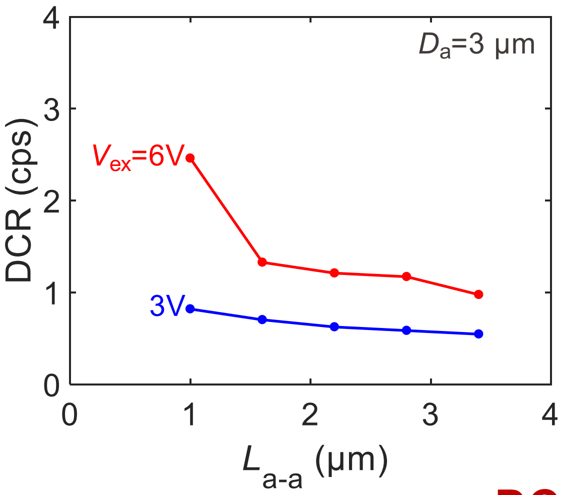


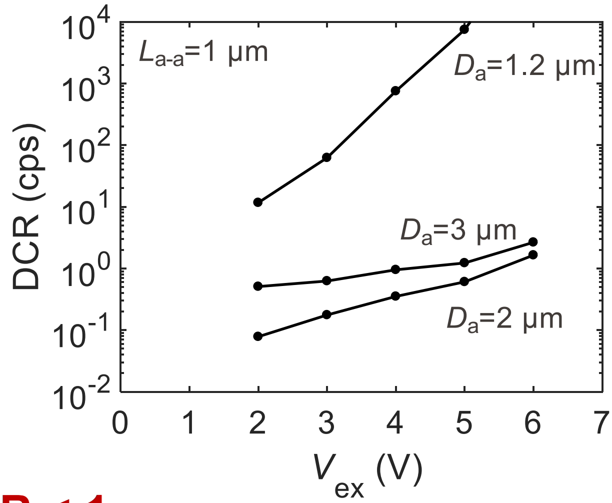
FF = 9.5%

K. Morimoto and E. Charbon
Optics Express, 2020

Pixel Scaling

Pixel pitch:
$L_p = D_a + L_{a\text{-}a}$



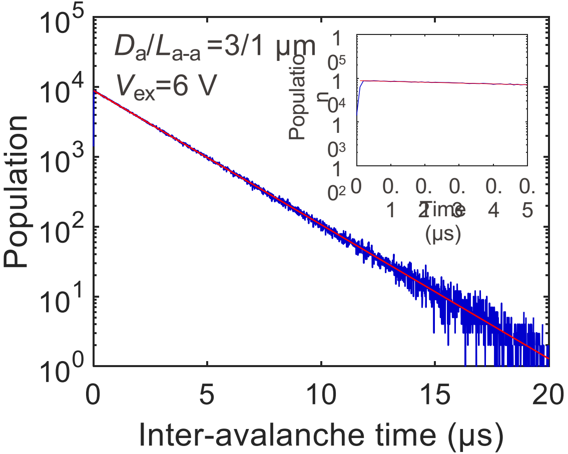


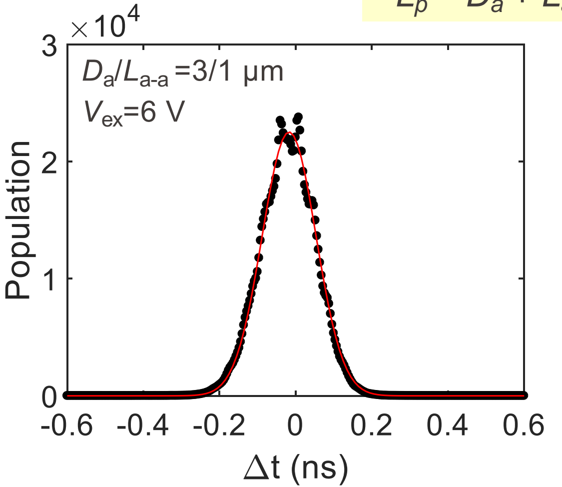
DCR < 1cps

K. Morimoto and E. Charbon
Optics Express, 2020

Pixel Scaling

Pixel pitch:
$L_p = D_a + L_{a\text{-}a}$

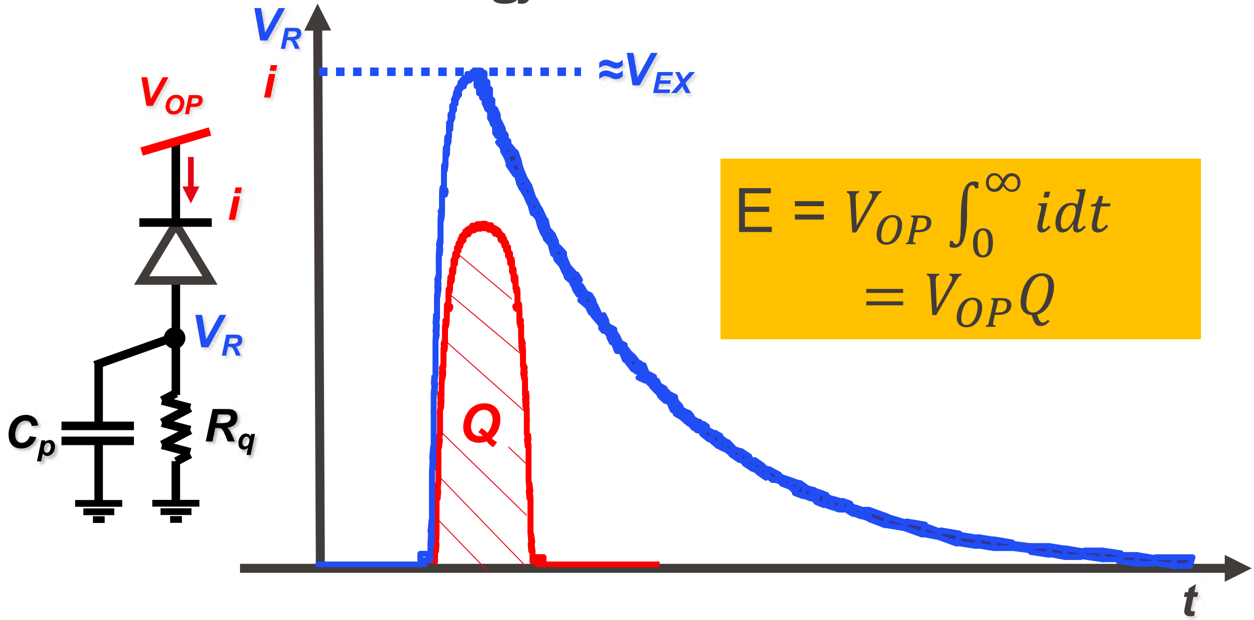




Afterpulsing probability ≤ 0.21%, timing jitter ≤ 88 ps

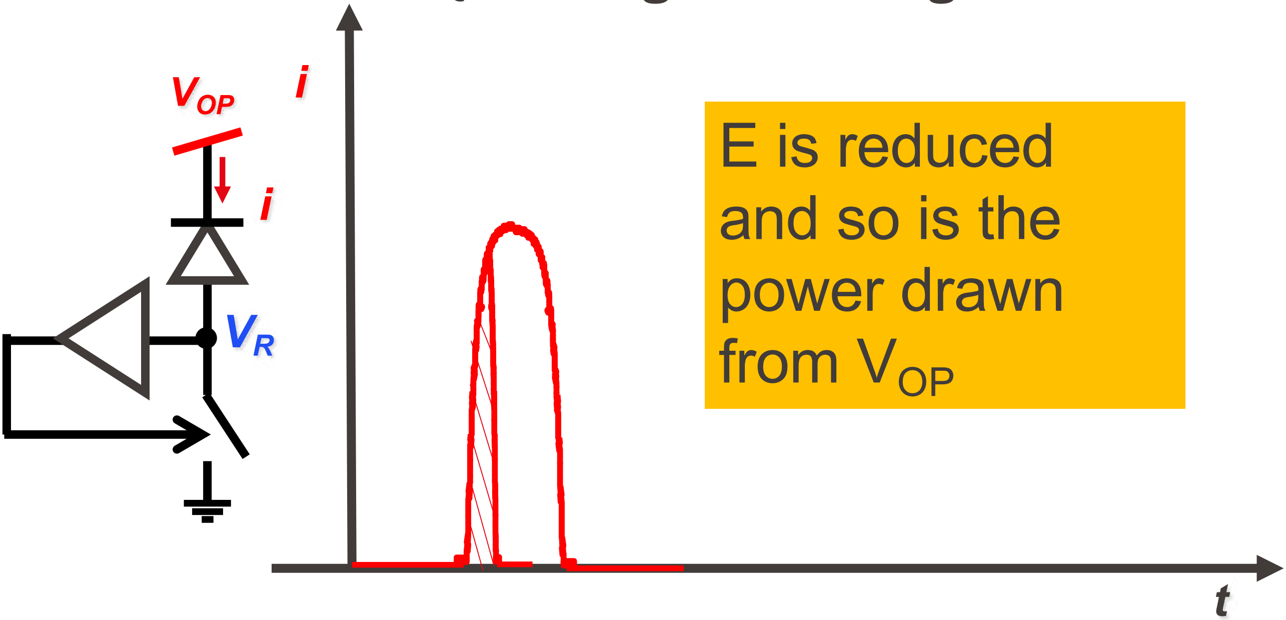
Challenge 2: Power

Energy of the Process



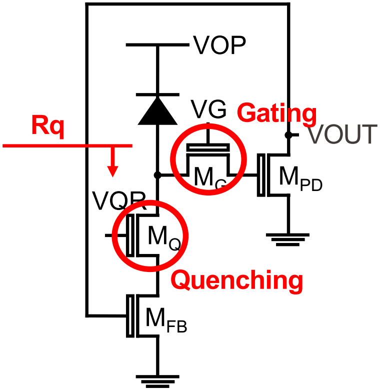
$$E = V_{OP} \int_0^{\infty} i\,dt$$
$$= V_{OP} Q$$

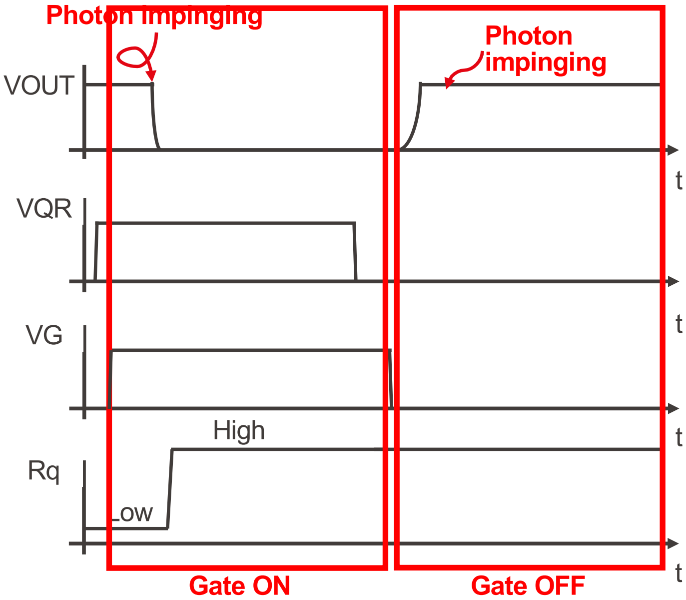
Fast Quenching and Recharge



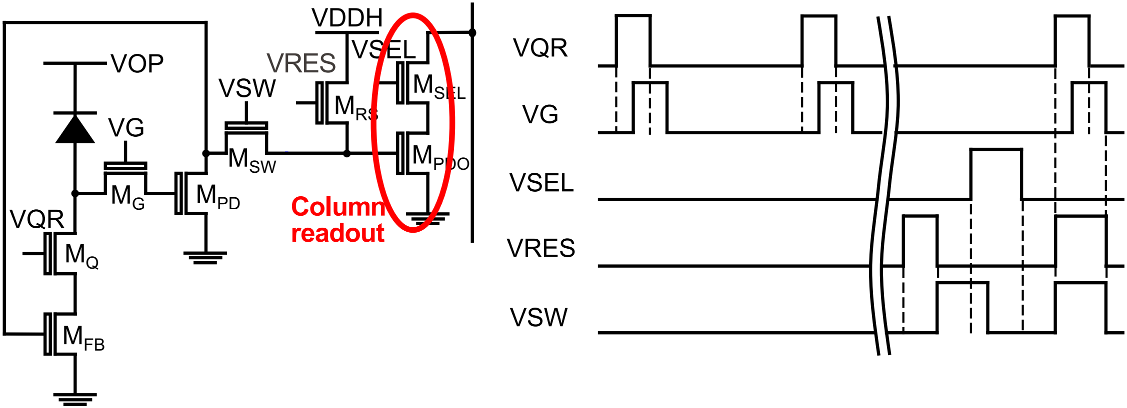
E is reduced and so is the power drawn from V_{OP}

Fast Quenching, Recharge, and Gating



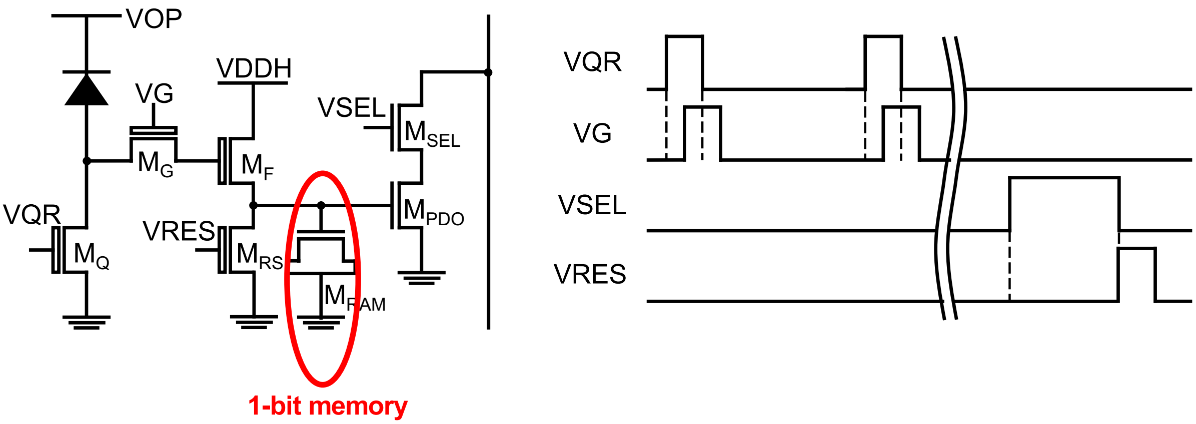


Pixel Readout Sharing (Pixel B)

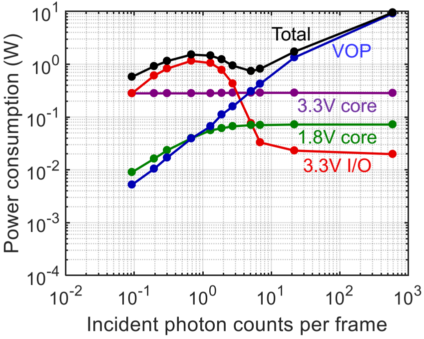


No Readout Sharing (Pixel A)

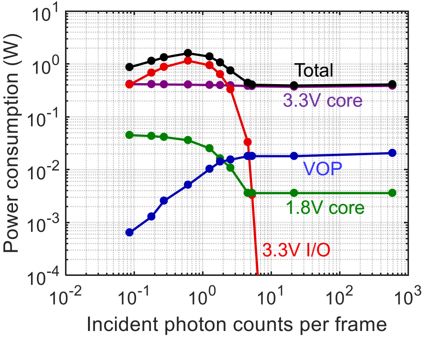
Pixel A: 7Trs./pix



Achieving Low Power



Pixel A



Pixel B

K. Morimoto et al., ArXiv preprint arXiv:1912.12910
K. Morimoto et al., *Optica* 2020

Challenge 3: Data

Achieving High Data Readout: Smart Pixels

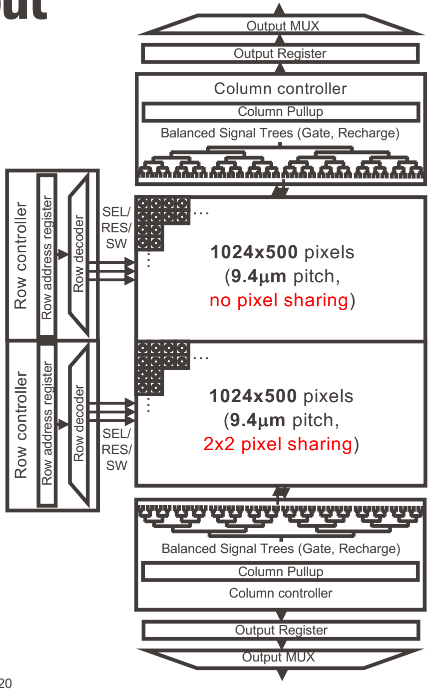
- Fast data transfer from pixel to bottom of the chip via low-C wires and appropriate buffers
- Memory-style readout via sense-amplifiers
- Pipelining
- LVDS output
- Processing
  - on chip
  - on column
  - on pixel

The MegaX Architecture

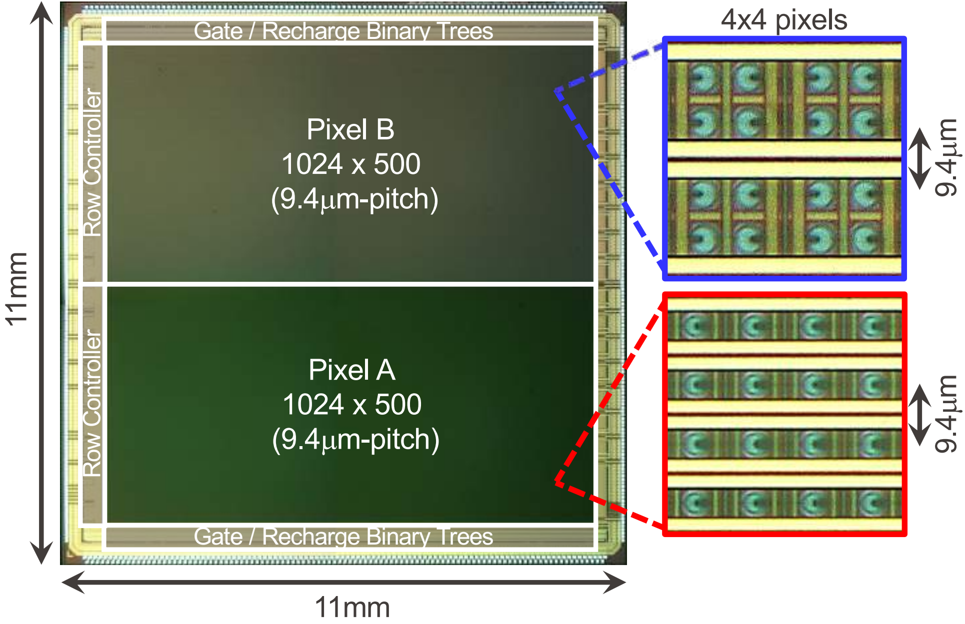
MegaX's High-Speed Read-out

- 1024 x 1000 pixels
- 9.4μm pitch
- 3.8ns gating
- 24,000 fps
- 24.5Gb/s
- VDD: 1.8V
- VBD: 24.7V

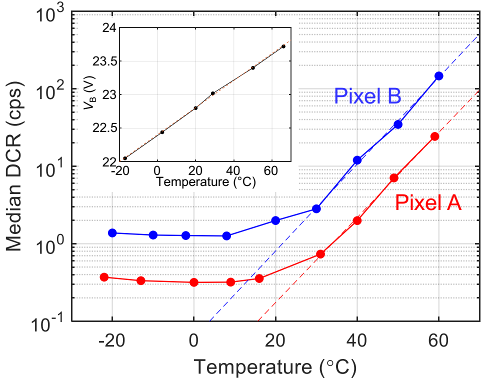
K. Morimoto *et al.*, *Optica* 2020

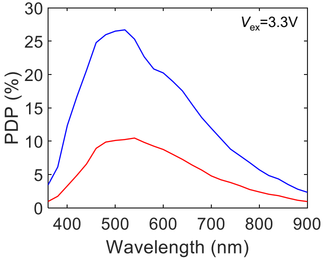


MegaX – Fabricated Chip (180nm CIS Technology)



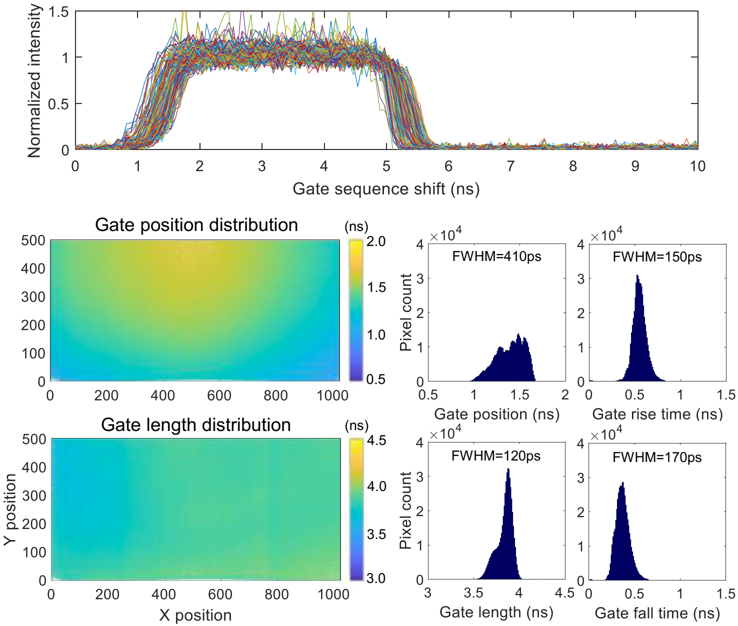
MegaX: Overall Performance



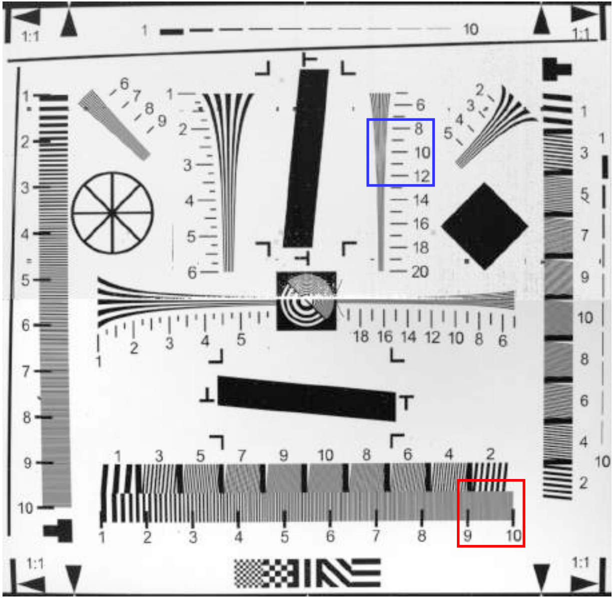


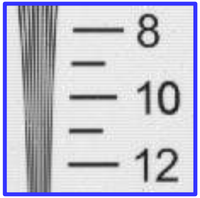
Process technology	180nm CMOS
Chip size (mm^2)	11×11
Sensor resolution	1024×1000
Pixel size (μm)	9.4
Fill factor (%)	7.0/13.4
Pixel output bit depth (b)	1
Number of pixel transistors	7/5.75
Median DCR (cps)	0.4/2.0 (V_{ex}=3.3V)
Maximum PDP (%)	10.5/26.7 (V_{ex}=3.3V)
Crosstalk (%)	0.17/0.39 (V_{ex}=3.3V)
Minimum gate length (ns)	3.8
Frame rate (fps)	24,000 (1b)
Power dissipation (W)	0.284/0.535

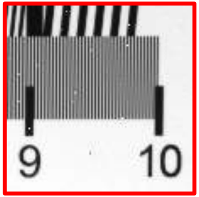
MegaX: Gating



MegaX: Pixel Resolution



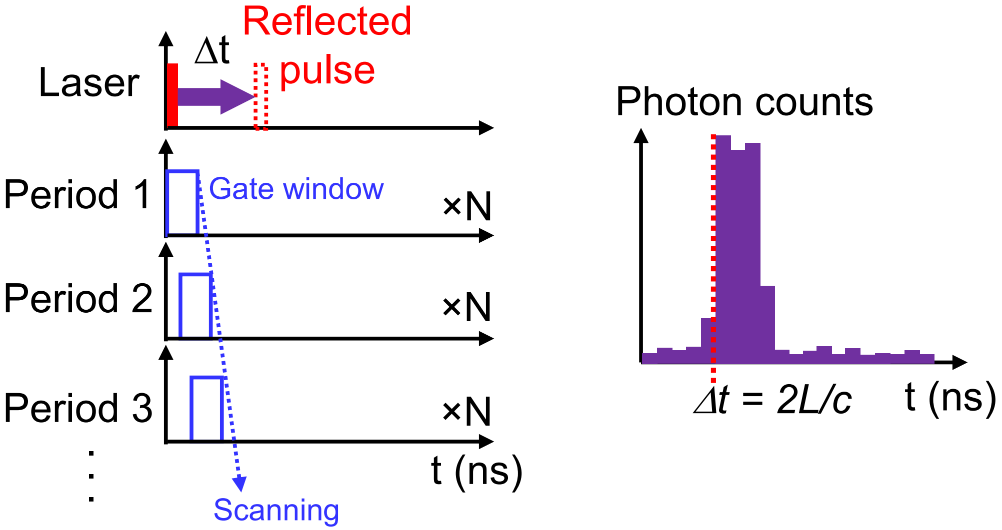




MegaX: Intensity Vision

K. Morimoto *et al.*, *Optica* 2020

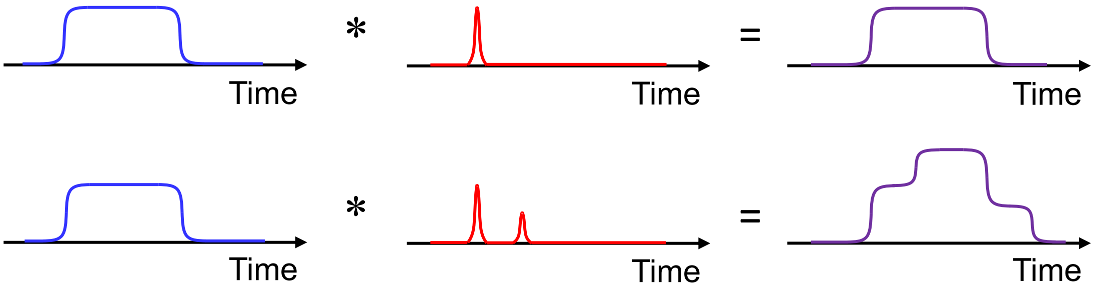
MegaX: LiDAR Vision



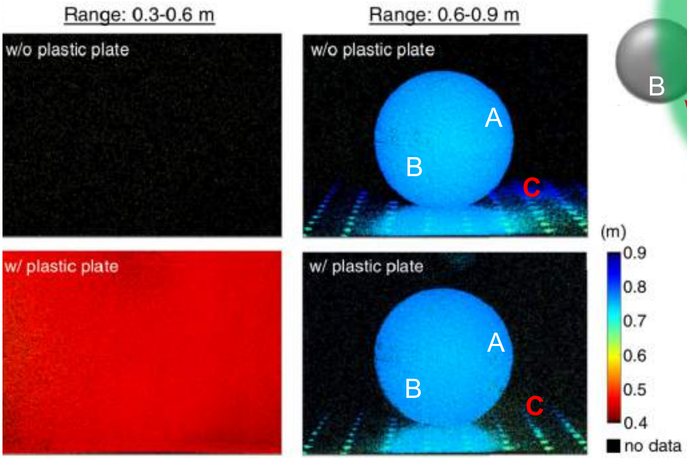
MegaX: LiDAR Vision

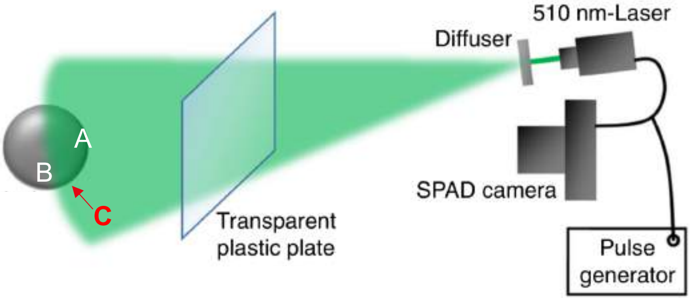
MegaX: Multiple Surfaces

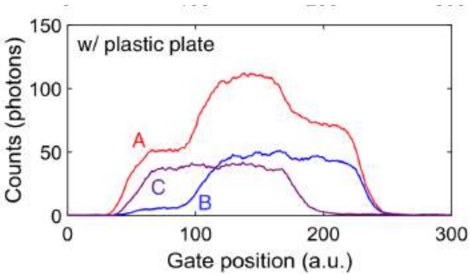
Gating window profile: $f(t)$ Photon distribution: $g(t)$ Detected intensity: $h(t)$



MegaX: Multiple Surfaces

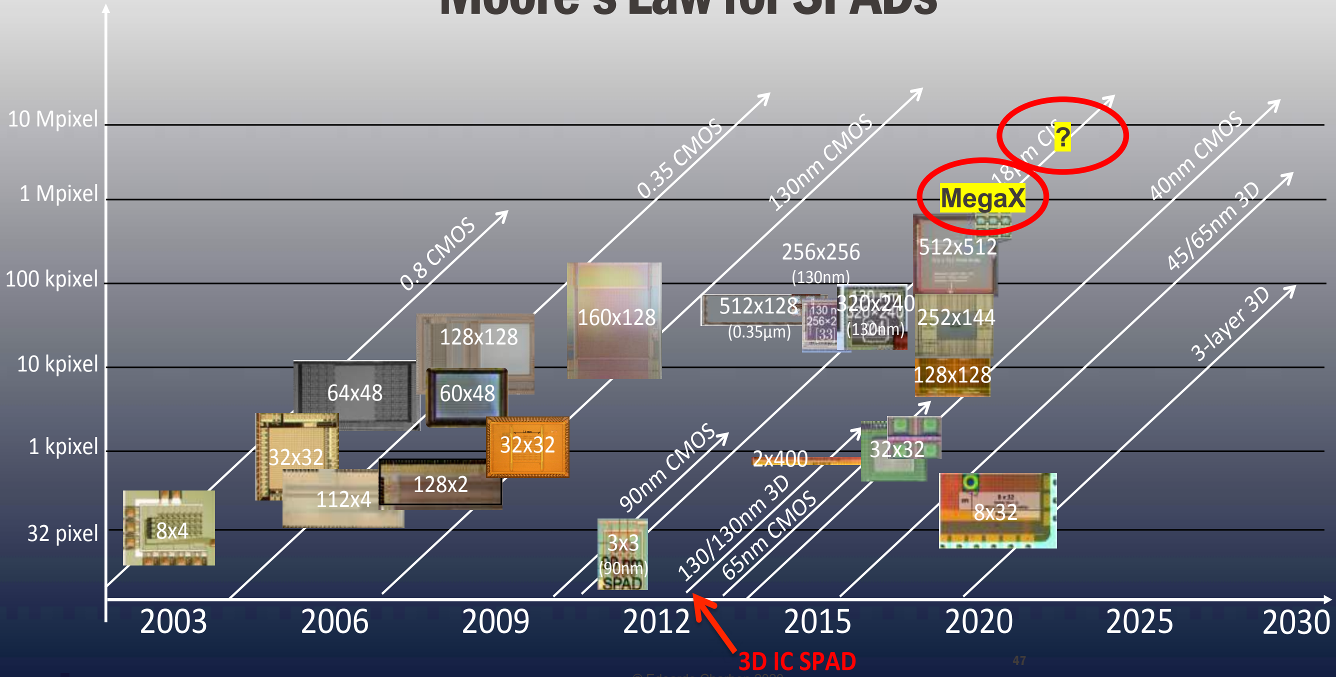






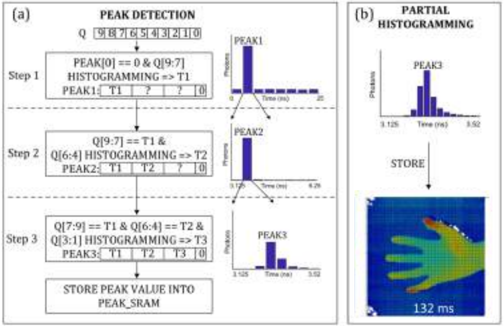
Outlook

Moore's Law for SPADs

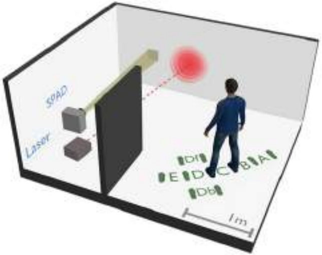


Smart Pixel (Networks)

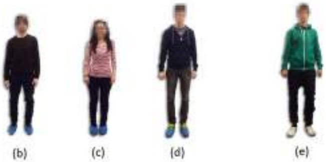
- Peak detection and smart histogramming to reduce data transfer
- On-pixel or on-chip algorithms for e.g. lifetime extraction
- Neural networks <u>on</u> SPADs



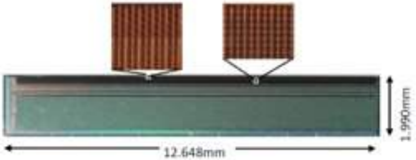
C. Zhang *et al*., *JSSC* 2019



Off SPADs, for now

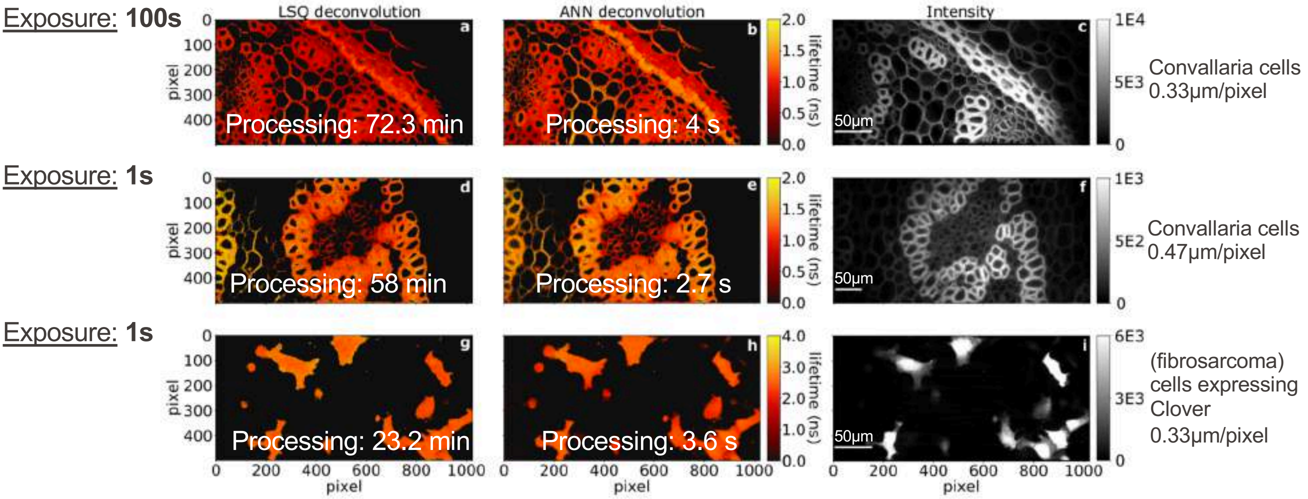


P. Caramazza *et al*., *Sci. Rep*. 2018



N. Finlayson *et al*., *ISSW* 2020

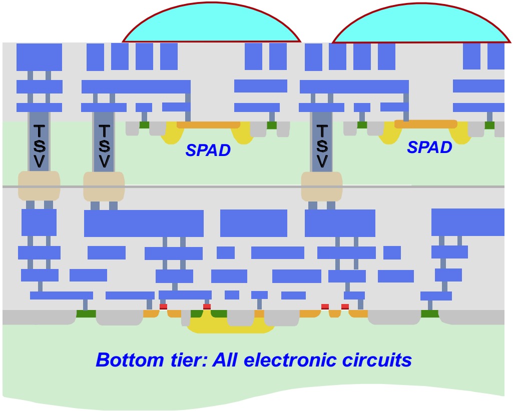
MegaX: Extracting Fluorescence Lifetime with ANNs



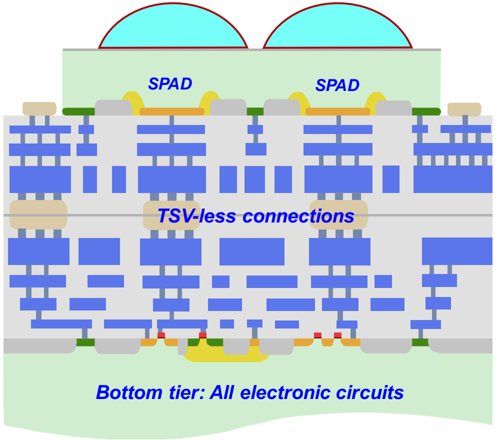
V. Zickus *et al.*, bioRxiv preprint Doi: https://doi.org/10.1101/2020.06.07.138685K.

3D-Stacking: BSI/FSI

- Better fill factor (potentially)
- Better space utilization
- Better cooling (with measures)



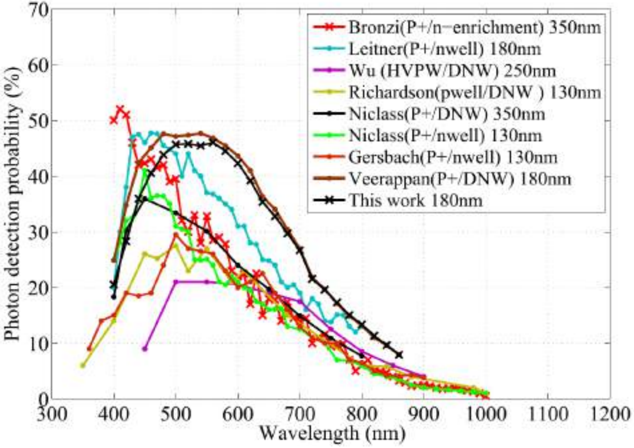
FSI- Front-side illumination



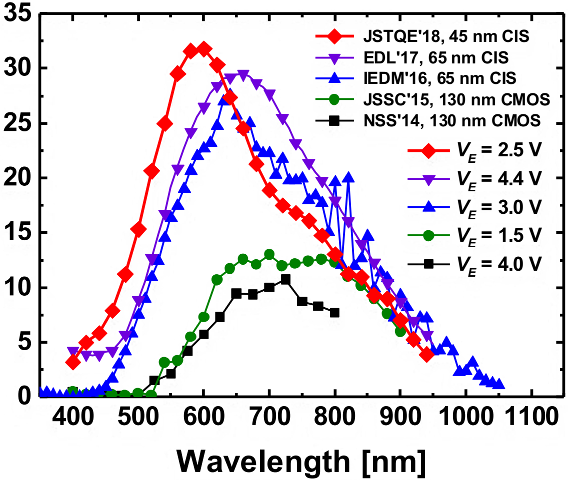
BSI- Backside illumination

SPAD BSI vs. FSI

FSI SPAD PDP



BSI SPAD PDP

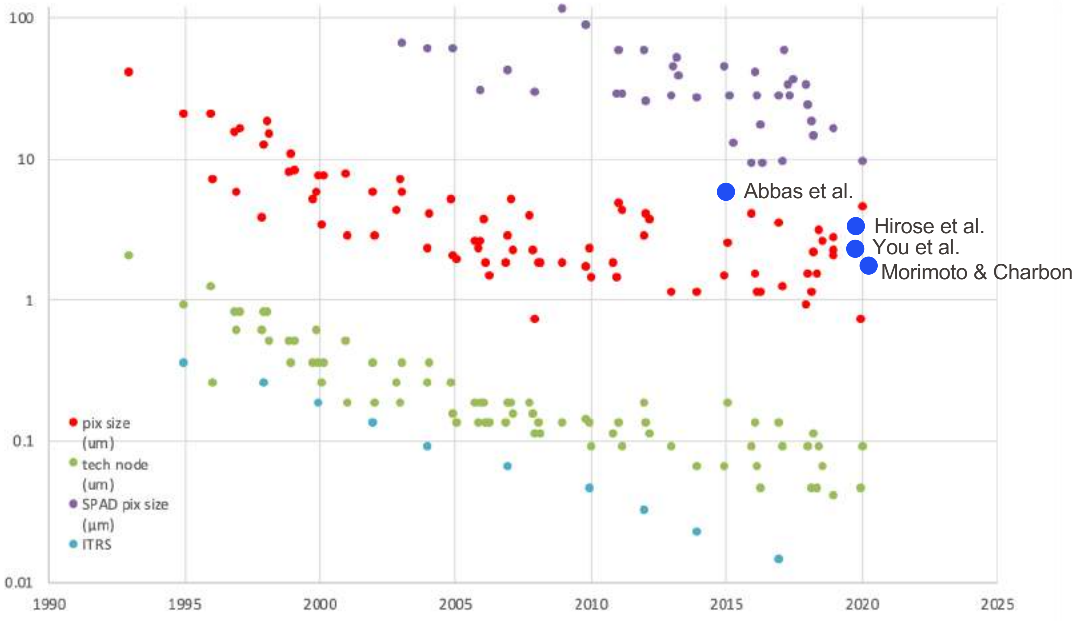


C. Veerappan & E. Charbon, TED(63) 2016

1µm-Pixels

	Abbas, IEDM'16	Henderson, IEDM'10	Abbas, IISW'17	Morimoto & Charbon OPEX'20		
Process technology	65/40nm 3D-BSI CMOS	90nm CMOS	130nm CIS	180nm CMOS		
Pixel pitch (µm)	7.83	5	3	2.2	3	4
Active diameter (µm)	-	2	1	1.2	2	3
Drawn fill factor (%)	45	12.5	14**	19.5*	32.3*	42.4*
Sensor resolution	128×120	3×3	4×4	4×4	4×4	4×4
Breakdown voltage (V)	12	10.3	15.8	32.35	23.6	22.1
Max. PDP (%)	27.5 (V_{ex}=3V)	36 (V_{ex}=0.6V)	15 (V_{ex}=3.2V)	10.3 (V_{ex}=4V)	17.3 (V_{ex}=6V)	33.5 (V_{ex}=6V)
Max. PDE (%)	12.4 (V_{ex}=3V)	4.5 (V_{ex}=0.6V)	2.1 (V_{ex}=3.2V)	2.0 (V_{ex}=4V)	5.6 (V_{ex}=6V)	14.2 (V_{ex}=6V)
Median DCR (cps)	11,000 (V_{ex}=3V)	250 (V_{ex}=0.6V)	150 (V_{ex}=1V)	751 (V_{ex}=4V)	1.6 (V_{ex}=6V)	2.5 (V_{ex}=6V)
Crosstalk (%)	-	<0.1 (V_{ex}=0.6V)	0.13-0.22 (V_{ex}=1V)	2.97 (V_{ex}=4V)	2.75 (V_{ex}=6V)	3.57 (V_{ex}=6V)
Afterpulsing probability (%)	-	-	0.18 (V_{ex}=1V)	<0.20 (V_{ex}=4V)	0.20 (V_{ex}=6V)	0.21 (V_{ex}=6V)
Timing jitter (ps)	136 (V_{ex}=3V)	107 (V_{ex}=0.6V)	107 (V_{ex}=3V)	72 (V_{ex}=4V)	70 (V_{ex}=6V)	88 (V_{ex}=6V)

The Race is On!



Take-home messages

- Large-format image sensors based on SPADs are an interesting trend with many interesting applications
- 3D-stacking could multiply the impact of these detectors with parallelism and machine learning in the forefront
- Work will focus on power reduction and miniaturization

- From ISSW 2020 (paraphrasing)
  - Histograms, histograms, histograms, Sara Pellegrini
  - Always start from the system, David Stoppa
  - Manage data before going big, Richard Walker
  - The 4 misconceptions about FLASH LiDAR, Hod Finkelstein
  - If you can, go digital, Daniel Van Blerkom

Acknowledgements

aqualab
http://aqua.epfl.ch

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