# BSI SPAD ARRAYS BASED ON WAFERBOND TECHNOLOGY

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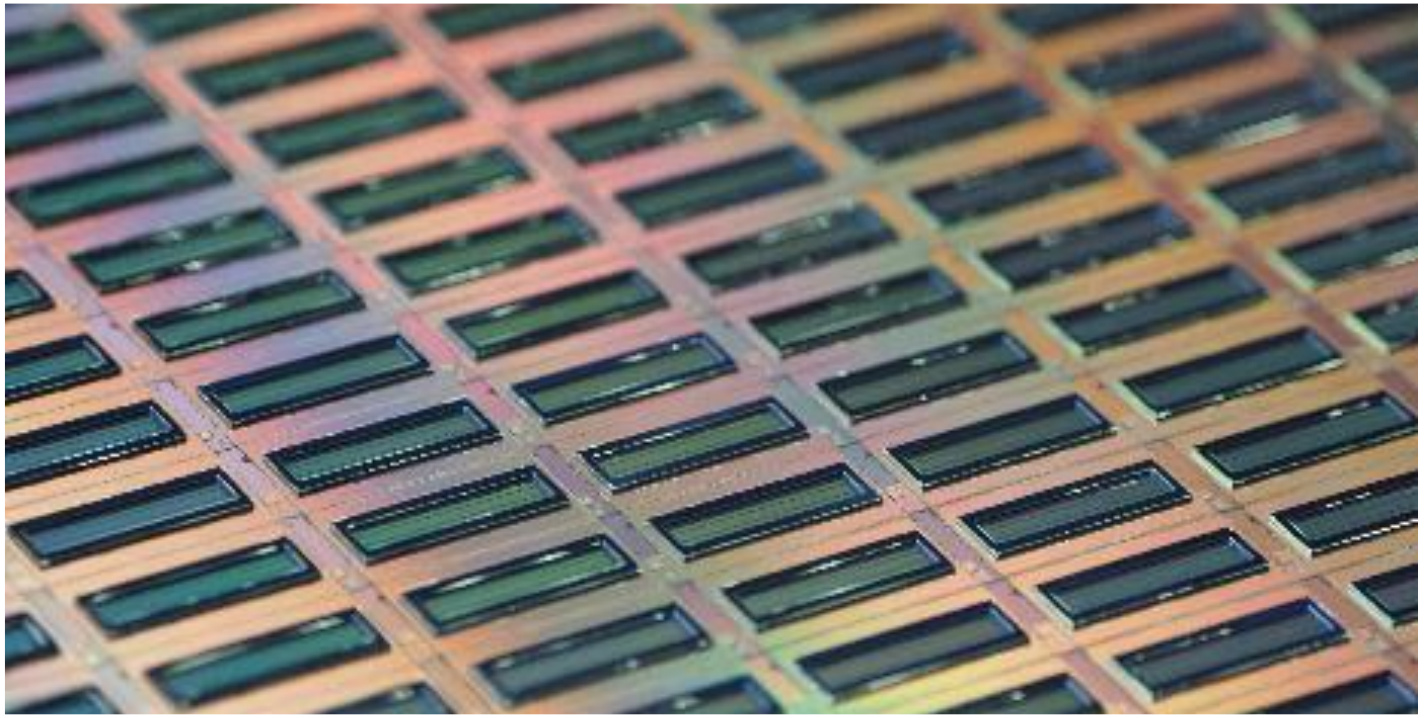




International SPAD Sensor Workshop ISSW2020, Edinburgh, June 8th, 2020

# OUTLINE

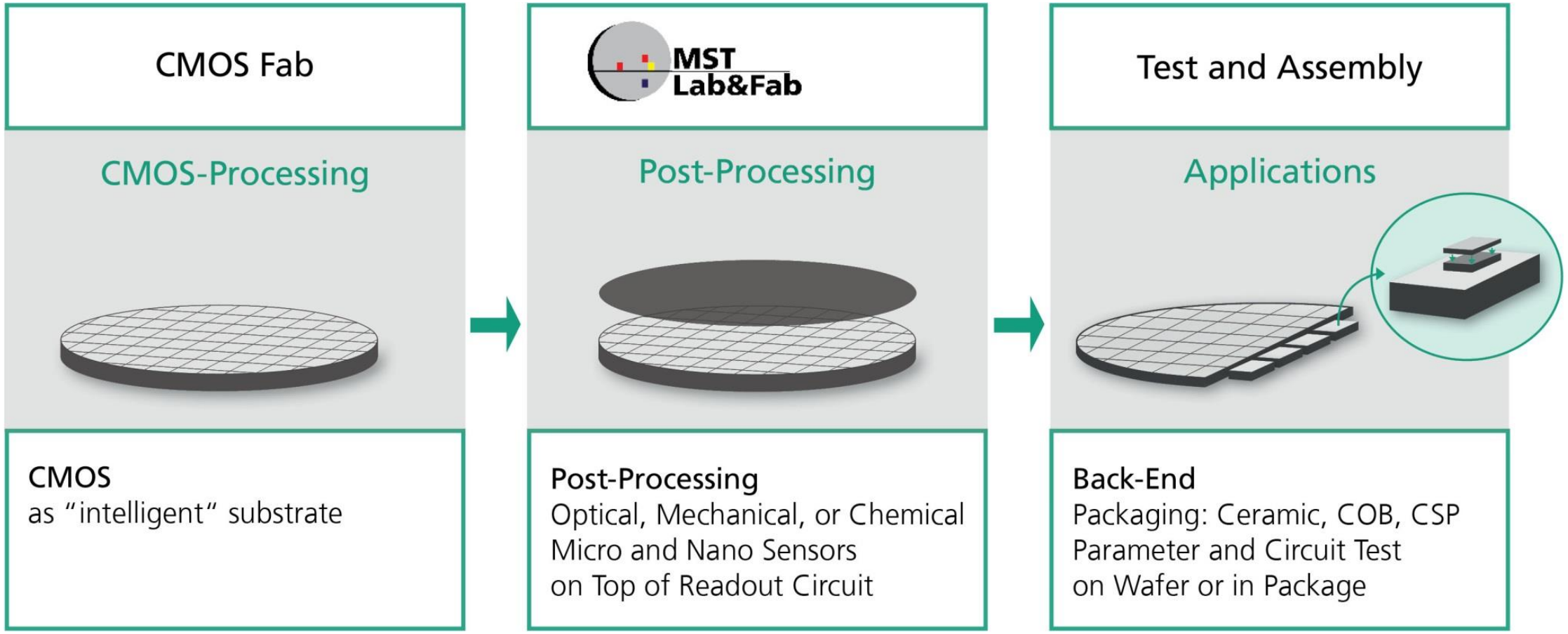
- Introduction to Fraunhofer IMS
- LiDAR application principles
- Wafer bonding and BSI
- Design example CSPAD3000
- Outlook

# Fraunhofer Institute for Microelectronics Circuits and Systems

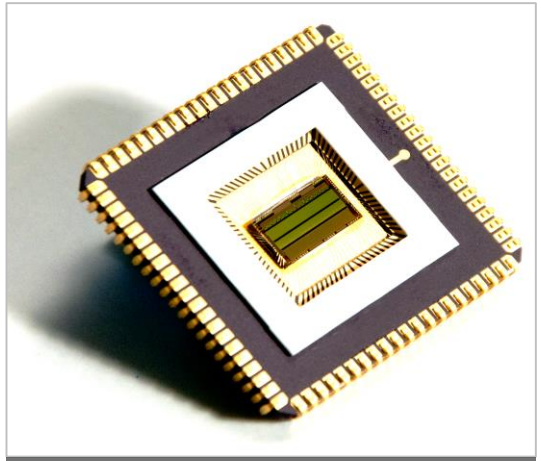
## Facts and Figures

- **Founded**
  1984/85
- **Employees**
  more than 250
- **Infrastructure**
  - Cleanrooms
  - inHaus-Center
- **Budget**
  33 million EUR in 2019
  - 25 % basic funding for corporate research and administration
  - 25 % publicity funded projects
  - 50 % projects funded by industry

# Fraunhofer IMS
## Infrastructure

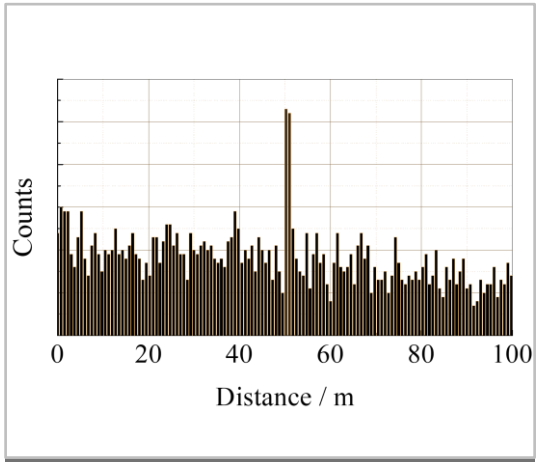


# Overview LiDAR topics @ Fraunhofer IMS



Chip design & fabrication

CSPAD, SiPM, ROIC
Qualification
Fabrication

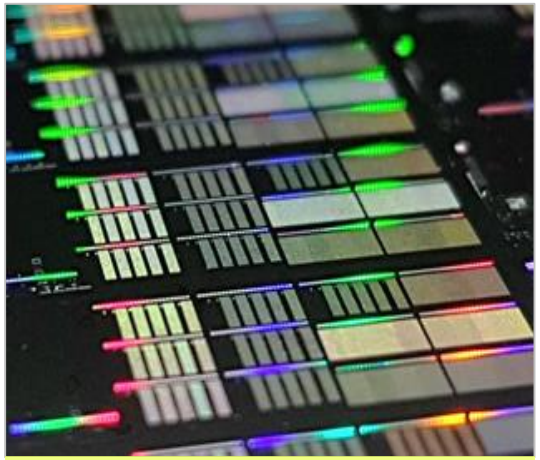



Signal processing

Photon coincidence circuits
Algorithms & filtering
Neuromorphic networks

System design

Camera demonstrators
System simulations



3D Integration

Wafer-to-Wafer and
Chip-to-wafer bonding
for backside illuminated
sensors (BSI)

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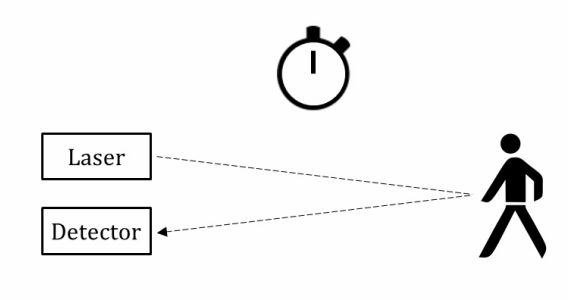
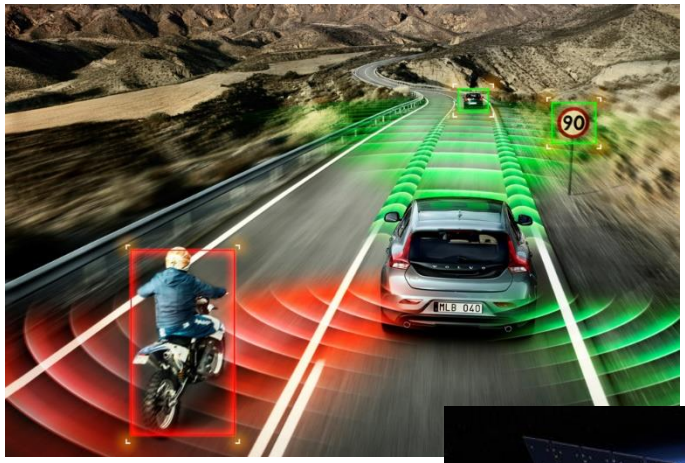
# LiDAR
## Light Detection and Ranging

- Distance measurement with photons



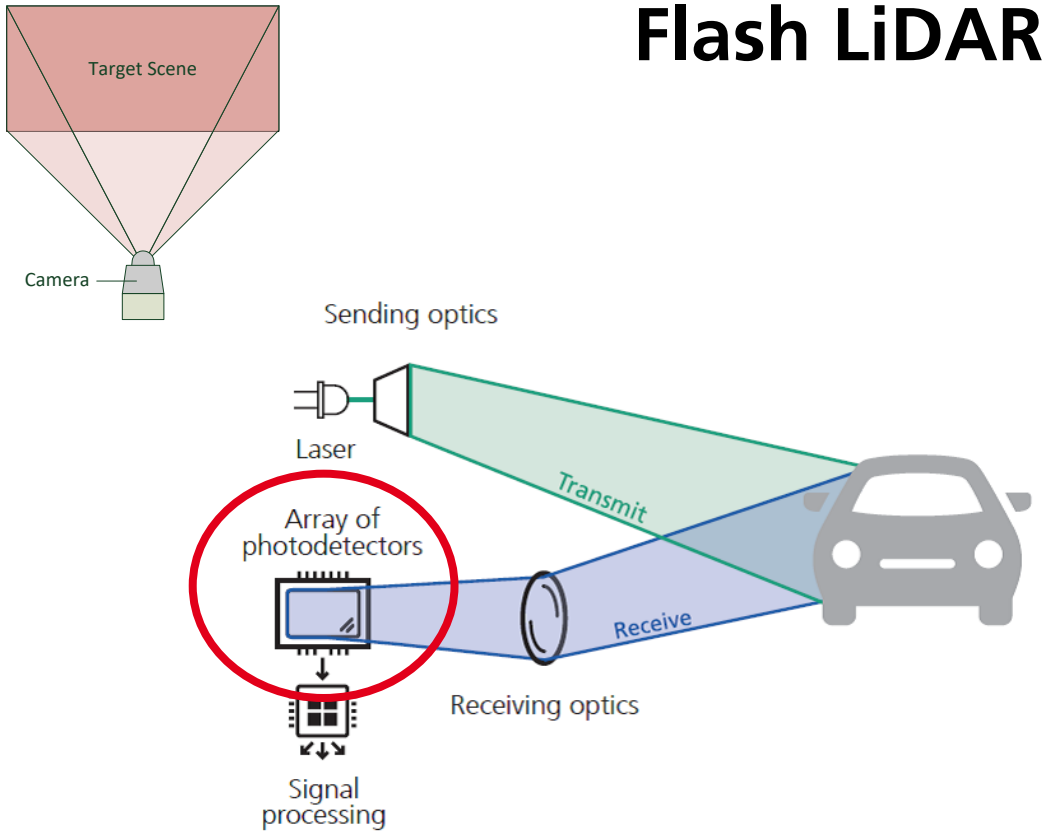

- Stop time after photon arrival: $T_{TOF}$ (ToF = Time-of-Flight)
- Direct Time-of-Flight

- Trend towards solid-state LiDAR

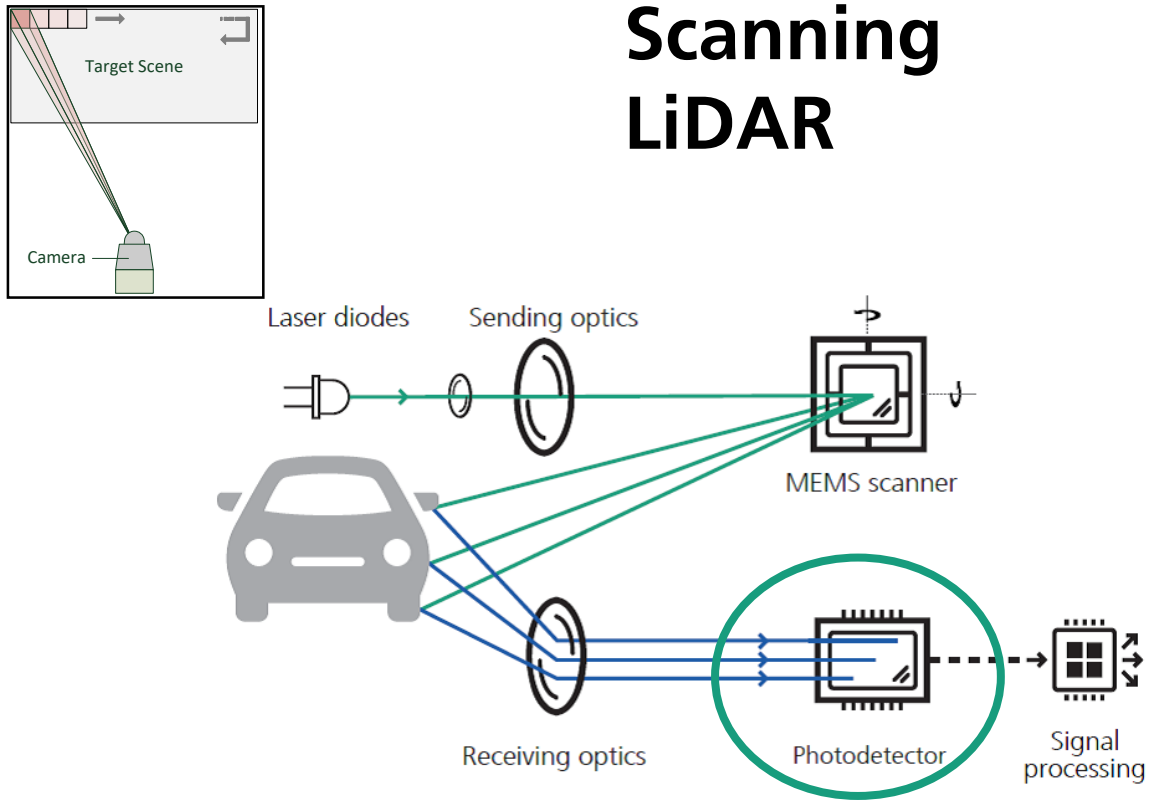
- *Autonomous driving*
- *Satellite rendezvous*
- *Industrial applications*

# Solid-state LiDAR – illumination method

## Flash LiDAR

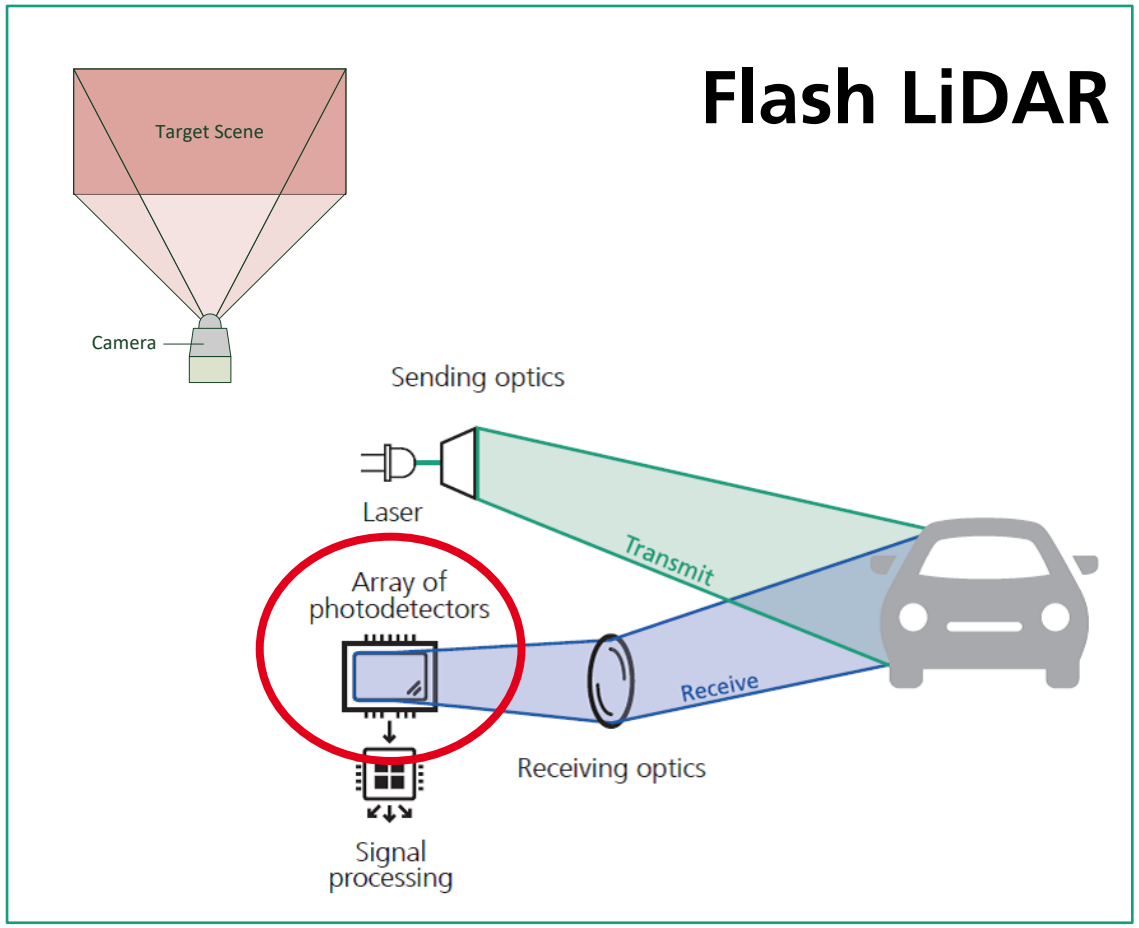



## Scanning LiDAR




source: Forschungsfabrik Mikroelektronik Deutschland

# Requirements for LiDAR photo detectors




**Highest demand in Flash LiDAR:**

- **High 2D pixel count** for high spatial resolution

**AND**

- Fast acquisition in kHz to MHz
  - **Timing information in µs per flash**

- **High resolution 2D arrays**
  - Long measurement range
  - Low power consumption
  - Co-integrated electronics
  - Cost-effective impementation

# Example: Detectors for Flash LiDAR
## Photodiode benchmark

- Best choice for Flash LiDAR: **Single Photon Avalanche Diodes (SPAD)**

**Silicon-based detectors**

| | PIN-PD | APD | SiPM | SPAD |
|---|---|---|---|---|
| Gain | 1 | $10^3$ | $10^6$ | $10^6$ |
| Single photon detection | No | No | Yes | Yes |
| Operational Bias | Low | Medium | Medium | Medium |
| Temperature Sensitivity | Low | High | Low | Low |
| Array possible | Limited | Limited | Limited | Yes |
| Readout / Electronics | Complex | Complex | Medium | Simple |
| Rise time | Medium | Slow | Fast | Fast |

source: Forschungsfabrik Mikroelektronik Deutschland

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- **Wafer bonding and BSI**
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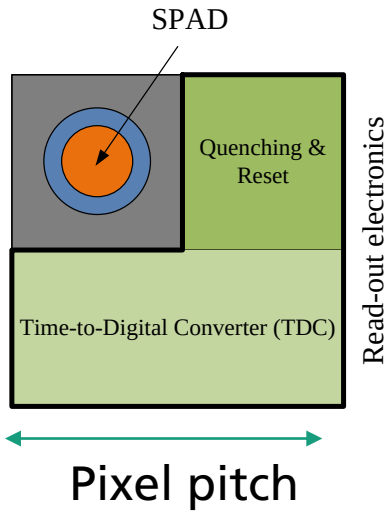
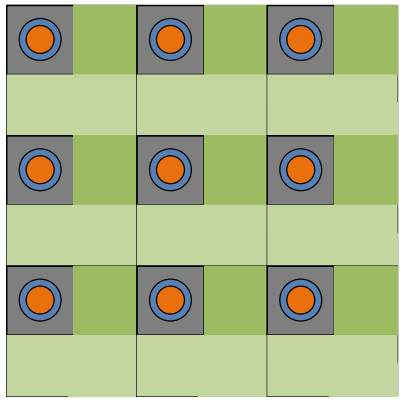
# Trade off: pixel pitch & in-pixel electronics

## Current status

- **CMOS SPAD with merging all parts in one wafer**



**Limiting pixel resolution due to pixel pitches up to 100 µm**

Dominating parameters for the pixel size

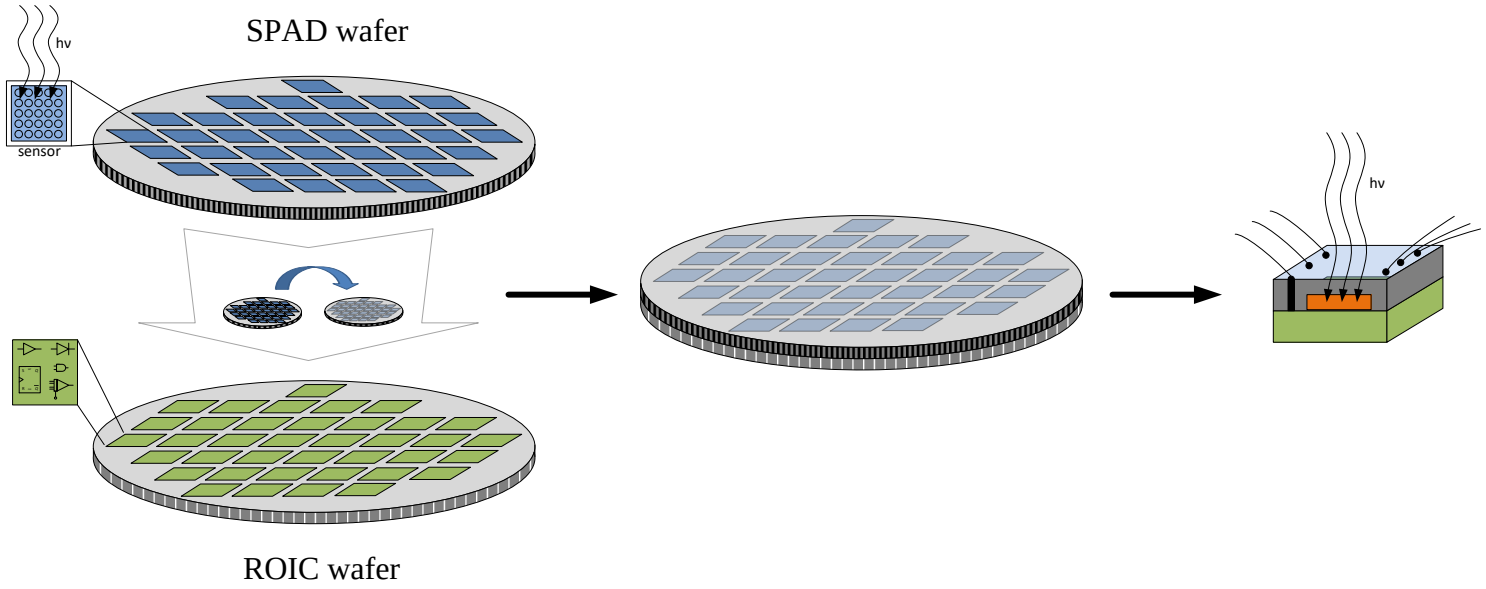
- TDC resolution
- SPAD size, including fill factor, crosstalk probability,…

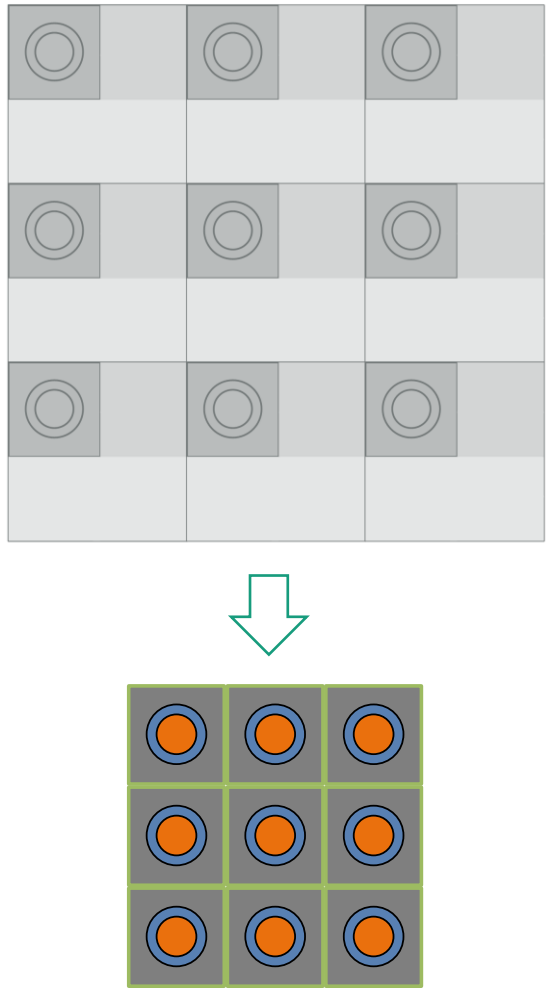
- Approach 1: Smaller CMOS technology node
  - Disadvantages: SPAD performance (e.g. spectral sensitivity) limited by CMOS process & high (initial) costs (masks, wafers)

- Approach 2: 3D-Integration of SPAD & CMOS

# 3D-Integration of SPAD & CMOS

## 3D stacking with 200 mm wafer-to-wafer bonding

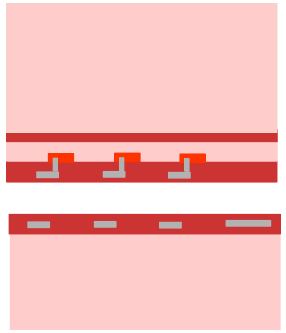


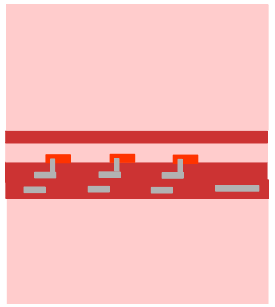
- 3D-Integration of SPADs and CMOS ROIC
  - allows effectivley lowering the pixel pitch
  - ..... and cost per pixel

# 3D-Integration of SPAD & CMOS

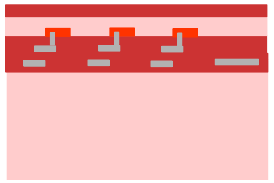
## Wafer-to-Wafer BSI process at IMS



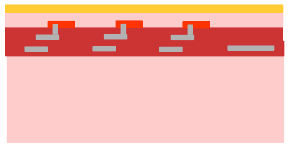
CMP-prepared surfaces



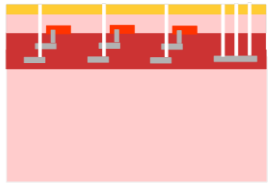
Oxide-oxide-bonding



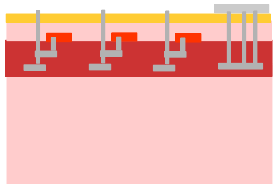
Grinding and etching



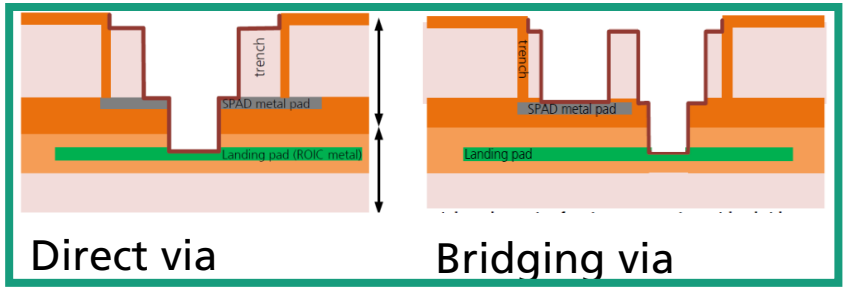
Box removal ARC deposition



TSµV etch (simplified)

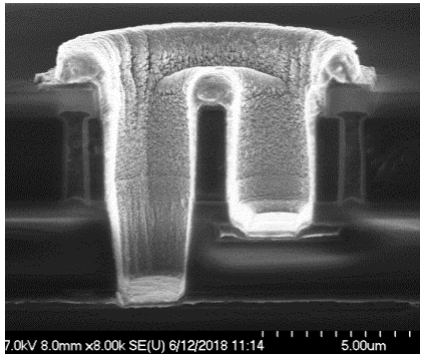


TSµV and pad metal deposition




Direct via Bridging via

- SOI base wafer is used for SPADs
- Wafer-to-wafer direct bonding
- Etch stop on buried oxide (BOX)
- ALD via metal (direct or bridging via)
- Backside passivation

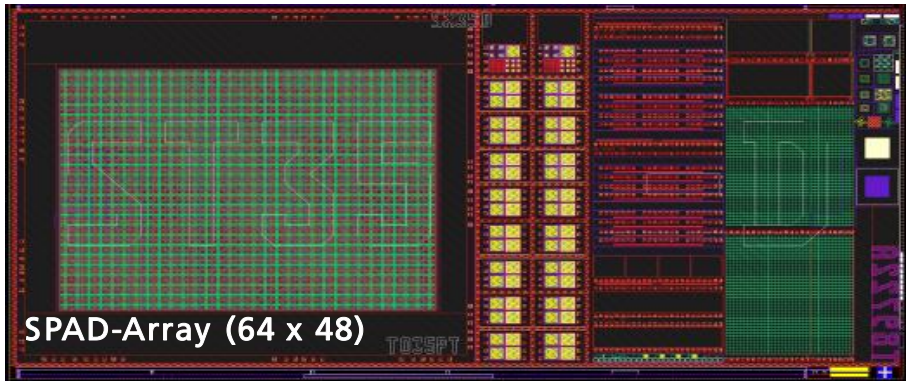


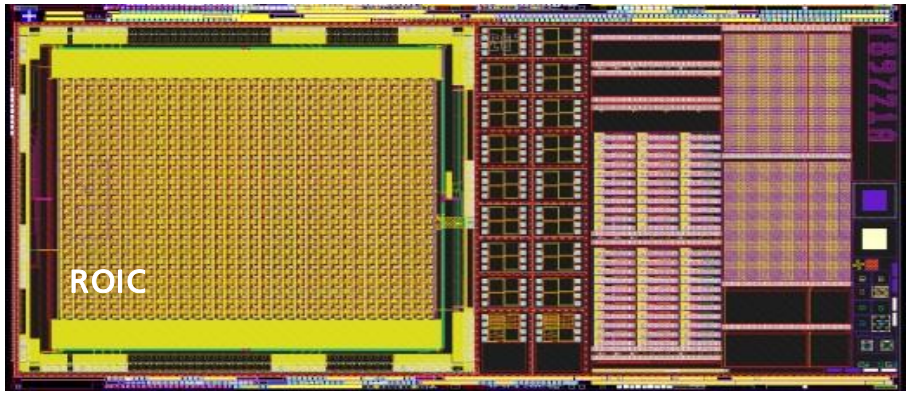
# OUTLINE

- Introduction to Fraunhofer IMS
- LiDAR application principles
- SPAD based LiDAR detectors
- Wafer bonding and BSI
- **Design example CSPAD3000**
- Outlook

# 3D-stacked 64x48 2D-CSPAD array

## CSPAD3000




CSPAD: SPAD with integrated CMOS

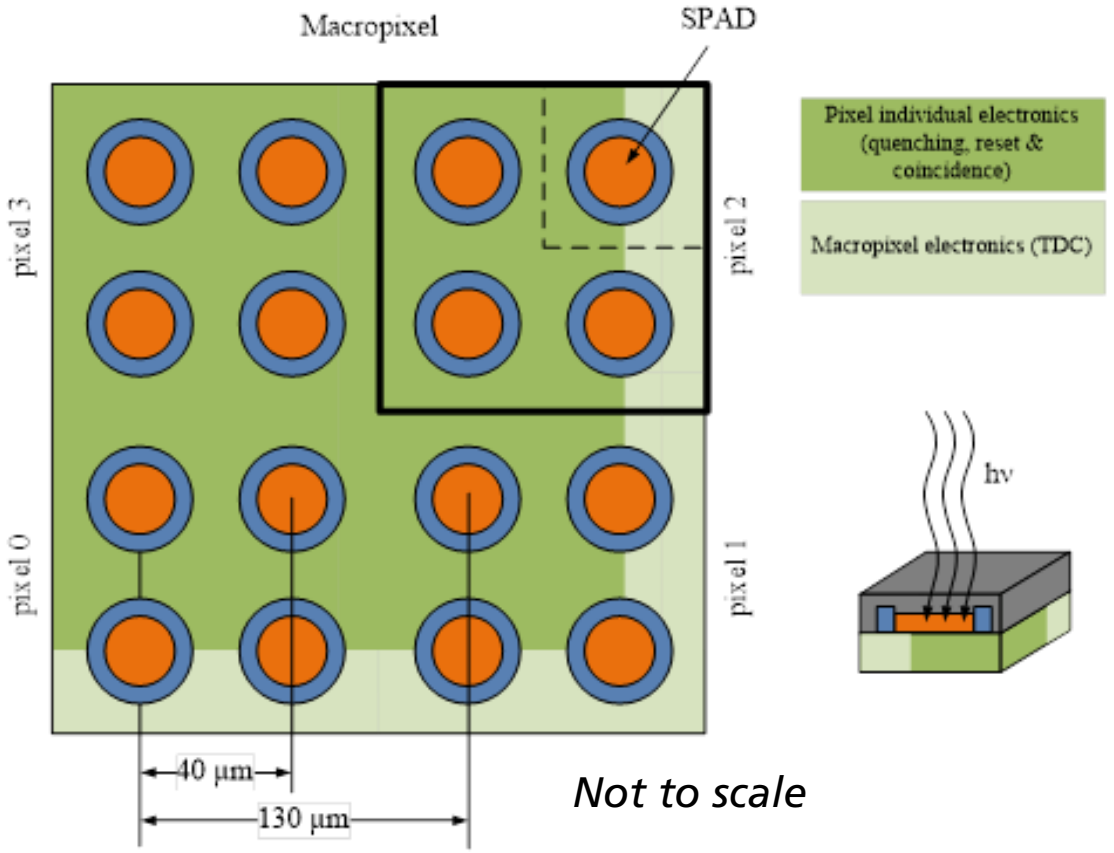
- **64 x 48** pixel resolution
- SPAD & ROIC in in-house **350 nm CMOS**
- **Back Side Illuminated** (BSI) SPAD sensor
- Chip size 10.25 x 10.19 mm²
- Operating in counting & timing modes
- **Adaptive coincidence** (IMS algorithm) for sunlight suppression

# 3D-stacked 64x48 2D-CSPAD array

## Macro pixel

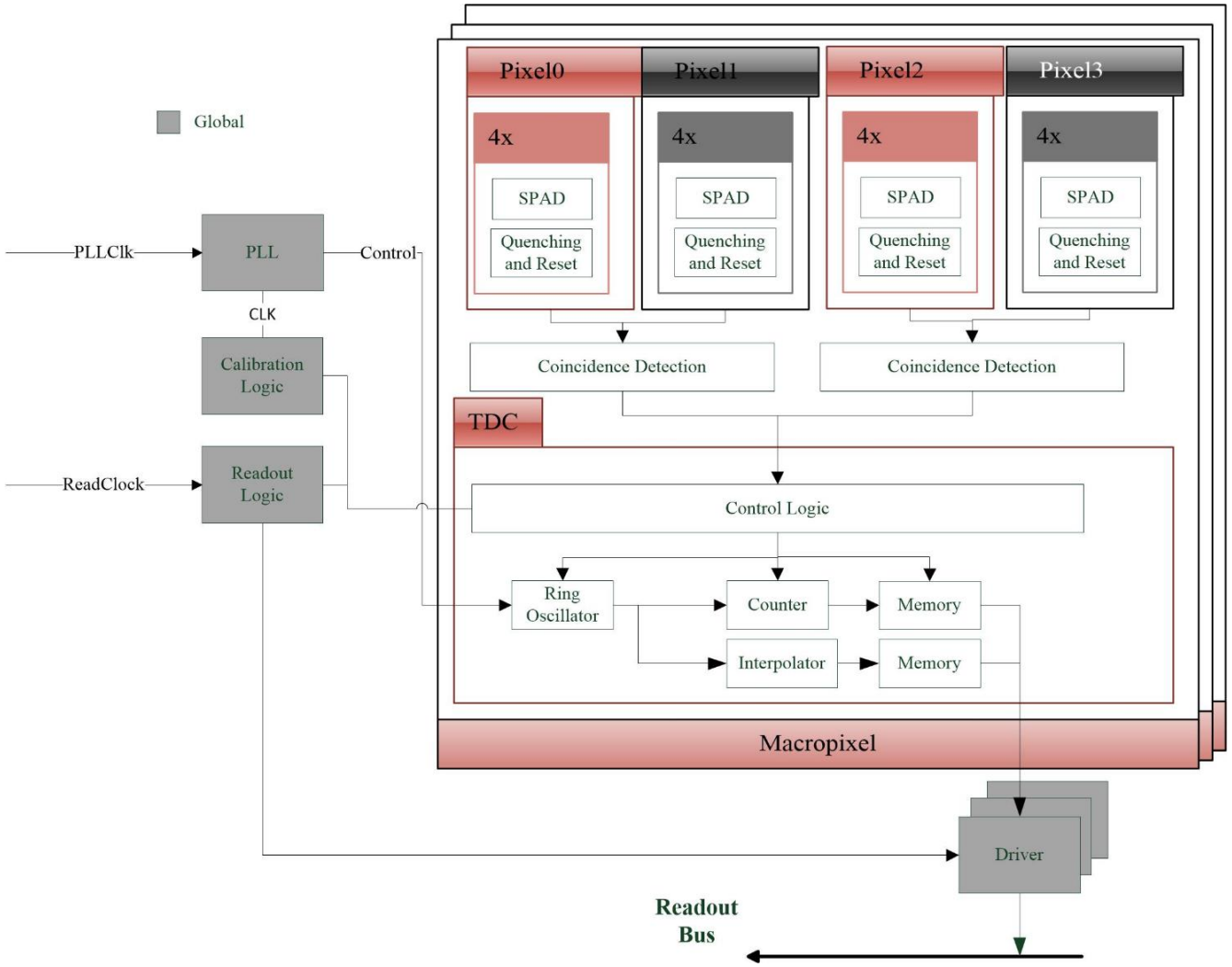
- Pixel pitch of 130 µm
- SPAD size of 40 µm

- Adaptive coincidence circuit for sunlight surpression
  - 4 SPADs in each pixel



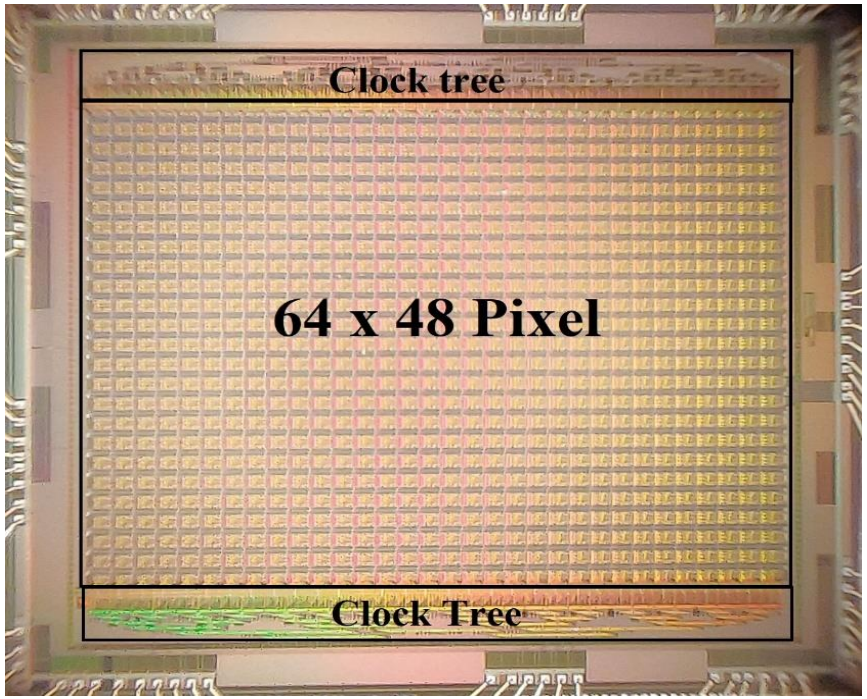
# Building block
## Read-out electronics

- In-pixel and global electronics
  - Red pixels: First laser illumination
  - Grey pixels:  Second laser illumination
- Read-out speed 20 MHz
  - Sensor read-out 26 kHz
  - Frame rate 13 kHz



# 64 x 48 2D-CSPAD array

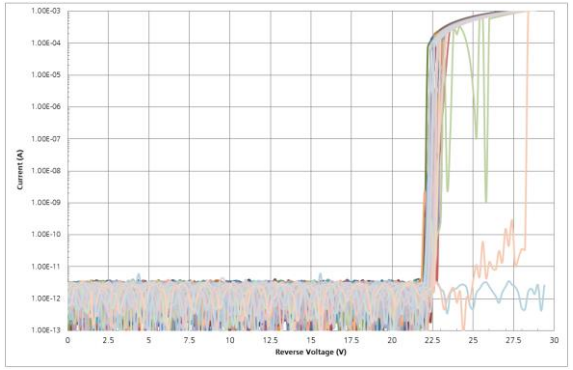
## Specifications

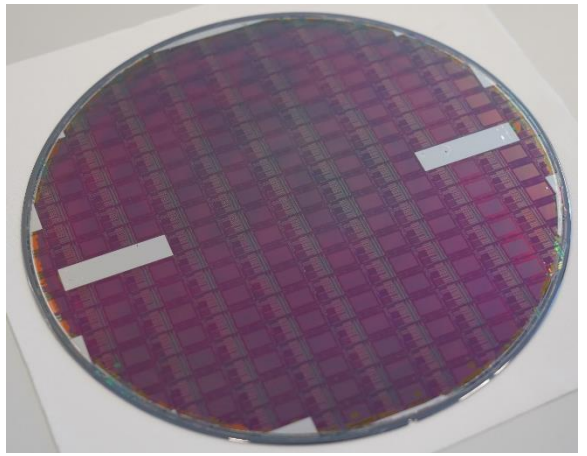


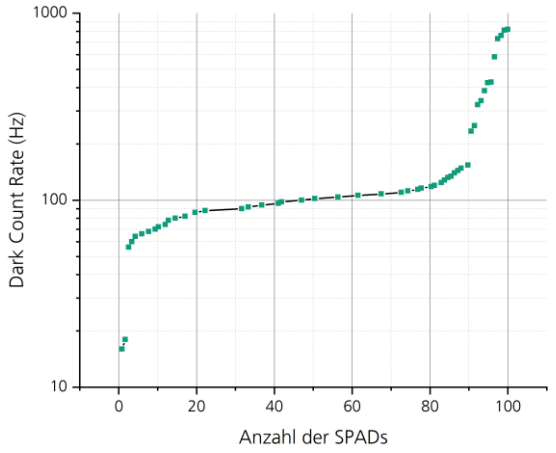

| | |
|---|---|
| Read-out concept | Interlaced flash |
| 3D integration details | Backside illuminated SPADs, Wafer-to-Wafer bonding |
| Wafer size | 200 mm |
| CMOS technology: SPAD / ROIC | Both in 0.35 µm CMOS |
| Pixel resolution | 64 x 48 |
| Pixel pitch | 130 µm |
| SPADs per pixel | 4 (for coincidence algorithm) |
| SPAD size | 40 µm x 40 µm |
| SPAD active area | 14 µm (diameter) |
| Fill factor | 3.6 % |
| Timing resolution | 312.5 ps |
| Features | Photon coincidence circuit, timing, and counting mode |
| Frame rate | 13 kHz |
| Number of IOs | 84 |
| Chip dimension | 10.25 x 10.19 mm² |

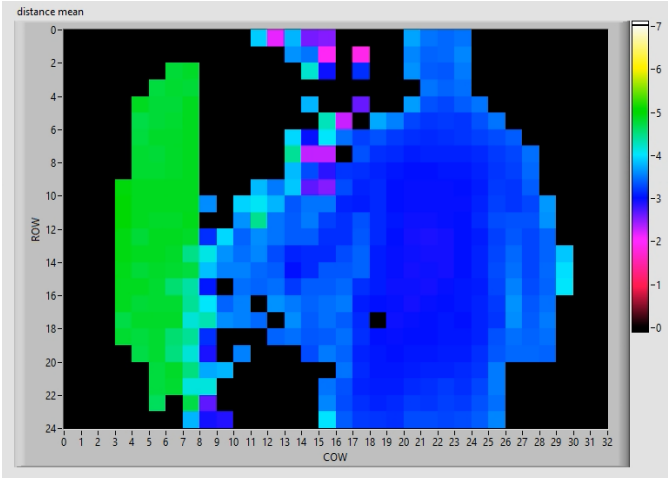
# CSPAD3000
## First results

- Break-through voltage ~ 22.5 V
- DCR ~100/SPAD ~0.65/µm²
- No open vias
- First ToF Images taken





# Outlook

## OPTIONS TO INCREASE PERFORMANCE

ROIC process technology 180 nm CMOS:

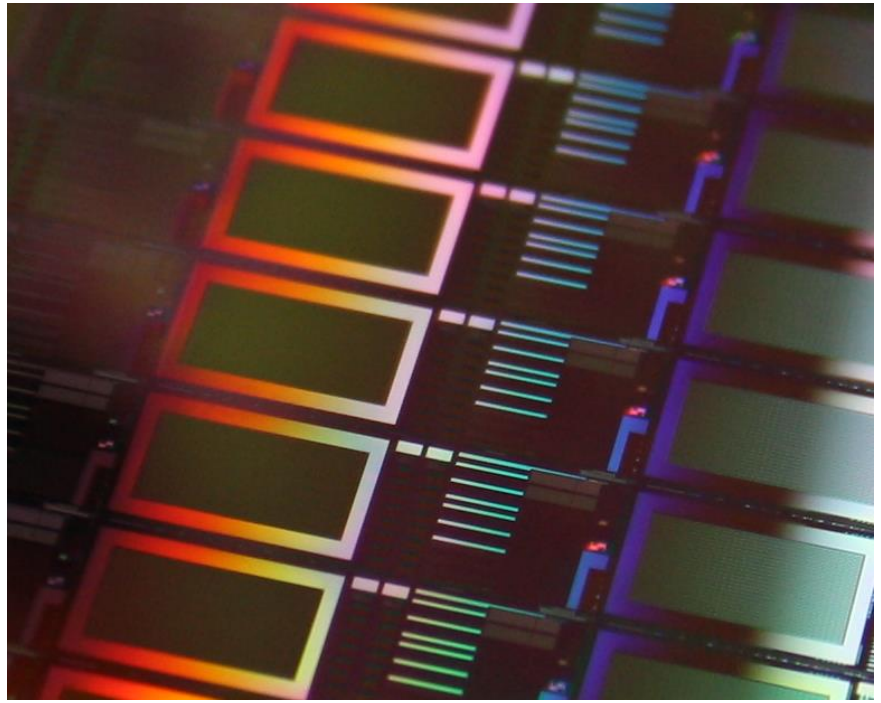
- **Additional factor of 4 in number of pixels**

NIR SPAD sensitivity using epi-wafer with optimized specs:

- **Increasing 905 nm Quantum Efficiency of SPAD to 25 %**

Wafer-level micro lenses

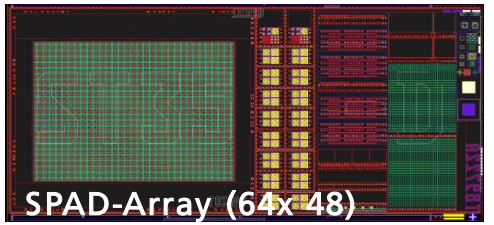
- **80 % fill factor  instead of 4 %**

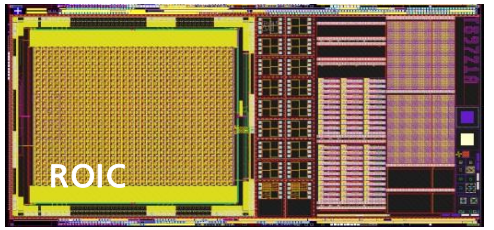


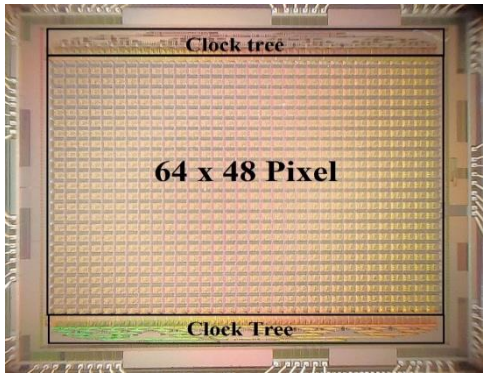
# Summary

- 3D-Integration approach âllows for high-resolution CSPAD-arrays
  - Decrease of pixel pitch by maintaining complex in-pixel electronics
- New interlaced-flash concept
  - Optimum combination of reduced pixel size and flash operation
- Presented 64 x 48 sensor design (CSPAD3000)
  - Sensor for LiDAR & low-light imaging applications

⇨ **3D-Integration allows future CSPAD arrays with dramatically better performance and cost**



# Thank you for your attention