

#### **ISSW2020**

#### "THE INTERNATIONAL SPAD SENSOR WORKSHOP"

June 8 – 10, 2020



#### CUSTOM SILICON TECHNOLOGIES FOR HIGH DETECTION EFFICIENCY SPAD ARRAYS

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## **OUR IDEA**

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#### **CMOS Technology**



CMOS steps for SPAD fabrication

- ✓ Smart Pixels / Complex Systems
- ✗ No SPAD optimization

#### **Custom Technology**



- ✓ SPAD optimization
- **K** External electronics





#### **Custom Technology**



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- External electronics

#### **Two Approaches for Si-SPAD**

#### **CMOS Technology**



# CMOS steps for SPAD fabrication Smart Pixels / Complex Systems

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#### **Two Approaches for Si-SPAD**

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#### **CMOS Technology**



# CMOS steps for SPAD fabrication Smart Pixels / Complex Systems No SPAD optimization

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- ✓ SPAD optimization
- **#** External electronics



## **APPLICATIONS**

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#### Collaboration with Weiss & Michalet group at UCLA



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#### Similar requirements in many other applications

- Quantum Key Distribution in free space
- Time Domain Diffuse Correlation Spectroscopy
- Super-Resolution Microscopy
- Quantum Information Processing

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#### Similar requirements in many other applications

- Quantum Key Distribution in free space
- Time Domain Diffuse Correlation Spectroscopy
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- Quantum Information Processing

#### Lack of SPADs that combine:

- High detection efficiency in the red / near infrared
- Low timing jitter
- Availability of arrays



# THIN SPAD IN CUSTOM TECHNOLOGY

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- Carriers generated in the substrate sometime trigger an avalanche
- Very slow diffusion tail in the temporal response

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Enrichment Shallow n Cathode n+ p+ p-٦ n+ Substrate  $\Rightarrow$ 

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Enrichment Shallow n Cathode n+ p+ pn+ √73 € Substrate  $\sim$ 

- Carriers generated in the substrate cannot trigger an avalanche
- Short diffusion tail in the temporal response

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Enrichment Shallow n Cathode n+ p+ p-Ъ n+ n+ Isolation n+ Substrate 

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Enrichment Shallow n Cathode Anode n+ p+ pn+ n+ Isolation n+ Substrate 1

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Enrichment Shallow n Cathode Anode n+ p+ p-٦ n+ n+ **Buried Layer** p+ Isolation n+ Substrate 3

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Enrichment Shallow n Cathode Anode n+p+ p-Ъ n+ p+ n+ p+ **Buried Layer** p+ Isolation Sinker n+ Substrate 3



## ENHANCING THE DETECTION EFFICIENCY

#### Increasing the Detection Efficiency



- Only the photons absorbed in the upper layer can be detected
- Limited PDE at longer wavelengths

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#### Increasing the Detection Efficiency



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- Thicker p- layer
- Not sufficient for good performance

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#### Extended Double Epitaxial SPAD



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#### **Extended Double Epitaxial SPAD**



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#### Engineered Extended Epitaxial SPAD



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#### Engineered Extended Epitaxial SPAD



#### Engineered Extended Epitaxial SPAD







#### **Thin SPAD**

- Overvoltage to optimize the performance
- Electric field increase: ΔE
- Vov= ΔE \* (t<sub>M</sub> + t<sub>D</sub>)





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#### **Thick SPAD**

- Same multiplication field wanted
- Same ΔE
- Larger Overvoltage: 20V

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# **NOT READY FOR ARRAYS**





## Lack of full electrical isolation

- Anodes shorted
- Lost flexibility for connecting electronic circuits

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## **Dielectric Isolation**

- Insulating layer between anodes
- It must reach the substrate
- Eliminates conductive paths between anodes





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## Fabrication: Planarization and Capping







- Influences avalanche current reading
- Negative impact on timing













## **Additional advantage**

Compactness (3µm-wide) → Denser arrays





## Additional advantage

Compactness (3µm-wide) → Denser arrays

## **Potential problem**

Stress introduced during fabrication → May increase Dark Count Rate



# **EXPERIMENTAL RESULTS**

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0.8 Thick SPAD **RE-SPAD** 0.7 Thin SPAD 0.6 Photon Detection Efficiency 0.5 **Longer Wavelengths** 0.4 Considerable improvement 40% @800nm 0.3 2.5x Improvement @800nm 0.2 0.1 0 400 500 600 700 800 900 1000 Wavelength (nm)

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### **Deep trenches have no effect on the Dark Count Rate**

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1 mm

## Designed for NIH funded project:

- Weiss / Michalet group at UCLA
- High-throughput Single Molecule Analysis

## Array geometry:

- 32 x 1 pixels
- Active diameter: 50 μm
- Pitch: 250 µm

Ceccarelli et al, IEEE PTL **30**(6), 557-560, (2018), doi:10.1109/LPT.2018.2804909

## **Compact Photon Counting Modules**

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#### **Features**

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- Temperature control
- Individual photon pulses available
- On board FPGA for basic processing
- High speed USB link

#### **Hermetically Sealed Chamber**

- Contains both SPADs and AQCs
- Dry atmosphere
- Cooling without moisture issues

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- Confirmed high Photon Detection Efficiency
- Good uniformity across the arrays

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# **NEXT DEVELOPMENTS**







- **Aim:** 3D atomic-scale movies of molecular machine in action
- Funding: Human Frontier Science Program (HFSP)





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## Questions

- How close we can get?
- What does limit the compactness?












### **Problems**

- Maximum bias voltage < 50V</li>
- Strong limitation for biasing with Vov ≈ 20V





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#### **Guard Rings** allow Bias Voltage > Edge Breakdown







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#### **Problems**

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- Complexity





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#### Must be removed



#### **Solution**

- Confine the charge layer to the active area
- Fabrication by high energy ion implantation

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## **3D INTEGRATION**







- Array size limited by wire bonding
- Max ≈ **100 pixels**



- Solves wire-bonding limitations
- Arrays size > 1000 pixels



Red-Enhanced SPAD technology:

- High detection efficiency (70% @ 600 nm) / Low timing jitter (90 ps FWHM)
- 32 x 1 array demonstrated
- Arrays with more pixels and more compact layout on the way

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- Cornell NanoScale Science & Technology Facility
- Human Frontier Science Program





# **HIGH REPETITION RATE**

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- Needed to quench the avalanche and to reset the bias
- Thin SPAD: dead time 6.2 ns → 160 Mcount/s
- Red Enhanced SPAD: dead time 12.5 ns → 85 Mcount/s



Acconcia et al, Optics Express **24**(16), 17819, (2016), doi:10.1364/OE.24.017819 Acconcia et al, Rev. Sci. Instr. **88**, 026103, (2017), doi:10.1063/1.4975598 Ceccarelli et al, IEEE PTL **30**(4), 391-394 (2018), doi:10.1109/LPT.2018.2792781

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