A BSI Global Shutter Pixel with Background Light Suppression for Multi-Frame Differential Imaging

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***Abstract* — A BSI compatible global shutter pixel with the feature of background light suppression has been developed for differential imaging applications. The proposed pixel scheme features in-pixel consecutive multiple frame subtraction and accumulation. This yields a good immunity to background light, thus enhancing the contrast and detection probability for differential images while eliminating the need for off-chip data buffer or storage. In this paper, the signal behavior and noise performance have also been analyzed with an extracted pixel model. The calculated SNR shows an increasing tendency with the use of the proposed in-pixel computing scheme.**

I. Introduction

This paper presents a BSI compatible global shutter pixel architecture for differential imaging applications, such as structured-light 3D surface imaging [1,2] and object tracking (e.g. eye tracking) [3]. In contrast with conventional CIS global shutter pixels [4,5] or differential imager pixels [6,7], the proposed architecture features in-pixel consecutive multiple frame arithmetic, i.e. subtraction and accumulation to improve the tolerance to background light, thus enhancing the contrast and detection probability [8] for differential images while relaxing the need for data-retention.

II. Operating Principle and Pixel Implementation

Fig. 1 conceptually illustrates the differential pixel operation together with a structured light illuminator. With the aid of the embedded subtraction function, two image signals, obtained with and without projected light, are differentiated and stored in the same pixel matrix. To increase the SNR and improve the tolerance of background light, multiple (*#n*) images are processed at the pixel-level in the same sequence and consecutively accumulated, the result of which is then readout at the end of each frame.

The schematic of the differential pixel is shown in Fig. 2. It adopts a fully differential switched-capacitor integrator as the pixel-level readout circuit, along with a single-ended source follower as output stage. During the exposure phase (Fig. 5), a laser source is controlled in synchronization with the imager. When the laser is active, the laser signal charge Q_{ON} is accumulated on PPD and converted to a voltage V_{ON} that is stored on C_{FD_ON} + C_{DIFF} (Fig. 3(a)). When the laser is off, the background signal Q_{OFF} is generated and transferred on C_{FD_OFF} + C_{DIFF} as V_{OFF} (Fig. 3(b)). Based on this bidirectional charge-transfer scheme, the voltage $\Delta V_{DIFF}(1)$ stored on C_{DIFF} can be derived as:

$$\Delta V_{DIFF}(1) = \left(\frac{a_{ON} Q_{ON}}{C_{FD\_ON} + C_{DIFF}} - \frac{Q_{OFF}}{C_{FD\_OFF} + C_{DIFF}} \right) \times a_{OFF} \quad (1)$$

where $\alpha_{ON} = \frac{C_{DIFF}}{C_{DIFF} + C_{FD\_ON}}$ and $\alpha_{OFF} = \frac{C_{DIFF}}{C_{DIFF} + C_{FD\_OFF}}$.

With the aid of this in-pixel differential operation, the parasitic photocurrents at the two floating diffusion nodes is also subtracted. The succeeding acquisition cycles follow the same sequence afterwards. As such, *#n* acquired differential signals are consecutively accumulated on C_{DIFF}.

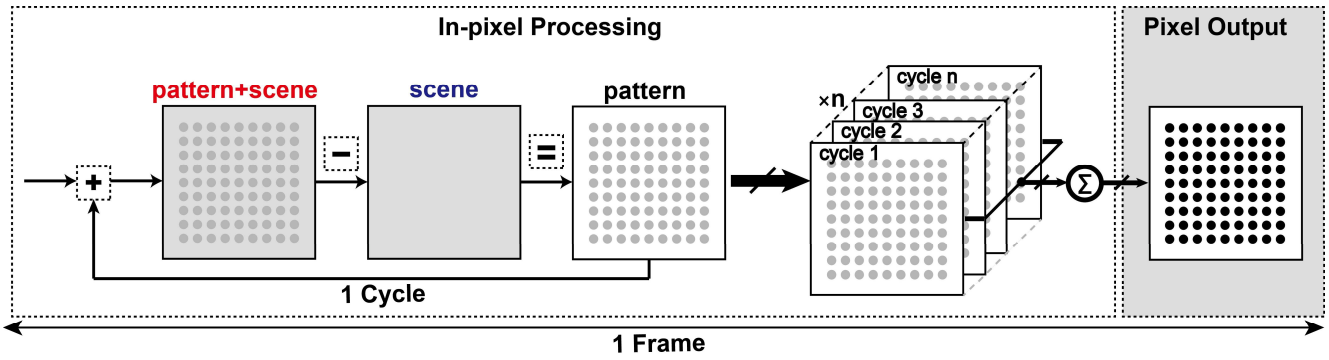


Fig. 1 Concept of a differential global shutter pixel operating together with a structured light illuminator.

During the readout phase, together with the on-state reset transistor RST_{ON}, the transfer gate TG_{OFF} can be biased at a mid-level state, acting as an anti-blooming drain to remove the excess charges. Meanwhile, the charge accumulated on C_{FD_ON} is readout with delta double sampling mode.

The proposed pixel is developed based on a BSI process. As the signal is kept at the FD node during readout phase, the stored signal will be deteriorated by the leakage and diffused photo-carriers caused by the parasitic light. To address this issue, dedicated process, pixel layout and readout strategy are being explored. Special care is taken to minimize C_{FD_ON} and C_{FD_OFF} as well as to optimize their matching. By applying a MIM cap on top of a PPD, a photodiode with 66% of the pixel area is achieved in a 2.8 μm pixel pitch.

III. Differential Signal Behavior and Noise Analysis

Eq. (1) in Section II presents the differential signal $\Delta V_{DIFF}(1)$ when $n = 1$. For the case of $n > 1$, the storage signal $\Delta V_{DIFF}(n)$ can be derived as:

$$\Delta V_{DIFF}(n) = \frac{\alpha_{ON} \times (\alpha_{ON} Q_{ON} - Q_{OFF})}{C_{DIFF} + C_{FD\_OFF}} \sum_{n=1}^{cycle} (\alpha_{ON} \alpha_{OFF})^{n-1} \qquad (2)$$

where $\sum_{n=1}^{cycle} (\alpha_{ON} \alpha_{OFF})^{n-1}$ is the overall attenuation factor for charge transfer and charge distribution within n cycles. This calculation result reveals that the differential signal add-up rate is a non-linear function of n and Fig. 5 confirms that $\Delta V_{DIFF}(n)$ increases with n at an ever decreasing rate.

The noise performance of the proposed pixel architecture has been analyzed with the extracted noise model based on the pixel layout (The noise calculation are excluding the attenuation factor). The temporal noise of the proposed differential pixel is dominated by the kTC noise and the photon shot noise. The magnitude of the kTC noise per cycle is determined by the size of C_{DIFF} as well as the two parasitic capacitors C_{FD_ON} and C_{FD_OFF}.

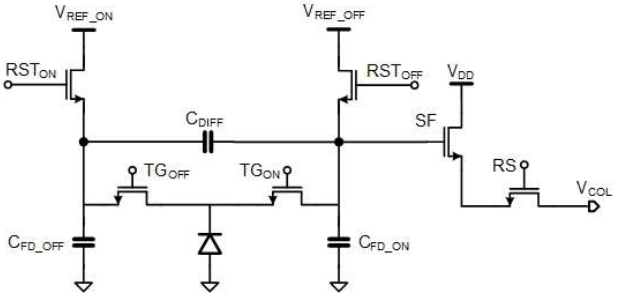


Fig. 2 Differential global shutter pixel schematic

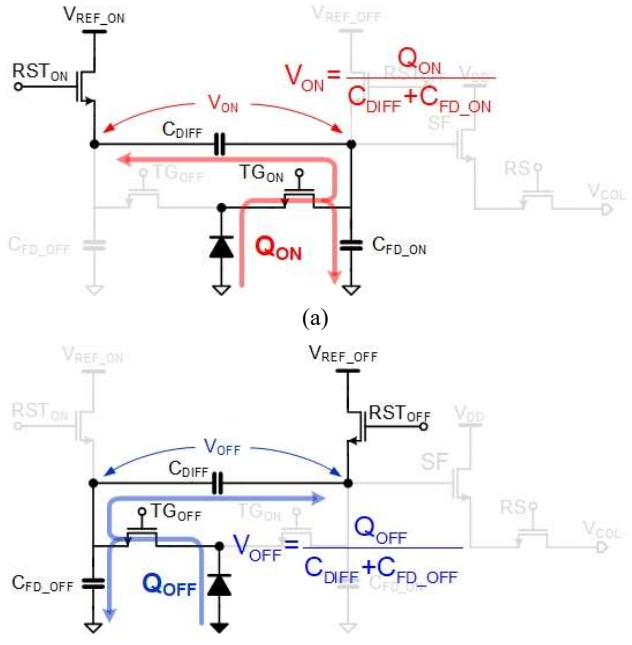


Fig. 3 Block diagram of pixel operation (a) Integration laser signal. (b) Integration background signal.

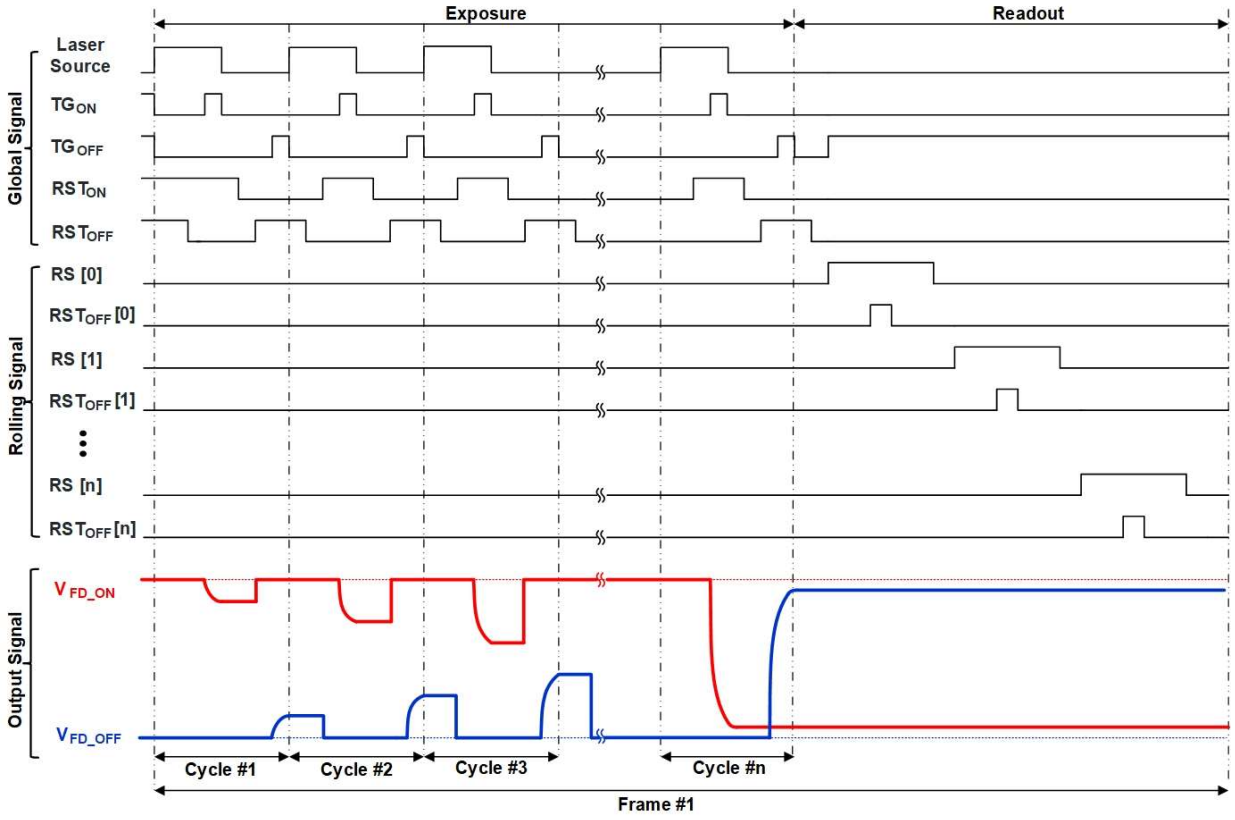


Fig. 4 Differential global shutter pixel timing diagram.

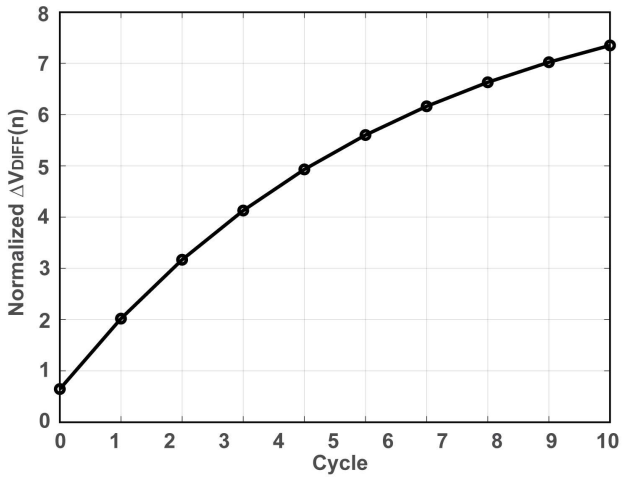


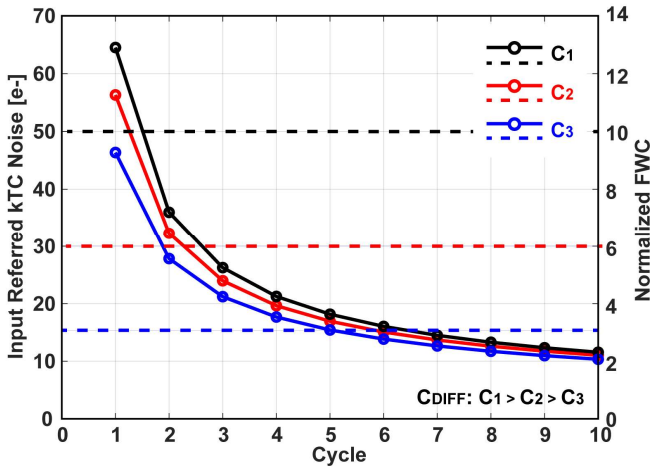
Fig. 5 Calculated normalized differential voltage on C_{DIFF} of differential global shutter pixel.

Fig. 6(a) shows the calculated equivalent input-referred readout noise σ_{RN}^2 as a function of n with different C_{DIFF} values. As shown in this figure, kTC noise in the electron domain is reduced as C_{DIFF} decreases, along with the scaling down of FWC at C_{DIFF}.

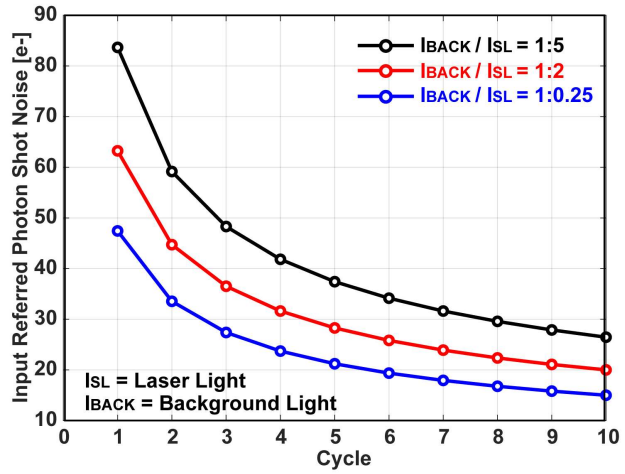
The photon shot noise, which is originated from a natural process, is typically unnoticeable in a normal image. However, after one frame differentiation of two equal images, this noise would become visible. Fig. 6(b) presents the simulated equivalent input-referred photon shot noise in three scenarios with different laser light levels based on the system prerequisite. As the laser light becomes stronger, the photon shot noise increases hand in hand. As the photon shot noise in two images is non-correlated, thus the process of subtraction leads to a degradation of the SNR. However, if multi-frame image acquisition approach is applied, this issue would be relieved. With the cycle number n, the SNR can be expressed as:

$$SNR = \frac{(Q_{ON} - Q_{OFF}) \times \sqrt{n}}{\sqrt{Q_{ON} + Q_{OFF} + \sigma_{RN}^2}} \quad (3)$$

Eq. (3) indicates that the SNR is not only determined by the captured electrons and noise floor, but is also increased proportionally to the square root of n, whose noise reduction principle is similar to the theory of CMS technique [9]. Fig. 7 shows the SNR as a function of n with the proposed in-pixel arithmetic scheme. It clearly shows an increasing tendency of the SNR when n increases.



(a)



(b)

Fig. 6 (a) Calculated equivalent input-referred readout noise and normalized FWC of C_{DIFF}. (b) Calculated equivalent input-referred photon-shot noise of differential global shutter pixel.

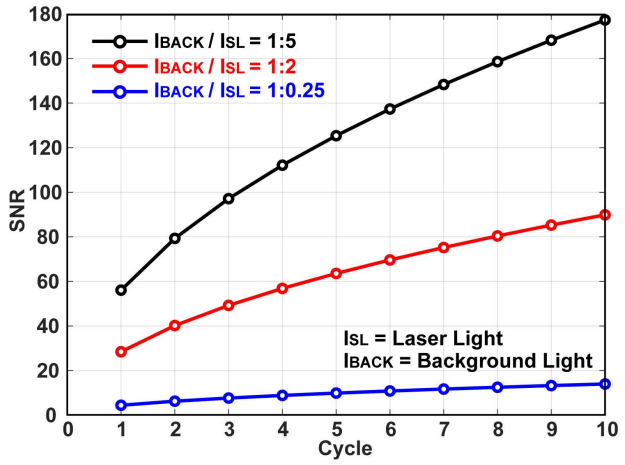


Fig. 7 Calculated normalized SNR of differential global shutter pixel.

IV. Progress and Conclusion

This paper presents a BSI compatible global shutter pixel for differential imaging applications. The proposed pixel scheme features in-pixel consecutive multiple frame subtraction and accumulation. Given the advantages described in this article, the proposed pixel stands out as the architecture choice for structured-light 3D surface imaging and object tracking, especially in outdoor environments. To demonstrate the performance of the proposed pixel structure, we developed a pixel-only test chip in a BSI CIS process. At the date of this article submission, the test chip with BSI version is under fabrication.

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