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A Time-Resolved Lock-in Pixel Image Sensor Using Multiple-Tapped Diode and Hybrid Cascade Charge Transfer Structures

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I. Introduction

Time-resolved multiple-tap lock-in pixel image sensors are expected to be used for various attractive applications including time-of-flight (TOF) range imaging and time-resolved biomedical imaging. Their pixels for future applications are required to meet (a) sub-nanosecond photo-carrier response, (b) high effective quantum efficiency or high sensitivity and (c) larger number of signal-taps. Structures for CIS (CMOS image sensor)-compatible lock-in pixels reported to date include pixels with photogate-based [1]-[5], pinned-photodiode with MOS-transfer gates [6][7], pinned photodiode with MOS-LEFM (lateral electric field controlled photo-charge modulation) gates [8] and CAPD (current-assisted photonic demodulator) [9]. This paper proposes another type of lock-in pixel design using a multiple-tapped pn-junction photodiode and cascading MOS-LEFM gates to them toward the goal for realizing high-performance lock-in pixels which meet above-mentioned requirements.

II. Pixel Design

Fig. 1 shows a basic structure of the proposed lock-in pixel with a 4-tapped pn-junction photodiode. A relevant structure is used for an imager device called pnCCD [10], but the detailed device structure and tuning points for implementing the proposed lock-in pixels are quite different from those of the pnCCD. To implement the lock-in pixel with pinned-photodiode-based CIS process technology, a p+ pinning layer of the pinned photodiode is divided into a few or several p+ regions (4 p+ regions in the case of Fig. 1) which are used for electrodes to control the potential of depleted n-type region of the photo-detector. The depleted n-type regions tapped by p+ electrodes are connected to n+ floating diffusion nodes (in the case of Fig. 1) or storage diode structures. By applying negative voltage (-2 V in Fig. 1) in T1, T2 and T4 electrodes and 0V in T3, the depleted potential in n-type region is controlled to attract photo-electrons to be transferred to the S3 node as shown by lateral electric field (high potential gradient in lateral the

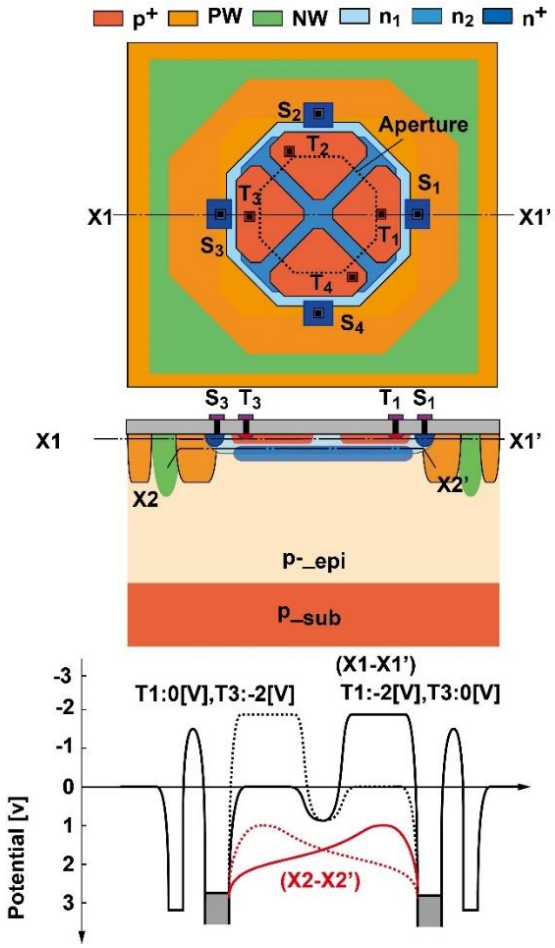

Fig. 1. 4-tapped photodiode charge modulator.

potential profile (red-colored solid-line) on the X2-X2' cross-section line. By carefully tuning the size, shape and doping conditions of the p+ electrode and multiple n-type layers (n1 and n2 in Fig. 1), very-high direction) is created in the depleted n-type region, and potential barriers on X1-X1' cross-section line to prevent hole current between p+ electrodes is also created. Fig. 2 shows an extended lock-in pixel structure cascading the multi-tapped (two taps in the case of Fig. 2) photodiode with MOS-LEFM gates for increasing effective aperture size in which the potential profile to control the direction of photo-carrier flows is modulated.

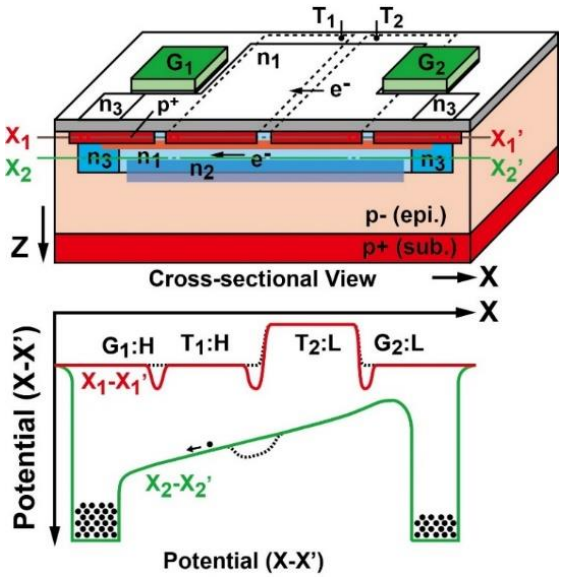

Fig. 2. Hybrid cascade charge modulator.

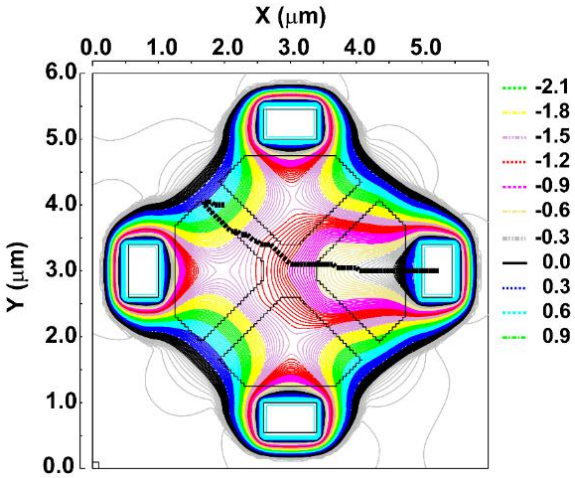

Fig. 3 Simulated potential 2-D plot of the 4-tapped diode modulator (T_2, T_3, T_4:- 2[V], T_1:0[V]).

III. Simulations

Fig. 3 shows a simulated 2-D potential plot of the 4-tapped photodiode modulator with a simplified structure when -2V is applied in T2, T3, T4 terminals, and 0V is applied to T1 and p+ substrate for depleting all the p-epi-layer. In Table 1, simulated photo carrier transfer time from the initial position of photo-carrier generation at (X=2μm, Y=4μm, and Z=3.3, 5.25, 7.2 and 9.15 μm) to S1 node. Extremely fast photo-carrier response time of smaller than 300ps for all the photo-sensitive volume is expected. Fig. 4 shows simulated 1-D potential plot on X1-X1' and X2-X2' lines of Fig. 1. A large modulated depleted potential difference of 1.1V in the channel is obtained by the applied p+ electrode potential difference of 2V. This large potential modulation ratio (55% to the applied control voltage swing) is a reason for the extremely fast photo-carrier response.

Table 1. Simulated carrier transfer time.

Initial Z-position [μm]	Transfer time [ps]
3.3	81
5.25	146
7.2	211
9.15	263

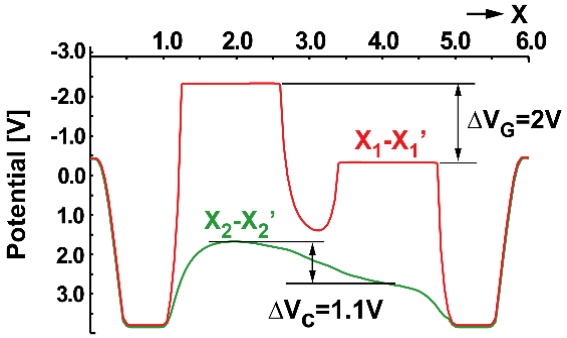

Fig. 4. Simulated potential profiles on X1-X1' and X2-X2' lines

IV. Implementations

A CIS chip for the proof-of-concept (Fig. 5) has been implemented using 0.11um CIS technology with high-resistivity thick-epi substrate. Test structures for 4-tapped lock-in pixels are included as an array of 110(V) x 16(H) pixels in a part of the pixel array in the multiple-purpose CIS chip.

As for preliminary test of the implemented lock-in pixel, a photo-response of the 4 tapped-outputs with

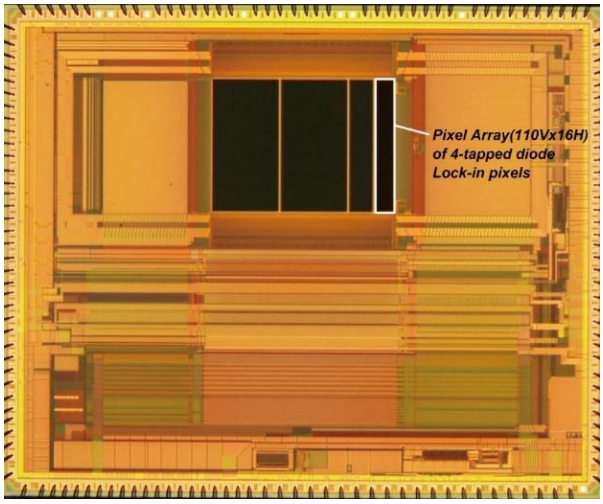

Fig. 5. Implemented CIS chip for the proof-of-concept.

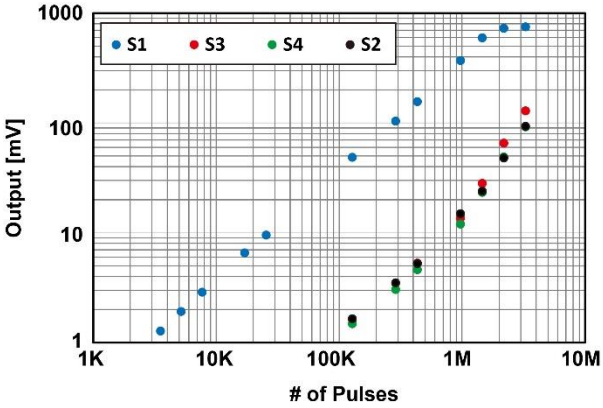

Fig. 6. Response of 4-tap outputs for fixed-tap voltage.

Table II. Relative sensitivity and demodulation contrast of 4 tapped-outputs.

Tap	S1	S2	S3	S4
Relative Sensitivity	0.98	1.03	1.0	1.04
Demodulation Contrast [%]	90.0	93.0	91.6	92.5

stationary gating is measured as shown in Fig. 6. The average of 20[V] x 10[H] pixels is shown. In this measurement, -2V is applied in T_2, T_3, T_4 terminals, and 0V is applied to T_1. High modulation contrast ($S_3/(S_1+S_2+S_3+S_4)$x100[%]) of 90% at around the 50% saturation of S_3 is attained as stationary gating operation. The maximum signal amplitude is 749mV and with the conversion gain of16μV/e-, the FWC is 47,000 [e^-]. In Table II, the relative sensitivity of the 4 outputs (the S3 output is used as the reference of the relative sensitivity) and the demodulation contrast. In this designed pixel for the proof-of concept, the size of pixel is 16.8μm x 16.8μm and the aperture size to attain high modulation contrast with light shielding done by metal layers is designed to be only 2μm x 2μm. As a result the fill factor is only 1.4%. Therefore, this test pixel is not aimed to demonstrate high-sensitivity. For the improvement of the aperture size (fill factor), the modification of the pixel structure using another central p+ tap will be effective as used in photogate-type lock-in pixels [3].

V. Conclusions.

This paper presents a time-resolved lock-in pixel image sensor using multiple-tapped diode and hybrid cascade charge transfer structures. The proposed structure will be useful for implementing lock-in pixels in long-distance TOF range image sensors featuring many tapped-outputs like pixels with 8, 12 and 16 taps, leading to the developments of indirect TOF image sensors suitable for longer range and strong ambient light operation. With the implemented chip, a preliminary test result on stationary gating operation is reported. The demonstration of high-speed modulation characteristics is left as a near future work.

Acknowledgments

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